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PCF8536

Universal LCD driver for low multiplex rates including a 6 channel PWM generator

Rev. 2 — 21 February 2012 Product data sheet

1. General description

The PCF8536 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any multiplexed LCD containing up to eight backplanes, up to 44 segments, and up to 320 elements. The PCF8536 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus (PCF8536AT) or a three line unidirectional SPI-bus (PCF8536BT). Communication overheads are minimized using a display RAM with auto-incremented addressing.

The PCF8536 features an on-chip PWM controller for LED illumination. Up to six independent channels can be configured. Each channel has 128 levels allowing the possibility for two RGB controllers. Each of them provides over 2 million colors. Each channel can also be used for static drive.

2. Features and benefits

- Single-chip 320 segment LCD controller and driver with 6 channel PWM generator
- 6 channel PWM generator for backlight LED illumination
- Selectable display bias configuration
- Wide range for digital power supply: from 1.8 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 9.0 V for high threshold twisted nematic LCDs
- Low power consumption
- Selectable backplane drive configuration: 4, 6, or 8 backplane multiplexing
- LCD and logic supplies may be separated
- 320-bit RAM for display data storage
- 6 PWM outputs with a 7-bit resolution (128 steps) and drivers for external transistors
- Programmable PWM frame frequency to avoid LCD backlight flickering
- 400 kHz I^2C-bus interface (PCF8536AT)
- 5 MHz SPI-bus interface (PCF8536BT)
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of 10 Hz; factory calibrated

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

- 320 segments driven allowing:
  - up to 40 7-segment alphanumeric characters
  - up to 20 14-segment alphanumeric characters
  - any graphics of up to 320 elements
- Manufactured in silicon gate CMOS process

3. Applications

- White goods and consumer products

4. Ordering information

Table 1. Ordering information

Type number	Interface type	Package		
		Name	Description	Version
PCF8536AT/1	I^2C-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCF8536BT/1	SPI-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF8536AT/1	PCF8536AT
PCF8536BT/1	PCF8536BT

6. Block diagram

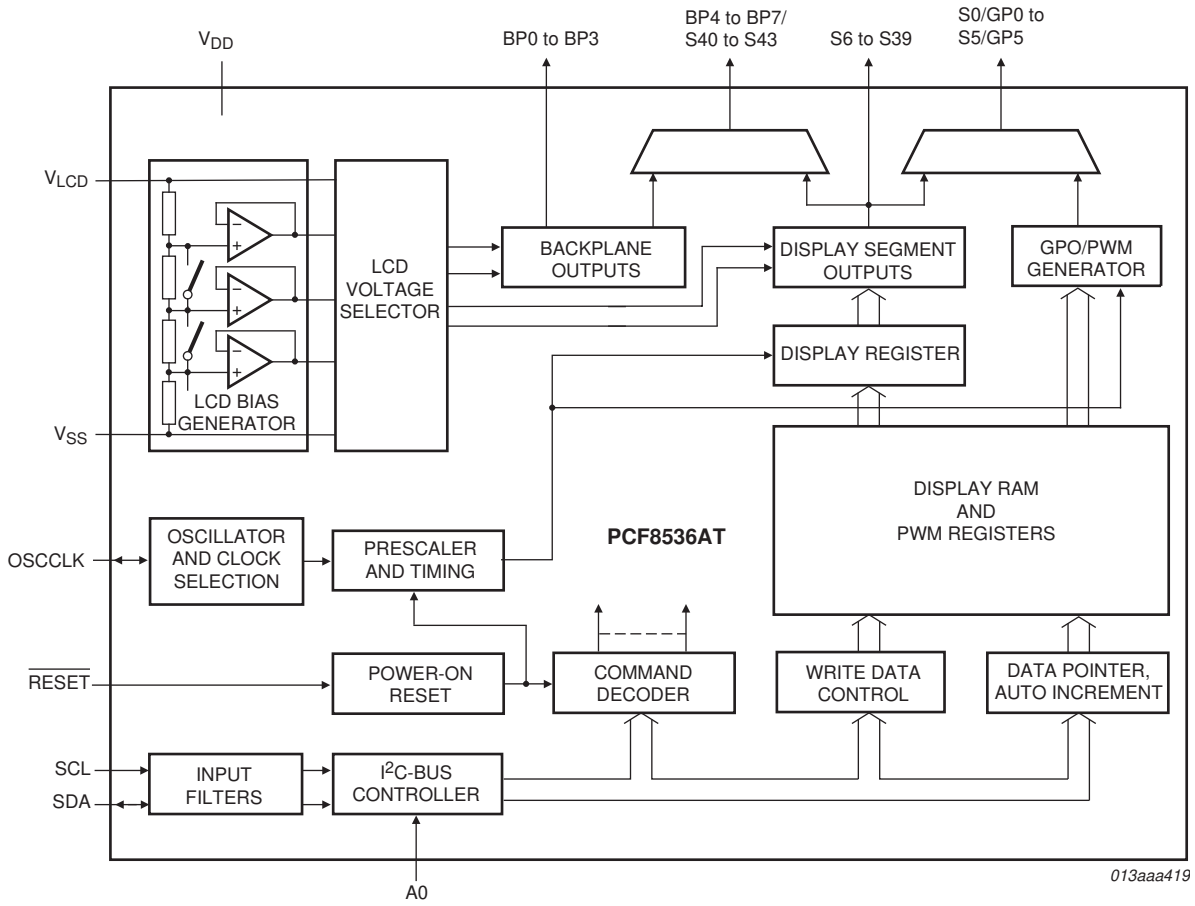


Fig 1. Block diagram of PCF8536AT

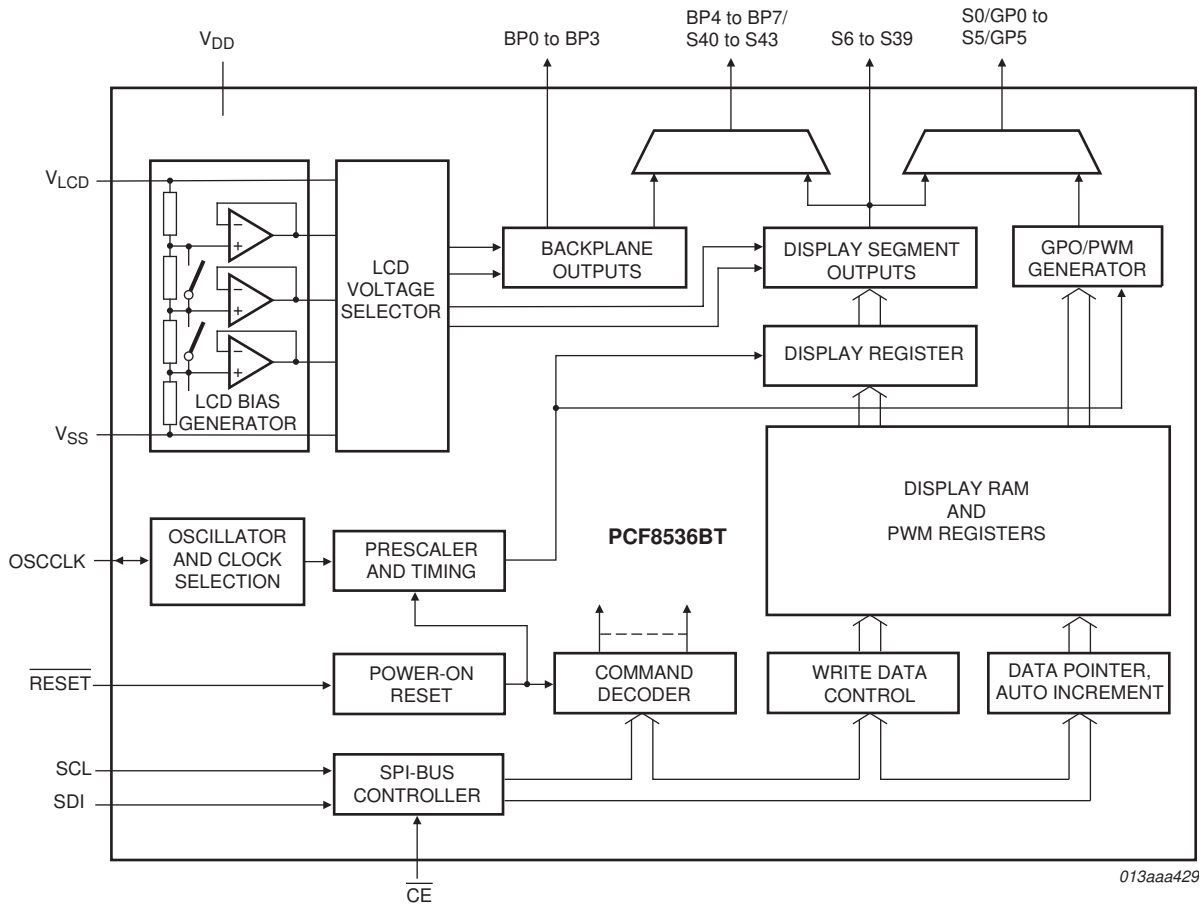
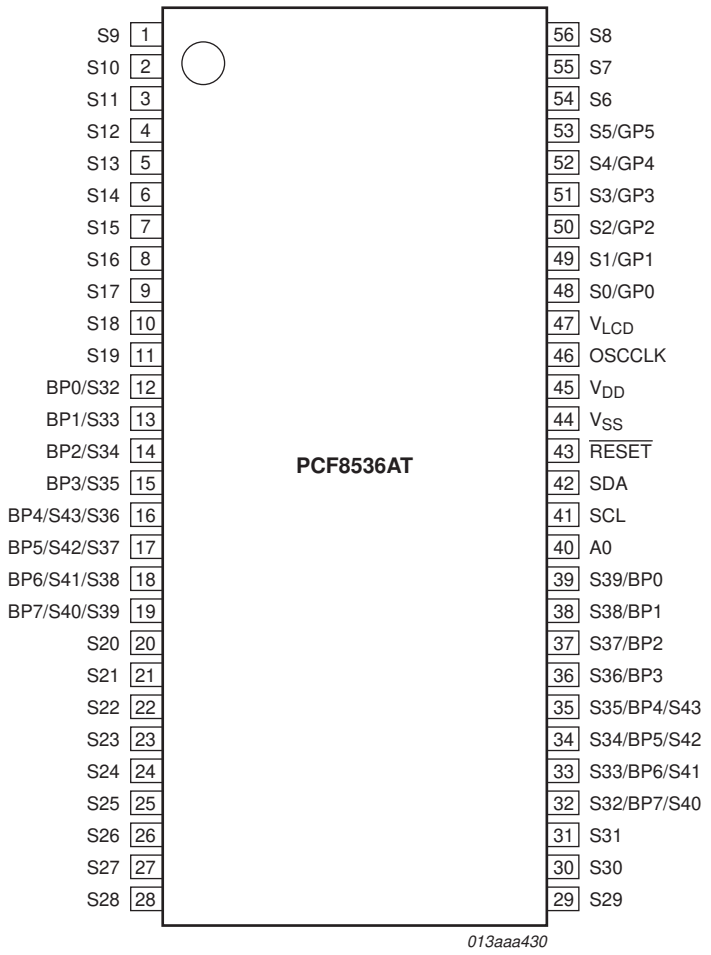


Fig 2. Block diagram of PCF8536BT

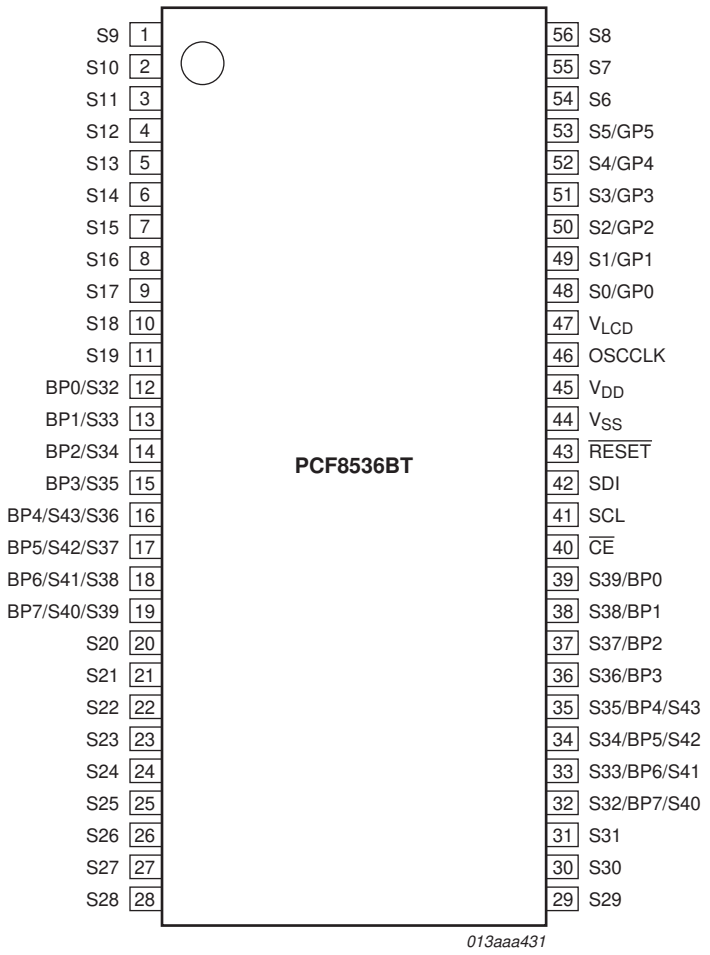
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 51.

Fig 3. Pin configuration for TSSOP56 (PCF8536AT)



Top view. For mechanical details, see Figure 51.

Fig 4. Pin configuration for TSSOP56 (PCF8536BT)

7.2 Pin description

Table 3. Pin description of PCF8536AT and PCF8536BT

Pin	Symbol	Type	Description
1 to 11	S9 to S19	output	LCD segment
20 to 31	S20 to S31	output	LCD segment
43	$\overline{\text{RESET}}$	input	active LOW reset input
44	V_{SS}	supply	ground supply voltage
45	V_{DD}	supply	supply voltage
46	OSCCLK	input/output	external clock input/internal oscillator output
47	V_{LCD}[1]	supply	LCD supply voltage
48 to 53	S0/GP0 to S5/GP5	output	LCD segment/GPO (PWM) output
54 to 56	S6 to S8	output	LCD segment
Pin layout depending on backplane swap configuration[2]			
	BPS = 0	**BPS = 1[3]**	
12	BP0	S32	output	LCD backplane/LCD segment
13	BP1	S33	
14	BP2	S34	
15	BP3	S35	
16	BP4/S43	S36	
17	BP5/S42	S37	
18	BP6/S41	S38	
19	BP7/S40	S39	
32	S32	BP7/S40	
33	S33	BP6/S41	
34	S34	BP5/S42	
35	S35	BP4/S43	
36	S36	BP3	
37	S37	BP2	
38	S38	BP1	
39	S39	BP0	
Pin layout depending on product and bus type			
	PCF8536AT	**PCF8536BT**	
40	A0		input	I^2C-bus slave address selection
		$\overline{\text{CE}}$	input	SPI-bus chip enable - active LOW
41	SCL		input	I^2C-bus serial clock
		SCL	input	SPI-bus serial clock
42	SDA		input/output	I^2C-bus serial data
		SDI	input	SPI-bus data input

[1] V_{LCD} must be equal to or greater than V_{DD}.

[2] Effect of backplane swapping is illustrated in Figure 5 on page 10.

[3] Bit BPS is explained in Section 8.1.4 on page 9.

8. Functional description

The PCF8536 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs and 6 backlight LEDs. It can directly drive any multiplexed LCD containing up to eight backplanes and up to 44 segments.

8.1 Commands of PCF8536

The PCF8536 is controlled by 15 commands, which are defined in Table 4. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCF8536.

Table 4. Commands of PCF8536

Command name	Register selection RS[1:0][1]		Bits								Reference
			7	6	5	4	3	2	1	0	
initialize	0	0	0	0	0	1	0	1	1	0	Section 8.1.1
OTP-refresh	0	0	1	1	1	1	0	0	0	0	Section 8.1.2
PWM-inversion	0	0	0	0	0	1	0	1	0	PWMI	Section 8.1.3
mode-settings	0	0	0	1	0	1	BPS	INV	PD	E	Section 8.1.4
oscillator-control	0	0	0	0	0	1	1	EFR	COE	OSC	Section 8.1.5
GPO-output-config	0	0	1	1	0	0	GPM1[1:0]		GPM0[1:0]		Section 8.1.6
	0	0	1	1	0	1	GPM3[1:0]		GPM2[1:0]		
	0	0	1	1	1	0	GPM5[1:0]		GPM4[1:0]		
set-MUX-mode	0	0	0	0	0	0	0	0	M[1:0]		Section 8.1.7
set-bias-mode	0	0	0	0	0	0	0	1	B[1:0]		Section 8.1.8
frame-frequency-LCD	0	0	0	0	1	FD[4:0]					Section 8.1.9
frame-frequency-PWM	0	0	0	1	0	0	FP[3:0]				Section 8.1.10
GPO-static-data	0	0	0	1	1	0	0	GPO2	GPO1	GPO0	Section 8.1.11
	0	0	0	1	1	0	1	GPO5	GPO4	GPO3	
load-data-pointer-LCD	0	0	1	0	DP[5:0]						Section 8.1.12
load-data-pointer-PWM	0	0	0	1	1	1	0	PP[2:0]			Section 8.1.13
write-RAM-data	0	1	D[7:0]								Section 8.1.14
write-PWM-data	1	0	0	P[6:0]							Section 8.1.15

[1] Information about control byte and register selection see Section 9.1 on page 46.

8.1.1 Command: initialize

This command generates a chip-wide reset. It has the same function as the $\overline{\text{RESET}}$ pin. Reset takes 1 ms to complete.

Table 5. Initialize - initialize command bit description

Bit	Symbol	Value	Description
7 to 0	-	00010110	fixed value

8.1.2 Command: OTP-refresh

During production and testing of the device, each IC is calibrated to achieve the specified accuracy of the frame frequency. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. The device reads these cells every time the OTP-refresh command is sent. This instruction has to be sent after a reset has been made and before the display is enabled.

This command will be completed after a maximum of 30 ms and requires either the internal or external clock to run. If the internal oscillator is not used, then a clock must be supplied to the OSCCLK pin. If the OTP-refresh instruction is sent and no clock is present, then the request is stored until a clock is available.

Remark: It is recommended not to enter power-down mode during the OTP refresh cycle.

Table 6. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
7 to 0	-	11110000	fixed value

8.1.3 Command: PWM-inversion

It is possible to invert the output of the PWM generators. This function may be useful for counteracting EMC issues. The description of this mode can be found in Section 8.11.2 on page 45.

Table 7. PWM-inversion - PWM inversion command bit description

Bit	Symbol	Value	Description
7 to 1	-	0001010	fixed value
0	PWMI		**PWM inversion mode**
		1	PWM inversion mode on
		0[1]	PWM inversion mode off

[1] Default value.

8.1.4 Command: mode-settings

Table 8. Mode-settings - mode settings command bit description

Bit	Symbol	Value	Description
7 to 4	-	0101	fixed value
3	BPS		**backplane swapping**
		0[1]	backplane configuration 0
		1	backplane configuration 1
2	INV		**set inversion mode**
		0[1][2]	Driving scheme A: LCD line inversion mode
		1	Driving scheme B: LCD frame inversion mode
1	PD		**set power mode**
		1	power-down mode; backplane and segment outputs are connected to V_{SS} and the internal oscillator is switched off
		0[1]	power-up mode
0	E		**display switch**
		0[1]	display disabled; backplane and segment outputs are connected to V_{SS}
		1	display enabled

[1] Default value.

[2] See Section 8.1.4.2.

8.1.4.1 Backplane swapping

Backplane swapping can be configured with the BPS bit (see Table 8). It moves the location of the backplane and the associated segment outputs from one side of the PCF8536 to the other. Backplane swapping is sometimes desirable to aid with the routing of PCBs that do not use multiple layers.

The BPS bit has to be set to the required value before enabling the display. Failure to do so does not damage the PCF8536 or the display, however unexpected display content may appear.

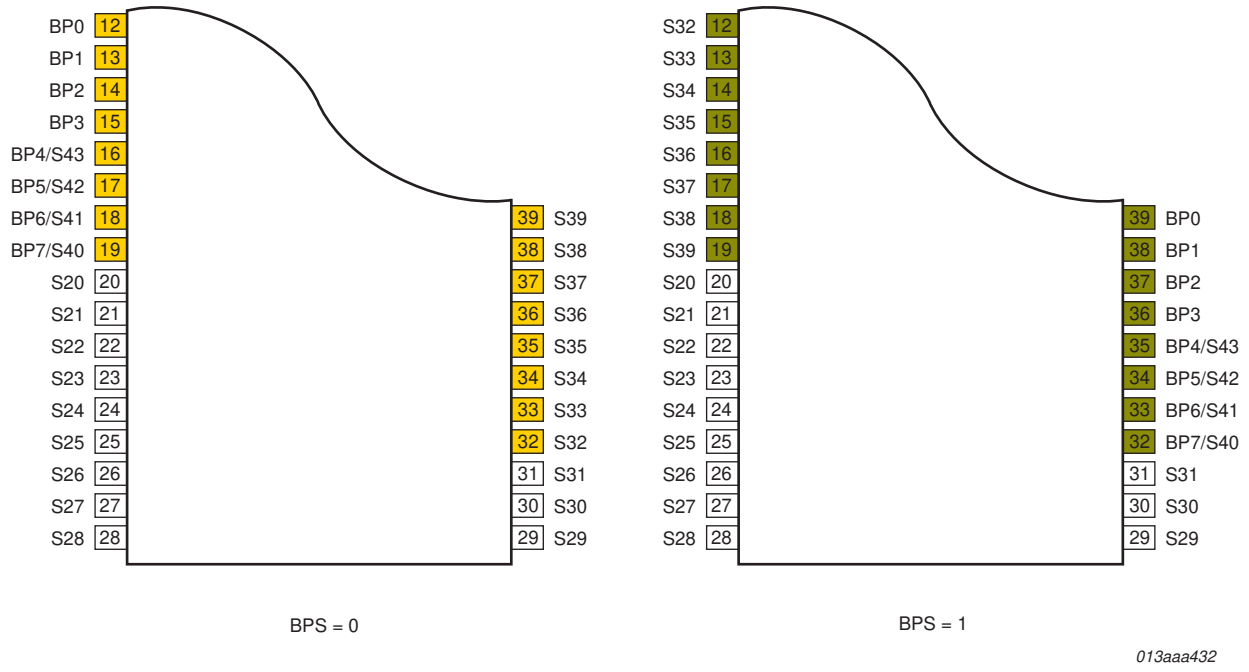


Fig 5. Effect of backplane swapping

8.1.4.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The DC offset of the voltage across the LCD is compensated over a certain period: line-wise in line inversion mode (driving scheme A) or frame-wise in frame inversion mode (driving scheme B). With the INV bit (see Table 8), the compensation mode can be switched.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption; therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined; however, since the switching frequency is reduced, there is possibility for flicker to occur.

The waveforms of Figure 15 on page 29 to Figure 18 on page 32 are showing line inversion mode. Figure 19 on page 33 shows an example of frame inversion.

8.1.4.3 Power-down mode

The power-down bit (PD) allows the PCF8536 to be put in a minimum power configuration. In order to avoid display artefacts, it is recommended to enter power-down only after the display has been switched off by setting bit E to logic 0.

During power-down, the internal oscillator is switched off and any selected PWM output is revert to the static value stored in bits GPO0 to GPO5. These bits may be programmed to give a static logic 0 or static logic 1 on selected GP0 to GP5 pins.

Table 9. Effect of the power-down bit (PD)

Effect on function	Mode settings	Effect of setting PD	
		0	1
backplane output	E = 1	normal function	V_{SS}
segment output	E = 1	normal function	V_{SS}
internal oscillator	OSC = 0, COE = 1	on	off
OSCCLK pin	OSC = 0, COE = 1	output of internal oscillator frequency	V_{DD}
OSCCLK pin	OSC = 1	input clock	clock input, can be logic 0, logic 1, or left floating
GPO	static drive	static drive	static drive
GPO	PWM drive	PWM drive	static drive

With the following sequence, the PCF8536 can be set to a state of minimum power consumption, called power-down mode.

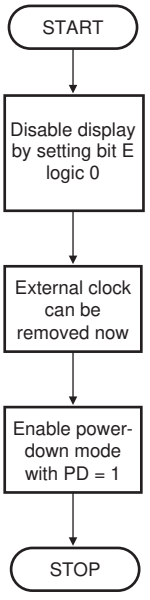


Fig 6. Recommended power-down sequence

Remarks:

- It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see Section 10). Otherwise it may cause unwanted display artifacts. In case of an uncontrolled removal of supply voltages, the PCF8536 will not be damaged.
- Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

- A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to disable the display first and afterwards to remove the clock signal.

8.1.4.4 Display enable

The display enable bit (E) is used to enable and disable the display. When the display is disabled, all LCD outputs go to V_{SS}. This function is implemented to ensure that no voltage can be induced on the LCD outputs as it may lead to unwanted displays of segments.

Recommended start-up sequences are found in Section 8.2.3

Remarks:

- The state of display enable has no effect on the GPO outputs.
- Display enable is not synchronized to an LCD frame boundary. Therefore using this function to flash a display for prolonged periods is not recommended due to the possible build-up of DC voltages on the display.

8.1.5 Command: oscillator-control

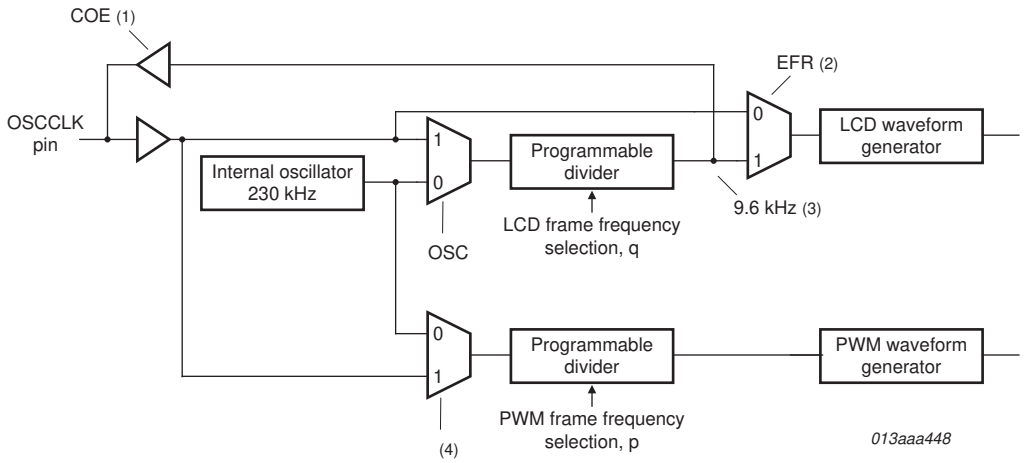
The oscillator-control command switches between internal and external oscillator and enables or disables the pin OSCCLK. It is also used to define what the external frequency will be.

Table 10. Oscillator-control - oscillator control command bit description

Bit	Symbol	Value	Description
7 to 3	-	00011	fixed value
2	EFR		**external clock frequency** applied on pin OSCCLK
		0[1]	9.6 kHz
		1	230 kHz
1	COE		**clock output enable for pin OSCCLK**
		0[1]	clock signal not available on pin OSCCLK; pin OSCCLK is in 3-state
		1	clock signal available on pin OSCCLK
0	OSC		**oscillator source**
		0[1]	internal oscillator running
		1	external oscillator used; pin OSCCLK becomes an input; used in combination with EFR to determine input frequency

[1] Default value.

The bits OSC, COE, and EFR control the source and frequency of the clock used to generate the LCD and PWM signals (see Figure 7). Valid combinations are shown in Table 11.



(1) Can only be used with the internal oscillator (OSC = 0).

(2) Can only be used with an external oscillator (OSC = 1).

(3) Nominal value for divide factor q is 24; source clock is 230 kHz (see Section 8.1.9).

(4) PWM requires an external or internal 230 kHz clock.

Fig 7. Oscillator selection

Table 11. Valid combinations of bits OSC, EFR, and COE

OSC	COE	EFR	OSCCLK pin	Clock source
0	0	not used	inactive; may be left floating	internal oscillator used
0	1	not used	output of internal oscillator frequency (prescaler)	internal oscillator used
1	not used	0	9.6 kHz input	OSCCLK pin
1	not used	1	230 kHz input	OSCCLK pin

Table 12. Typical use of bits OSC, EFR, and COE

Usage	OSC	CDE	EFR
LCD and/or PWM with internal oscillator	0	0	not used
LCD and PWM with external oscillator	1	not used	1
LCD with external oscillator	1	not used	0

8.1.5.1 Oscillator

The internal logic and LCD drive signals of the PCF8536 are timed either by the built-in oscillator or from an external clock.

Internal clock: When the internal oscillator is used, all LCD and PWM signals are generated from it. The oscillator runs at nominal 230 kHz. The relationship between this frequency and the LCD frame frequency is detailed in Section 8.1.9. The relationship between this frequency and the PWM frame frequency is detailed in Section 8.1.10.

Control over the internal oscillator is made with the OSC bit (see Section 8.1.5). The internal oscillator is also switched on or off under certain combinations of modes which are described in Table 13.

Table 13. Internal oscillator on/off table

PD	OSC	PWM	EFR	Internal oscillator state[1]
power-down	n.a.	n.a.	n.a.	off
power-up	internal oscillator	n.a.	n.a.	on
	external oscillator	off	n.a.	off
		on	9.6 kHz	on[2]
		on	230 kHz	off

[1] When $\overline{\text{RESET}}$ is active, the internal oscillator is off.

[2] Special case. The PWM generator needs 230 kHz and must be enabled when PWM is enabled.

It is possible to make the internal oscillator signal available on pin OSCCLK by using the oscillator-control command (see Table 10) and configuring the clock output enable (COE) bit. If not required, the pin OSCCLK should be left open or connected to V_{SS}. At power-on the signal at pin OSCCLK is disabled and pin OSCCLK is in 3-state.

Clock output is only valid when using the internal oscillator. The signal will appear on the OSCCLK pin.

An intermediate clock frequency is available at the OSCCLK pin. The duty cycle of this clock varies with the chosen divide ratio.

Table 14. OSCCLK table

PD	OSC	COE	EFR	OSCCLK pin[1]
power-down	n.a.	off	n.a.	3-state[2]
power-down	n.a.	on	n.a.	V_{DD}
power-up	internal oscillator	off	n.a.	3-state
		on	n.a.	9.6 kHz output[3]
	external oscillator	n.a.	9.6 kHz	9.6 kHz input
			230 kHz	230 kHz input

[1] When $\overline{\text{RESET}}$ is active, the pin OSCCLK is in 3-state.

[2] In this state, an external clock may be applied, but it is not a requirement.

[3] 9.6 kHz is the nominal frequency with q = 24, see Table 15.

External clock: In applications where an external clock must be applied to the PCF8536, bit OSC (see Table 10) has to be set logic 1. In this case pin OSCCLK becomes an input.

The OSCCLK signal must switch between the V_{SS} and the V_{DD} voltage supplied to the chip.

The system is designed for a 230 kHz clock or alternatively for using a 9.6 kHz clock. The EFR bit determines the external clock frequency. The clock frequency ($f_{clk(ext)}$) in turn determines the LCD frame frequency, see Table 15.

The PWM generator requires a 230 kHz clock to operate. If PWM is enabled and an external clock of 9.6 kHz is selected, then the internal oscillator will automatically start and be used for the PWM signal generation.

Remark: If an external clock is used, then this clock signal must always be supplied to the device when the display is on. Removing the clock may freeze the LCD in a DC state which will damage the LCD material.

8.1.5.2 Timing and frame frequency

The timing of the PCF8536 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 15). The frame frequency is a fixed division of the internal clock or of the frequency applied to pin OSCCLK when an external clock is used.

Table 15. LCD frame frequencies

Frame frequency	Typical external frequency (Hz)	Nominal frame frequency (Hz)	EFR bit	Value of q[1]
$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48}$	9600	200	0	-
$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q}$	230000	200	1	24

[1] Other values of the frame frequency prescaler see Table 21.

When the internal clock is used, or an external clock with EFR = 1, the LCD frame frequency can be programmed by software in steps of approximately 10 Hz in the range of 60 Hz to 300 Hz (see Table 21). Furthermore the internal oscillator is factory calibrated, see Table 44 on page 59.

8.1.6 Command: GPO-output-config

The behavior of the combined LCD and GPO outputs S5/GP5 to S0/GP0 is configured with the bits described in Table 16.

Table 16. GPO-output-config - output mode config command for S5/GP5 to S0/GP0

Bit	Symbol	Value	Description
GPM0 and GPM1			
7 to 4	-	1100	fixed value
3 to 2	GPM1[1:0]	see Table 17	output mode for S1/GP1
1 to 0	GPM0[1:0]	see Table 17	output mode for S0/GP0
GPM2 and GPM3			
7 to 4	-	1101	fixed value
3 to 2	GPM3[1:0]	see Table 17	output mode for S3/GP3
1 to 0	GPM2[1:0]	see Table 17	output mode for S2/GP2
GPM4 and GPM5			
7 to 4	-	1110	fixed value
3 to 2	GPM5[1:0]	see Table 17	output mode for S5/GP5
1 to 0	GPM4[1:0]	see Table 17	output mode for S4/GP4

Each output can be individually configured to be either an LCD segment output, a PWM output or a static general-purpose output (GPO), see Table 17.

Remark: Even if using GPO only, V_{LCD} must still be applied to the device.

Table 17. GPMO mode definition

GPM0[1:0] to GPM5[1:0]	Mode	Description
00[1], 01	LCD	output is an LCD segment
10	static	output is static GPO
11	PWM	output is PWM GPO

[1] Default value.

8.1.7 Command: set-MUX-mode

The multiplex drive mode is configured with the bits described in Table 18.

Table 18. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000000	fixed value
1 to 0	M[1:0]	00[1], 01	1:8 multiplex drive mode; eight backplanes
		10	1:6 multiplex drive mode; 6 backplanes
		11	1:4 multiplex drive mode; 4 backplanes

[1] Default value.

8.1.8 Command: set-bias-mode

The set-bias-mode command allows setting the bias level.

Table 19. Set-bias-mode - set bias mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000001	fixed value
1 to 0	B[1:0]	00[1], 01	1/4 bias
		11	1/3 bias
		10	1/2 bias

[1] Default value.

8.1.9 Command: frame-frequency-LCD

With the frame-frequency-LCD command, the frame frequency for the display can be configured. The clock frequency determines the frame frequency.

Table 20. Frame-frequency-LCD - frame frequency and output clock frequency command bit description

Bit	Symbol	Value	Description
7 to 5	-	001	fixed value
4 to 0	FD[4:0]	see Table 21	frequency prescaler

The system is designed for a 230 kHz clock. It is either internally generated or externally provided. Alternatively a 9.6 kHz clock signal can be provided as well. The EFR bit (see Table 10) has to be set according to the external clock frequency.

When EFR is set to 9.6 kHz, then the LCD frame frequency is calculated with Equation 1:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48} \quad (1)$$

When EFR is set to 230 kHz, then the LCD frame frequency is calculated with Equation 2:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q} \quad (2)$$

where q is the frequency divide factor (see Table 21).

Remark: $f_{clk(ext)}$ is the external input clock frequency to pin OSCCLK.

When the internal oscillator is used, the intermediate frequency may be output on the OSCCLK pin. Its frequency is given in Table 21.

Table 21. Frame frequency prescaler values for 230 kHz clock operation

FD[4:0]	Nominal LCD frame frequency (Hz)[1]	Divide factor, q	Intermediate clock frequency (Hz)
00000	59.9	80	2875
00001	70.5	68	3382
00010	79.9	60	3833
00011	90.4	53	4340
00100	99.8	48	4792
00101	108.9	44	5227
00110	119.8	40	5750
00111	129.5	37	6216
01000	140.9	34	6765
01001	149.7	32	7188
01010	159.7	30	7667
01011	171.1	28	8214
01100	177.5	27	8519
01101	191.7	25	9200
01110[2]	199.7	24	9583
01111	208.3	23	10000
10000	217.8	22	10455
10001	228.3	21	10952
10010	239.6	20	11500
10011	252.2	19	12105
10100	266.2	18	12778
10101	281.9	17	13529
10110	299.5	16	14375
10111 to 11111	not used		

[1] Nominal frame frequency calculated for the default clock frequency of 230 kHz.

[2] Default value.

8.1.10 Command: frame-frequency-PWM

With the frame-frequency-PWM command, the frame frequency for the PWM signal can be set.

The PWM system requires a clock of 230 kHz either internally generated or externally supplied. Using a slower clock may result in visible flickering of LEDs driven with the PWM signal.

When EFR is set to 230 kHz, then the PWM frame frequency will be calculated with Equation 3:

$$f_{PWM} = \frac{f_{clk(ext)}}{128 \cdot p} \quad (3)$$

where p is the frequency divide factor (see Table 23).

Table 22. Frame-frequency-PWM - PWM frame frequency command bit description

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	FP[3:0]	see Table 23	frequency prescaler

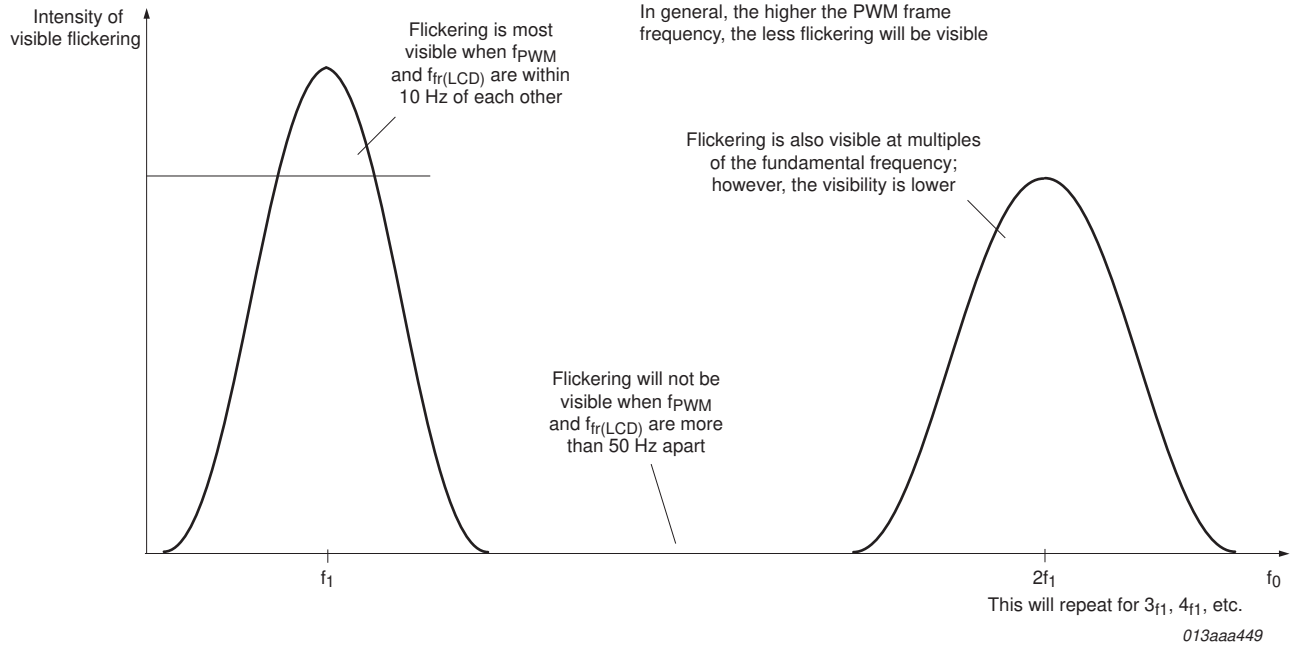
Table 23. PWM frame frequency prescaler values for 230 kHz clock operation

FP[3:0]	Nominal PWM frame frequency (Hz)[1]	Divide factor, p
0000	59.9	30
0001	69.1	26
0010	81.7	22
0011	89.8	20
0100	99.8	18
0101	112.3	16
0110	119.8	15
0111[2]	128.3	14
1000	138.2	13
1001	149.7	12
1010	163.4	11
1011	179.7	10
1100	199.7	9
1101	224.6	8
1110	256.7	7
1111	299.5	6

[1] Nominal frame frequency calculated for the default clock frequency of 230 kHz.

[2] Default value.

In order to avoid flickering caused by the interaction of the backlight LED and the LCD frame frequency, the PWM frame frequency should be programmed to be more than 50 Hz different from LCD frame frequency or multiples of the LCD frame frequency (see Figure 8 and Table 49 on page 68).



Where $f_0 = f_{PWM}$ and $f_1 = f_{fr(LCD)}$ or $f_1 = f_{PWM}$ and $f_0 = f_{fr(LCD)}$.

Fig 8. Flicker avoidance for LED backlighting

8.1.11 Command: GPO-static-data

When static GPOs are selected instead of PWM, then the value for the output is taken from these register bits. The output is a static level.

Table 24. GPO-static-data - write GPO data for GP0 to GP5 command bit description

Bit	Symbol	Value	Description
GPO0 to GPO2			
7 to 3	-	01100	fixed value
2	GPO2	0[1]	0 level output on pin GP2
		1	1 level output on pin GP2
1	GPO1	0[1]	0 level output on pin GP1
		1	1 level output on pin GP1
0	GPO0	0[1]	0 level output on pin GP0
		1	1 level output on pin GP0
GPO3 to GPO5			
7 to 3	-	01101	fixed value
2	GPO5	0[1]	0 level output on pin GP5
		1	1 level output on pin GP5
1	GPO4	0[1]	0 level output on pin GP4
		1	1 level output on pin GP4
0	GPO3	0[1]	0 level output on pin GP3
		1	1 level output on pin GP3

[1] Default value.

8.1.12 Command: load-data-pointer-LCD

The load-data-pointer-LCD command defines the start address of the display RAM. The data pointer is auto incremented after each RAM write. The size of the display RAM is dependent on the current multiplex drive mode setting, see Table 25.

Table 25. Load-data-pointer-LCD - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 6	-	10	fixed value
Multiplex drive mode 1:8			
5 to 0	DP[5:0]	000000[1] to 100111	6-bit binary value of 0 to 39
Multiplex drive mode 1:6			
5 to 0	DP[5:0]	000000[1] to 101001	6-bit binary value of 0 to 41
Multiplex drive mode 1:4			
5 to 0	DP[5:0]	000000[1] to 101011	6-bit binary value of 0 to 43

[1] Default value.

Remark: Data pointer values outside of the valid range will be ignored and no RAM content will be transferred until a valid data pointer value is set.

Filling of the display RAM is described in Section 8.9.

8.1.13 Command: load-data-pointer-PWM

The load-data-pointer-PWM command defines one of the 6 PWM addresses.

Table 26. Load-data-pointer-PWM - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 3	-	01110	fixed value
2 to 0	PP[2:0]	000[1] to 101	3-bit binary value of 0 to 5

[1] Default value.

Remark: Data pointer values outside of the valid range will be ignored and no PWM content will be transferred until a valid data pointer value is set.

8.1.14 Command: write-RAM-data

This command will initiate the transfer of data to the display RAM. Data will be written into the address defined by the load-data-pointer-LCD command. RAM filling is described in Section 8.9.

Table 27. Write-RAM-data - write RAM data command bit description[1]

Bit	Symbol	Value	Description
7 to 0	D[7:0]	00000000 to 11111111[2]	writing data byte-wise to RAM

[1] For this command to be effective bit RS[1:0] of the control byte has to be set logic 01, see Table 36 on page 46.

[2] After Power-On Reset (POR), the RAM content is random and should be brought to a defined status by writing meaningful content otherwise unexpected display content may appear.

8.1.15 Command: write-PWM-data

This command will initiate the transfer of data to the PWM registers. Data will be written into the address defined by the load-data-pointer-PWM command. PWM register filling is described in Section 8.10

Table 28. Write-PWM-data - write PWM data command bit description[1]

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000[2] to 1111111	writing data byte-wise to PWM registers

[1] For this command to be effective bit RS[1:0] of the control byte has to be set logic 10, see Table 36 on page 46.

[2] Default value. After Power-On Reset (POR) the PWM content is set to 0.

8.2 Start-up and shut-down

8.2.1 Reset and Power-On Reset (POR)

After a reset and at power-on the PCF8536 resets to starting conditions as follows:

1. The display is disabled.
2. All backplane outputs are set to V_{SS}.
3. All segment outputs are set to V_{SS}.
4. All GPO outputs are disabled.
5. Selected drive mode is: 1:8 with $^1/_4$ bias.
6. The data pointers are cleared (set logic 0).
7. PWM values are all reset to zero.
8. RAM data is not initialized. Its content can be considered to be random.
9. The internal oscillator is running; no clock signal is available on pin OSCCLK; pin OSCCLK is in 3-state.

The reset state is as shown in Table 29.

Table 29. Reset state

Reset state of configurable bits shown in the command table format for clarity.

Associated command	Bits							
	7	6	5	4	3	2	1	0
PWM-inversion								PWMI = 0
mode-settings	-	-	-	-	BPS = 0	INV = 0	PD = 0	E = 0
oscillator-control	-	-	-	-	-	EFR = 0	COE = 0	OSC = 0
GPO-output-config	-	-	-	-	GPM1[1:0] = 00		GPM0[1:0] = 00	
	-	-	-	-	GPM3[1:0] = 00		GPM2[1:0] = 00	
	-	-	-	-	GPM5[1:0] = 00		GPM4[1:0] = 00	
set-MUX-mode	-	-	-	-	-	-	M[1:0] = 00	
set-bias-mode	-	-	-	-	-	-	B[1:0] = 00	
frame-frequency-LCD	-	-	-	FD[4:0] = 01110				
frame-frequency-PWM	-	-	-	-	FP[3:0] = 0111			
GPO-static-data	-	-	-	-	-	GPO2 = 0	GPO1 = 0	GPO0 = 0
	-	-	-	-	-	GPO5 = 0	GPO4 = 0	GPO3 = 0
load-data-pointer-LCD	-	-	DP[5:0] = 000000					
load-data-pointer-PWM	-	-	-	-	-	PP[2:0] = 000		

The first command sent to the device after the power-on event must be the initialize command (see Section 8.1.1).

After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined state by writing meaningful content (e.g. a graphic) otherwise unwanted display artifacts may appear on the display.

8.2.2 $\overline{\text{RESET}}$ pin function

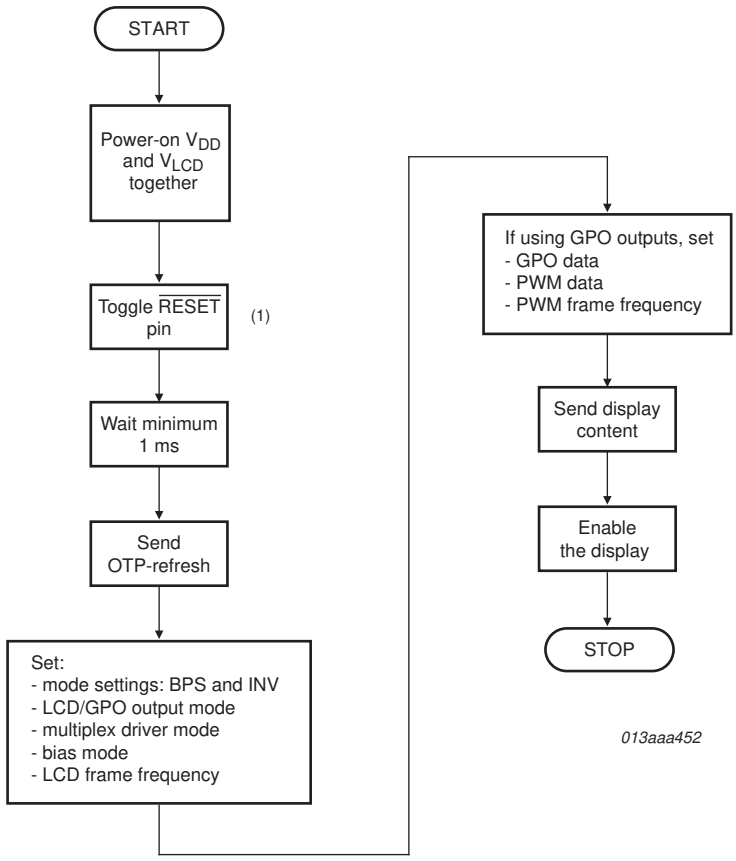
The $\overline{\text{RESET}}$ pin of the PCF8536 will reset all the registers to their default state. The reset state is given in Table 29. The RAM contents will remain unchanged. After the reset signal is removed, the PCF8536 will behave in the same manner as after Power-On Reset (POR). See Section 8.2.1 for details.

8.2.3 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.

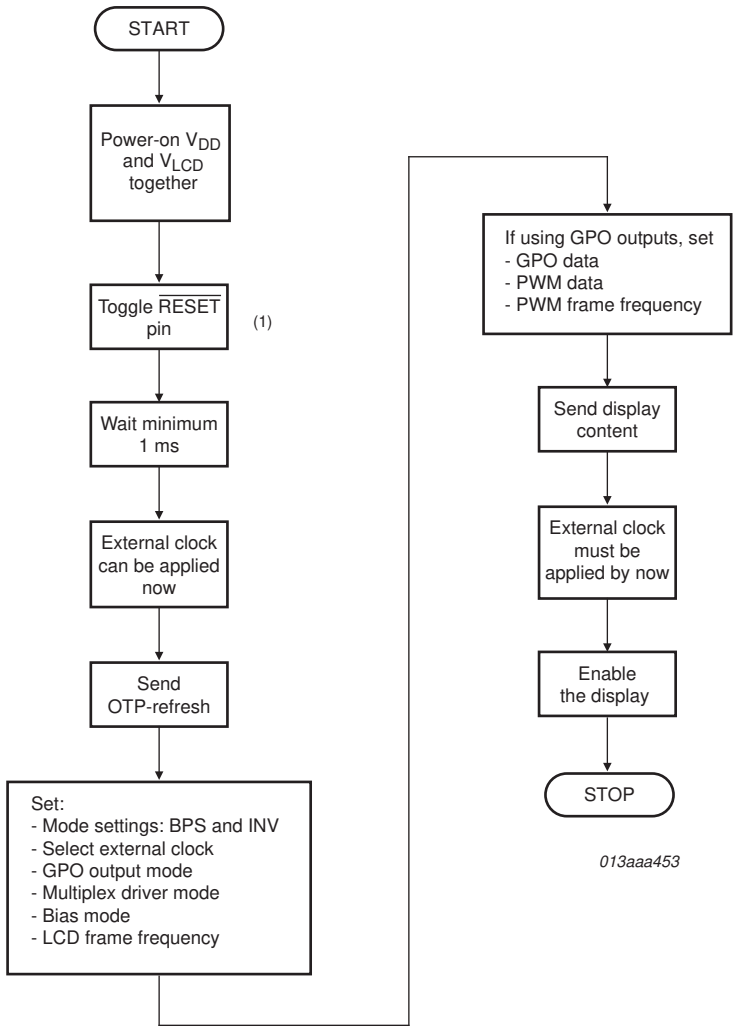
In general, the sequence should always be:

1. Power-on the device,
2. set the display and functional modes,
3. fill the display memory and then
4. turn on the display.



(1) Alternatively, it is possible to send the initialize command.

Fig 9. Recommended start-up sequence when using the internal oscillator



(1) Alternatively, it is possible to send the initialize command.

Fig 10. Recommended start-up sequence when using an external clock signal

8.3 Possible display configurations

The PCF8536 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 11). It can drive multiplexed LCD with 4, 6, or 8 backplanes and up to 44 segments.

The display configurations possible with the PCF8536 depend on the number of active backplane outputs required. A selection of possible display configurations is given in Table 30.

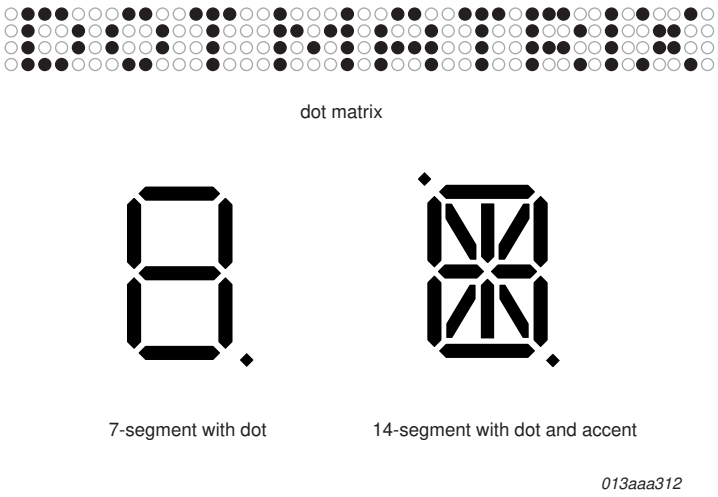


Fig 11. Example of displays suitable for PCF8536

Table 30. Selection of display configurations

Number of			Digits/Characters		Dot matrix/ Elements
Backplanes	Segments	Icons	7 segment[1]	14 segment[2]	
No GPO or PWM outputs enabled					
8	40	320	40	20	320
6	42	252	31	15	252
4	44	176	22	11	176
With 6 GPO or PWM outputs enabled					
8	34	272	34	17	272
6	36	216	27	13	216
4	38	152	19	9	152

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

All of the display configurations in Table 30 can be implemented in the typical systems shown in Figure 12 and Figure 13.