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PCF8545

Universal LCD driver for multiplex rates up to 1:8

Rev. 1 — 13 November 2013 Product data sheet

1. General description

The PCF8545 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any multiplexed LCD containing up to eight backplanes, and up to 320 elements. The PCF8545 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus (PCF8545A) or a three line unidirectional SPI-bus (PCF8545B). Communication overheads are minimized using a display RAM with auto-incremented addressing.

For a selection of NXP LCD segment drivers, see Table 40 on page 61.

2. Features and benefits

- Single-chip 320 elements LCD controller and driver
- Wide range for digital power supply: from 1.8 V to 5.5 V
- LCD supply range from 2.5 V up to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption
- Selectable backplane drive configuration: 4, 6, or 8 backplane multiplexing
- Selectable display bias configuration
- 320-bit RAM for display data storage
- 400 kHz I^2C-bus interface (PCF8545A)
- 5 MHz SPI-bus interface (PCF8545B)
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of 10 Hz; factory calibrated
- 320 segments driven allowing:
  - up to 40 7-segment alphanumeric characters
  - up to 20 14-segment alphanumeric characters
  - any graphics of up to 320 elements
- Manufactured in silicon gate CMOS process

3. Applications

- Industrial and consumer products

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21.

4. Ordering information

Table 1. Ordering information

Type number	Interface type	Package		
		Name	Description	Version
PCF8545ATT	I^2C-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCF8545BTT	SPI-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8545ATT/A	935302987118	PCF8545ATT/AJ	1	tape and reel, 13 inch
PCF8545BTT/A	935302988118	PCF8545BTT/AJ	1	tape and reel, 13 inch

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF8545ATT/A	PCF8545ATT
PCF8545BTT/A	PCF8545BTT

6. Block diagram

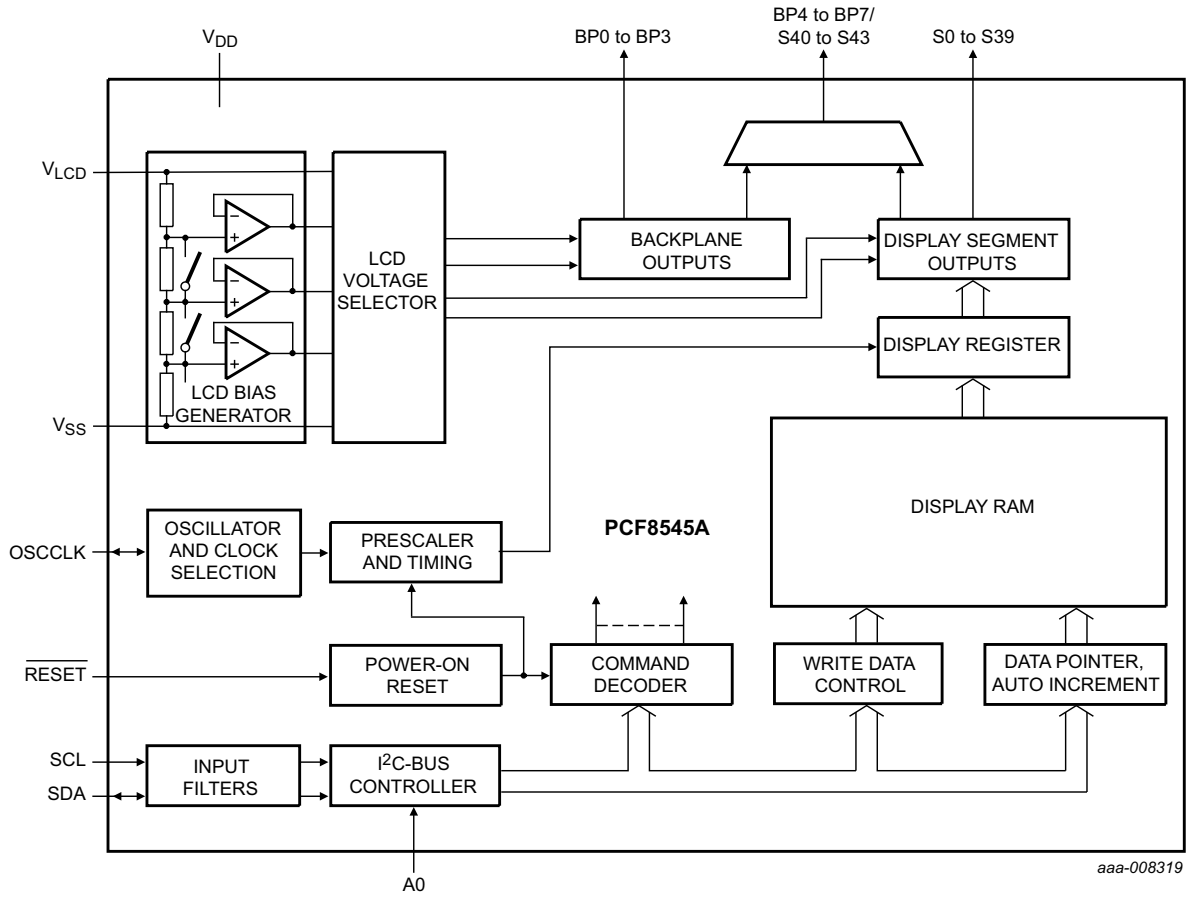


Fig 1. Block diagram of PCF8545A

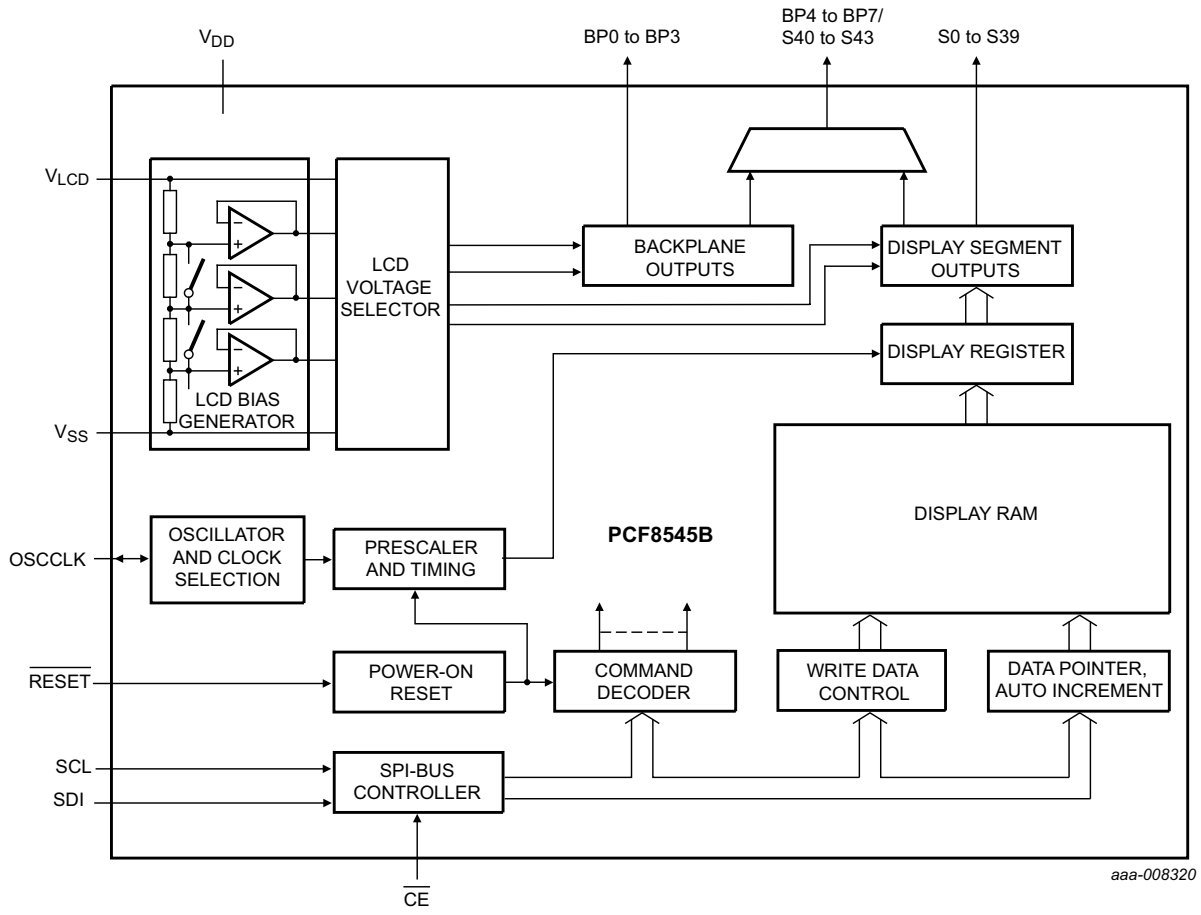
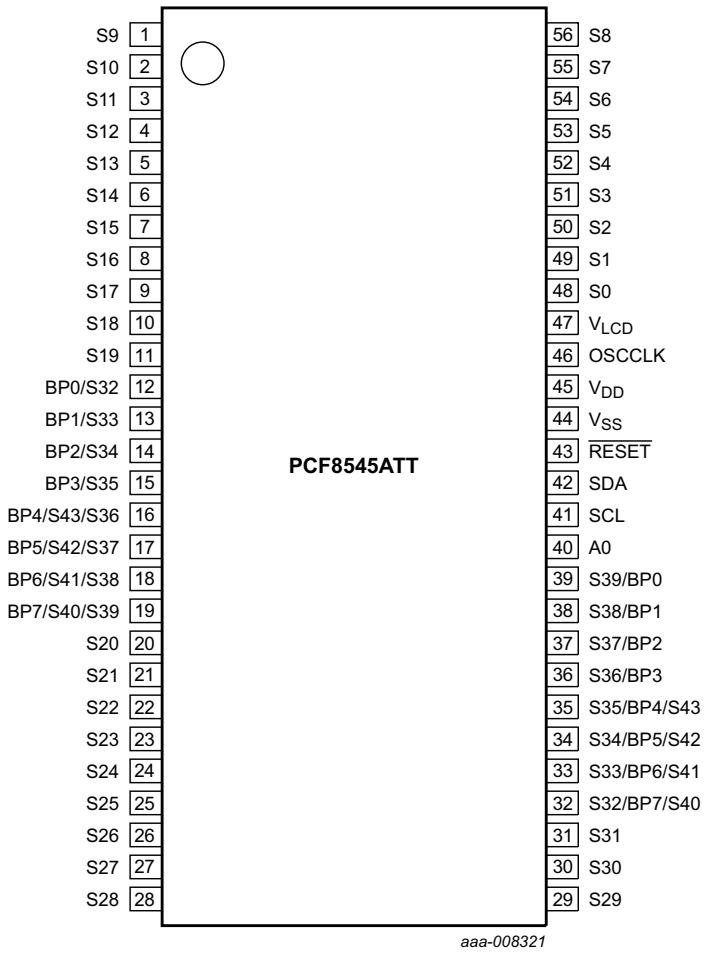


Fig 2. Block diagram of PCF8545B

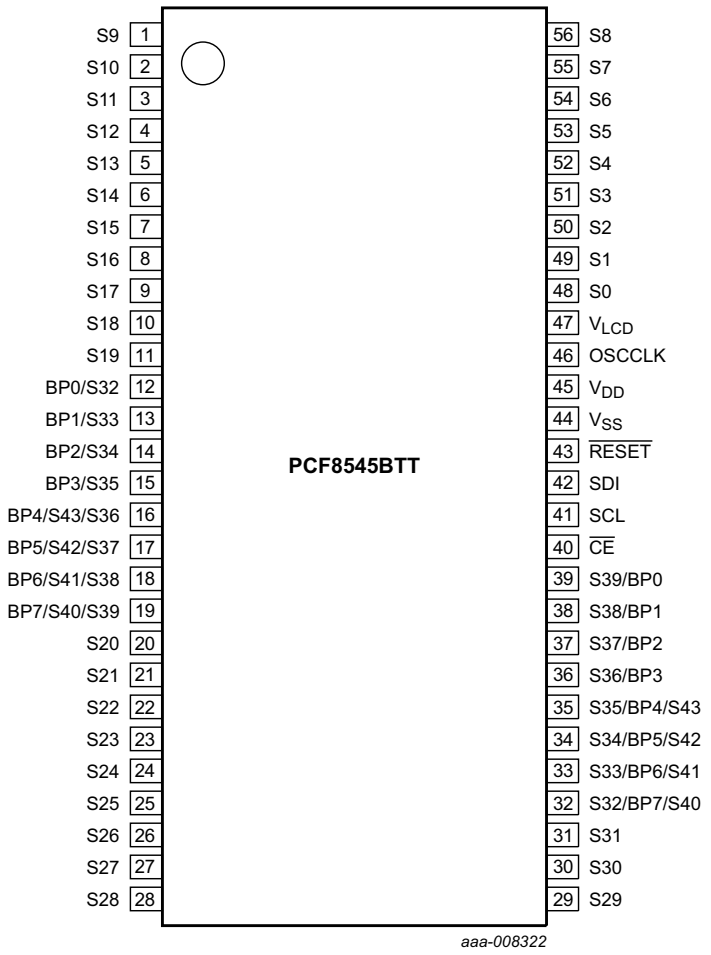
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 45.

Fig 3. Pin configuration for TSSOP56 (PCF8545ATT)



Top view. For mechanical details, see Figure 45.

Fig 4. Pin configuration for TSSOP56 (PCF8545BTT)

7.2 Pin description

Table 4. Pin description of PCF8545ATT and PCF8545BTT

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Pin	Symbol		Type	Description
1 to 11	S9 to S19		output	LCD segment
20 to 31	S20 to S31		output	LCD segment
43	$\overline{\text{RESET}}$		input	active LOW reset input
44	V_{SS}		supply	ground supply voltage
45	V_{DD}		supply	supply voltage
46	OSCCLK		input/output	external clock input/internal oscillator output
47	V_{LCD}[1]		supply	LCD supply voltage
48 to 56	S0 to S8		output	LCD segment
Pin layout depending on backplane swap configuration[2]				
	BPS = 0[3]	**BPS = 1**		
12	BP0	S32	output	LCD backplane/LCD segment
13	BP1	S33		
14	BP2	S34		
15	BP3	S35		
16	BP4/S43	S36		
17	BP5/S42	S37		
18	BP6/S41	S38		
19	BP7/S40	S39		
32	S32	BP7/S40		
33	S33	BP6/S41		
34	S34	BP5/S42		
35	S35	BP4/S43		
36	S36	BP3		
37	S37	BP2		
38	S38	BP1		
39	S39	BP0		
Pin layout depending on product and bus type				
	PCF8545ATT	**PCF8545BTT**		
40	A0		input	I^2C-bus slave address selection
		$\overline{\text{CE}}$	input	SPI-bus chip enable - active LOW
41	SCL		input	I^2C-bus serial clock
		SCL	input	SPI-bus serial clock
42	SDA		input/output	I^2C-bus serial data
		SDI	input	SPI-bus data input

[1] V_{LCD} must be equal to or greater than V_{DD}.

[2] Effect of backplane swapping is illustrated in Figure 5 on page 9.

[3] Bit BPS is explained in Section 8.1.3 on page 8.

8. Functional description

The PCF8545 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs. It can directly drive any multiplexed LCD containing up to eight backplanes and up to 44 segments.

8.1 Commands of PCF8545

The PCF8545 is controlled by 9 commands, which are defined in Table 5. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCF8545.

Table 5. Commands of PCF8545

Command name	Register selection RS[1:0][1]		Bits								Reference
			7	6	5	4	3	2	1	0	
initialize	0	0	0	0	0	1	0	1	1	0	Section 8.1.1
OTP-refresh	0	0	1	1	1	1	0	0	0	0	Section 8.1.2
mode-settings	0	0	0	1	0	1	BPS	INV	PD	E	Section 8.1.3
oscillator-control	0	0	0	0	0	1	1	EFR	COE	OSC	Section 8.1.4
set-MUX-mode	0	0	0	0	0	0	0	0	M[1:0]		Section 8.1.5
set-bias-mode	0	0	0	0	0	0	0	1	B[1:0]		Section 8.1.6
frame-frequency	0	0	0	0	1	FD[4:0]					Section 8.1.7
load-data-pointer	0	0	1	0	DP[5:0]						Section 8.1.8
write-RAM-data	0	1	D[7:0]								Section 8.1.9

[1] Information about control byte and register selection see Section 9.1 on page 36.

8.1.1 Command: initialize

This command generates a chip-wide reset. It has the same function as the $\overline{\text{RESET}}$ pin. Reset takes 1 ms to complete.

Table 6. Initialize - initialize command bit description

Bit	Symbol	Value	Description
7 to 0	-	00010110	fixed value

8.1.2 Command: OTP-refresh

During production of the device, each IC is calibrated to achieve the specified accuracy of the frame frequency. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. The device reads these cells every time the OTP-refresh command is sent. The OTP-refresh command has to be sent after a reset has been made and before the display is enabled.

This command will be completed after a maximum of 30 ms and requires either the internal or external clock to run. If the internal oscillator is not used, then a clock must be supplied to the OSCCLK pin. If the OTP-refresh instruction is sent and no clock is present, then the request is stored until a clock is available.

Remark: It is recommended not to enter power-down mode during the OTP refresh cycle.

Table 7. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
7 to 0	-	11110000	fixed value

8.1.3 Command: mode-settings

Table 8. Mode-settings - mode settings command bit description

Bit	Symbol	Value	Description
7 to 4	-	0101	fixed value
3	BPS		**backplane swapping**
		0[1]	backplane configuration 0
		1	backplane configuration 1
2	INV		**set inversion mode**
		0[1][2]	Driving scheme A: LCD line inversion mode
		1	Driving scheme B: LCD frame inversion mode
1	PD		**set power mode**
		1	power-down mode; backplane and segment outputs are connected to V_{SS} and the internal oscillator is switched off
		0[1]	power-up mode
0	E		**display switch**
		0[1]	display disabled; backplane and segment outputs are connected to V_{SS}
		1	display enabled

[1] Default value.

[2] See Section 8.1.3.2.

8.1.3.1 Backplane swapping

Backplane swapping can be configured with the BPS bit (see Table 8). It moves the location of the backplane and the associated segment outputs from one side of the PCF8545 to the other. Backplane swapping is sometimes desirable to aid with the routing of PCBs that do not use multiple layers.

The BPS bit has to be set to the required value before enabling the display. Failure to do so does not damage the PCF8545 or the display, however unexpected display content may appear.

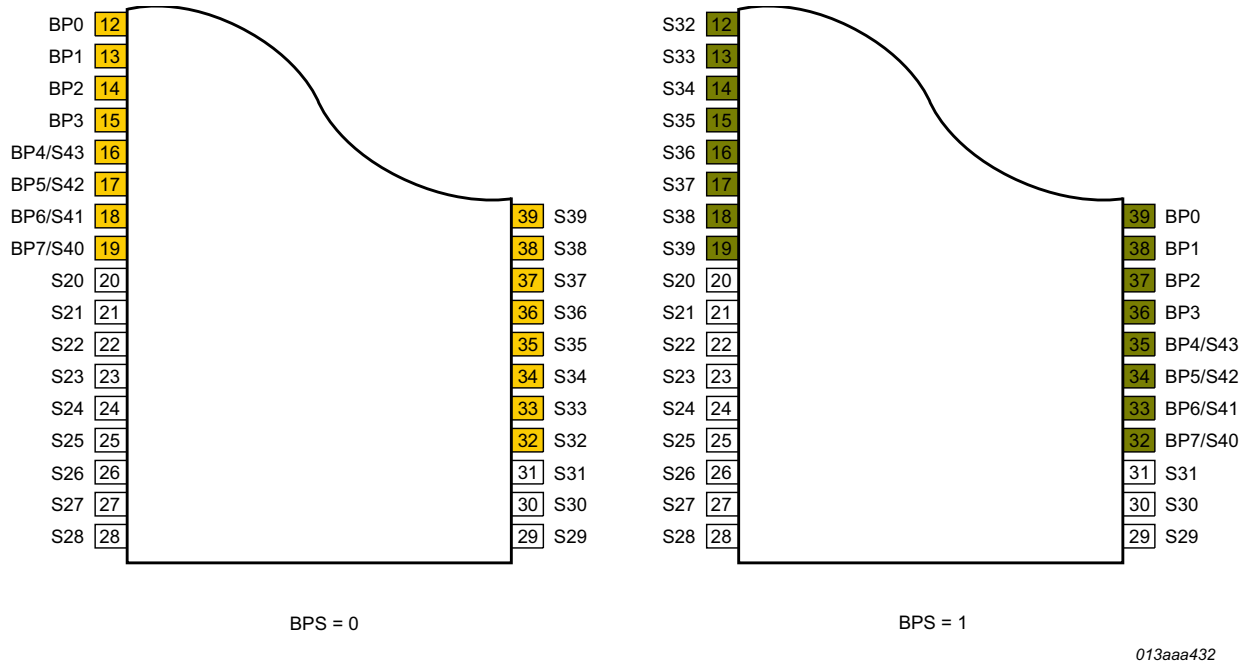


Fig 5. Effect of backplane swapping

8.1.3.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The DC offset of the voltage across the LCD is compensated over a certain period: line-wise in line inversion mode (driving scheme A) or frame-wise in frame inversion mode (driving scheme B). With the INV bit (see Table 8), the compensation mode can be switched.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption; therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined; however, since the switching frequency is reduced, there is possibility for flicker to occur.

The waveforms of Figure 14 on page 24 to Figure 17 on page 27 are showing line inversion mode. Figure 18 on page 28 shows an example of frame inversion.

8.1.3.3 Power-down mode

The power-down bit (PD) allows the PCF8545 to be put in a minimum power configuration. To avoid display artifacts, enter power-down only after the display has been switched off by setting bit E to logic 0. During power-down, the internal oscillator is switched off.

Table 9. Effect of the power-down bit (PD)

Effect on function	Mode settings	Effect of setting PD	
		0	1
backplane output	E = 1	normal function	V_{SS}
segment output	E = 1	normal function	V_{SS}
internal oscillator	OSC = 0, COE = 1	on	off
OSCCLK pin	OSC = 0, COE = 1	output of internal oscillator frequency	V_{DD}
OSCCLK pin	OSC = 1	input clock	clock input, can be logic 0, logic 1, or left floating

With the following sequence, the PCF8545 can be set to a state of minimum power consumption, called power-down mode.

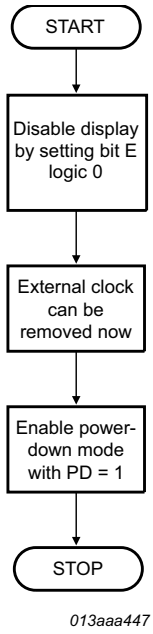


Fig 6. Recommended power-down sequence

Remarks:

- It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see Section 10). Otherwise it may cause unwanted display artifacts. If an uncontrolled removal of the supply happens, the PCF8545 does not get damaged.
- Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage is off, or the other way around. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

- A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. First disable the display and afterwards remove the clock signal.

8.1.3.4 Display enable

The display enable bit (E) is used to enable and disable the display. When the display is disabled, all LCD outputs go to V_{SS}. This function is implemented to ensure that no voltage can be induced on the LCD outputs as it may lead to unwanted displays of segments.

Recommended start-up sequences are found in Section 8.2.3

Remark: Display enable is not synchronized to an LCD frame boundary. Therefore using this function to flash a display for prolonged periods is not recommended due to the possible build-up of DC voltages on the display.

8.1.4 Command: oscillator-control

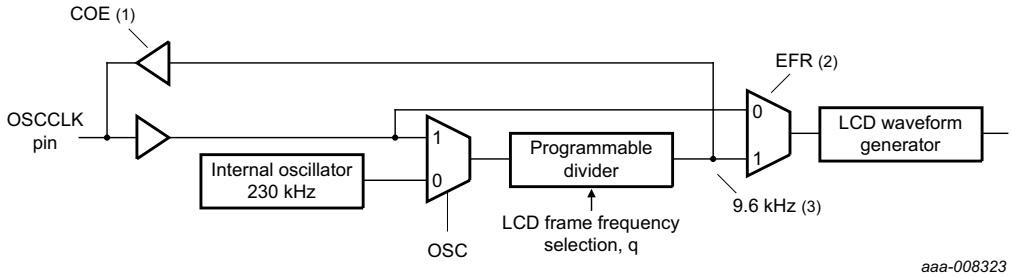
The oscillator-control command switches between internal and external oscillator and enables or disables the pin OSCCLK. It is also defines the external frequency.

Table 10. Oscillator-control - oscillator control command bit description

Bit	Symbol	Value	Description
7 to 3	-	00011	fixed value
2	EFR		**external clock frequency** applied on pin OSCCLK
		0[1]	9.6 kHz
		1	230 kHz
1	COE		**clock output enable for pin OSCCLK**
		0[1]	clock signal not available on pin OSCCLK; pin OSCCLK is in 3-state
		1	clock signal available on pin OSCCLK
0	OSC		**oscillator source**
		0[1]	internal oscillator running
		1	external oscillator used; pin OSCCLK becomes an input; used in combination with EFR to determine input frequency

[1] Default value.

The bits OSC, COE, and EFR control the source and frequency of the clock used to generate the LCD signals (see Figure 7). Valid combinations are shown in Table 11.



(1) Can only be used with the internal oscillator (OSC = 0).

(2) Can only be used with an external oscillator (OSC = 1).

(3) Nominal value for divide factor q is 24; source clock is 230 kHz (see Section 8.1.7).

Fig 7. Oscillator selection

Table 11. Valid combinations of bits OSC, EFR, and COE

OSC	COE	EFR	OSCCLK pin	Clock source
0	0	not used	inactive; may be left floating	internal oscillator used
0	1	not used	output of internal oscillator frequency (prescaler)	internal oscillator used
1	not used	0	9.6 kHz input	OSCCLK pin
1	not used	1	230 kHz input	OSCCLK pin

Table 12. Typical use of bits OSC, EFR, and COE

Usage	OSC	COE	EFR
LCD with internal oscillator	0	0	not used
LCD with external oscillator (230 kHz)	1	not used	1
LCD with external oscillator (9.6 kHz)	1	not used	0

8.1.4.1 Oscillator

The system is designed to operate from a 9.6 kHz or a 230 kHz clock. This clock can be sourced internally or externally. The internal logic and LCD drive signals of the PCF8545 are timed either by the internal oscillator or from the clock externally supplied.

Internal clock: When the internal oscillator is used, all LCD signals are generated from it. The oscillator runs at nominal 230 kHz. The relationship between this frequency and the LCD frame frequency is detailed in Section 8.1.7. Control over the internal oscillator is made with the OSC bit (see Section 8.1.4).

It is possible to make the internal oscillator signal available on pin OSCCLK by using the oscillator-control command (see Table 10) and configuring the clock output enable (COE) bit. If not required, the pin OSCCLK should be left open or connected to V_{SS}. At power-on the signal at pin OSCCLK is disabled and pin OSCCLK is in 3-state.

Clock output is only valid when using the internal oscillator. The signal appears on the OSCCLK pin.

An intermediate clock frequency is available at the OSCCLK pin. The duty cycle of this clock varies with the chosen divide ratio.

Table 13. OSCCLK pin state depending on configuration

PD	OSC	COE	EFR	OSCCLK pin[1]
power-down	n.a.	off	n.a.	3-state[2]
power-down	n.a.	on	n.a.	V_{DD}
power-up	internal oscillator	off	n.a.	3-state
		on	n.a.	9.6 kHz output[3]
	external oscillator	n.a.	9.6 kHz	9.6 kHz input
			230 kHz	230 kHz input

[1] When $\overline{\text{RESET}}$ is active, the pin OSCCLK is in 3-state.

[2] In this state, an external clock may be applied, but it is not a requirement.

[3] 9.6 kHz is the nominal frequency with q = 24, see Table 14.

External clock: In applications where an external clock must be applied to the PCF8545, bit OSC (see Table 10) has to be set logic 1. In this case pin OSCCLK becomes an input.

The OSCCLK signal must switch between the V_{SS} and the V_{DD} voltage supplied to the chip.

The EFR bit determines the external clock frequency (230 kHz or 9.6 kHz). The clock frequency ($f_{clk(ext)}$) in turn determines the LCD frame frequency, see Table 14.

Remark: If an external clock is used, then this clock signal must always be supplied to the device when the display is on. Removing the clock may freeze the LCD in a DC state which damages the LCD material.

8.1.4.2 Timing and frame frequency

The timing of the PCF8545 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 14). The frame frequency is a fixed division of the internal clock or of the frequency applied to pin OSCCLK when an external clock is used.

Table 14. LCD frame frequencies

Frame frequency	Typical external frequency (Hz)	Nominal frame frequency (Hz)	EFR bit	Value of q[1]
$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48}$	9600	200	0	-
$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q}$	230000	200	1	24

[1] Other values of the frame frequency prescaler see Table 18.

When the internal clock is used, or an external clock with EFR = 1, the LCD frame frequency can be programmed by software in steps of approximately 10 Hz in the range of 60 Hz to 300 Hz (see Table 18). Furthermore the internal oscillator is factory calibrated, see Table 34 on page 50.

8.1.5 Command: set-MUX-mode

The multiplex drive mode is configured with the bits described in Table 15.

Table 15. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000000	fixed value
1 to 0	M[1:0]	00[1], 01	1:8 multiplex drive mode; eight backplanes
		10	1:6 multiplex drive mode; 6 backplanes
		11	1:4 multiplex drive mode; 4 backplanes

[1] Default value.

8.1.6 Command: set-bias-mode

The set-bias-mode command allows setting the bias level.

Table 16. Set-bias-mode - set bias mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000001	fixed value
1 to 0	B[1:0]	00[1]. 01	1/4 bias
		11	1/3 bias
		10	1/2 bias

[1] Default value.

8.1.7 Command: frame-frequency

With the frame-frequency command, the frame frequency for the display can be configured. The clock frequency determines the frame frequency.

Table 17. Frame-frequency - frame frequency and output clock frequency command bit description

Bit	Symbol	Value	Description
7 to 5	-	001	fixed value
4 to 0	FD[4:0]	see Table 18	frequency prescaler

When using an **external clock** it can be either a 230 kHz or a 9.6 kHz clock signal. The EFR bit (see Table 10) has to be set according to the external clock frequency.

When EFR is set to 9.6 kHz, then the LCD frame frequency is calculated with Equation 1:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48} \quad (1)$$

When EFR is set to 230 kHz, then the LCD frame frequency is calculated with Equation 2:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q} \quad (2)$$

where q is the frequency divide factor (see Table 18).

Remark: $f_{clk(ext)}$ is the external input clock frequency to pin OSCCLK.

When the **internal oscillator** is used, the intermediate frequency may be output on the OSCCLK pin. Its frequency is given in Table 18.

Table 18. Frame frequency prescaler values for 230 kHz clock operation

FD[4:0]	Nominal LCD frame frequency (Hz)[1]	Divide factor, q	Intermediate clock frequency (Hz)
00000	59.9	80	2875
00001	70.5	68	3382
00010	79.9	60	3833
00011	90.4	53	4340
00100	99.8	48	4792
00101	108.9	44	5227
00110	119.8	40	5750
00111	129.5	37	6216
01000	140.9	34	6765
01001	149.7	32	7188
01010	159.7	30	7667
01011	171.1	28	8214
01100	177.5	27	8519
01101	191.7	25	9200
01110[2]	199.7	24	9583
01111	208.3	23	10000
10000	217.8	22	10455
10001	228.3	21	10952
10010	239.6	20	11500
10011	252.2	19	12105
10100	266.2	18	12778
10101	281.9	17	13529
10110	299.5	16	14375
10111 to 11111	not used		

[1] Nominal frame frequency calculated for the default clock frequency of 230 kHz.

[2] Default value.

8.1.8 Command: load-data-pointer

The load-data-pointer command defines the start address of the display RAM. The data pointer is auto incremented after each RAM write. The size of the display RAM is dependent on the current multiplex drive mode setting, see Table 19.

Table 19. Load-data-pointer - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 6	-	10	fixed value
Multiplex drive mode 1:8			
5 to 0	DP[5:0]	000000[1] to 100111	6-bit binary value of 0 to 39
Multiplex drive mode 1:6			
5 to 0	DP[5:0]	000000[1] to 101001	6-bit binary value of 0 to 41
Multiplex drive mode 1:4			
5 to 0	DP[5:0]	000000[1] to 101011	6-bit binary value of 0 to 43

[1] Default value.

Remark: Data pointer values outside of the valid range are ignored and no RAM content is transferred until a valid data pointer value is set.

Filling of the display RAM is described in Section 8.9.

8.1.9 Command: write-RAM-data

This command initiates the transfer of data to the display RAM. Data is written into the address defined by the load-data-pointer command. RAM filling is described in Section 8.9.

Table 20. Write-RAM-data - write RAM data command bit description[1]

Bit	Symbol	Value	Description
7 to 0	D[7:0]	00000000 to 11111111	writing data byte-wise to RAM

[1] For this command to be effective bit RS[1:0] of the control byte has to be set logic 01, see Table 25 on page 36.

8.2 Start-up and shut-down

8.2.1 Reset and Power-On Reset (POR)

After a reset and at power-on the PCF8545 resets to starting conditions as follows:

1. The display is disabled.
2. All backplane outputs are set to V_{SS}.
3. All segment outputs are set to V_{SS}.
4. Selected drive mode is: 1:8 with $^1/_4$ bias.
5. The data pointers are cleared (set logic 0).
6. RAM data is not initialized. Its content can be considered to be random.
7. The internal oscillator is running; no clock signal is available on pin OSCCLK; pin OSCCLK is in 3-state.

The reset state is as shown in Table 21.

Table 21. Reset state

Reset state of configurable bits shown in the command table format for clarity.

Associated command	Bits							
	7	6	5	4	3	2	1	0
mode-settings	-	-	-	-	BPS = 0	INV = 0	PD = 0	E = 0
oscillator-control	-	-	-	-	-	EFR = 0	COE = 0	OSC = 0
set-MUX-mode	-	-	-	-	-	-	M[1:0] = 00	
set-bias-mode	-	-	-	-	-	-	B[1:0] = 00	
frame-frequency	-	-	-	FD[4:0] = 01110				
load-data-pointer	-	-	DP[5:0] = 000000					

The first command sent to the device after the power-on event must be the initialize command (see Section 8.1.1).

After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined state by writing meaningful content (for example, a graphic) otherwise unwanted display artifacts may appear on the display.

8.2.2 $\overline{\text{RESET}}$ pin function

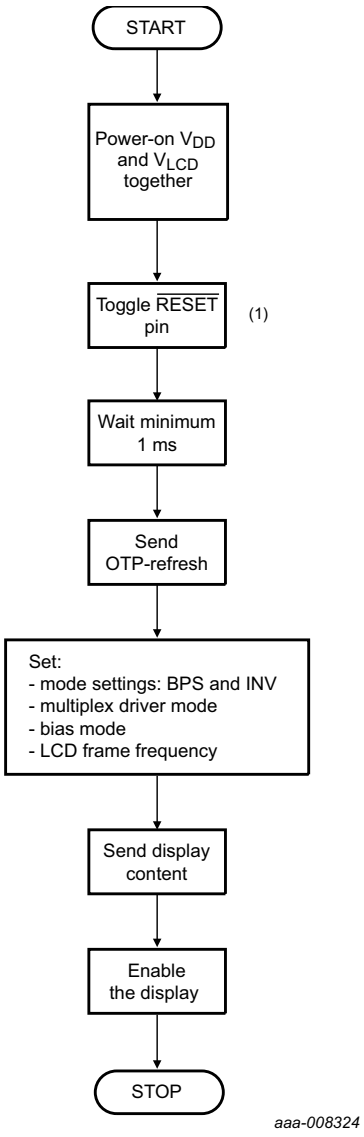
The $\overline{\text{RESET}}$ pin of the PCF8545 sets all the registers to their default state. The reset state is given in Table 21. The RAM contents remains unchanged. After the reset signal is removed, the PCF8545 will behave in the same manner as after Power-On Reset (POR). See Section 8.2.1 for details.

8.2.3 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.

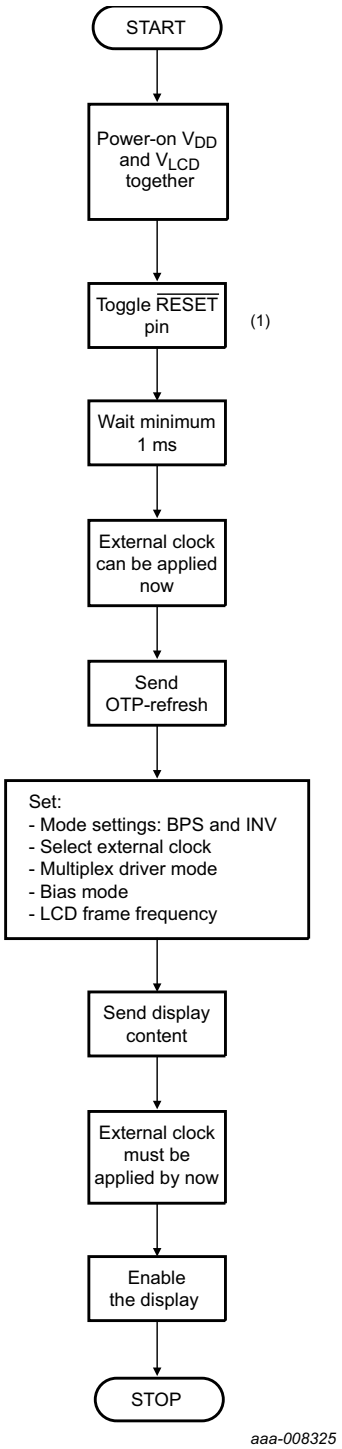
In general, the sequence should always be:

1. Power-on the device,
2. set the display and functional modes,
3. fill the display memory and then
4. turn on the display.



(1) Alternatively, it is possible to send the initialize command.

Fig 8. Recommended start-up sequence when using the internal oscillator



(1) Alternatively, it is possible to send the initialize command.

Fig 9. Recommended start-up sequence when using an external clock signal

8.3 Possible display configurations

The PCF8545 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 10). It can drive multiplexed LCD with 4, 6, or 8 backplanes and up to 44 segments.

The display configurations possible with the PCF8545 depend on the required number of active backplane outputs. A selection of possible display configurations is given in Table 22.

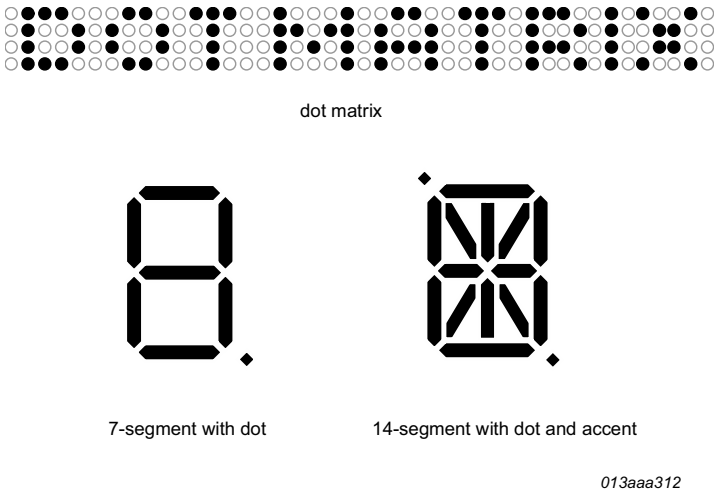


Fig 10. Example of displays suitable for PCF8545

Table 22. Selection of display configurations

Number of			Digits/Characters		Dot matrix/ Elements
Backplanes	Segments	Icons	7 segment[1]	14 segment[2]	
8	40	320	40	20	320
6	42	252	31	15	252
4	44	176	22	11	176

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

All of the display configurations in Table 22 can be implemented in the typical systems shown in Figure 11 and Figure 12.

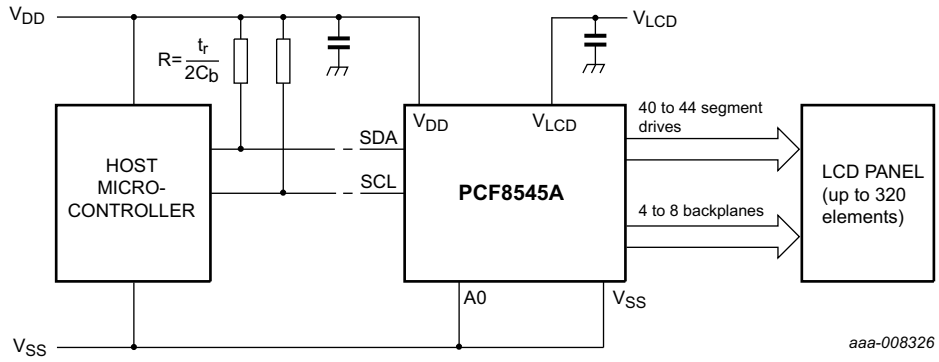


Fig 11. Typical system configuration for the I²C-bus

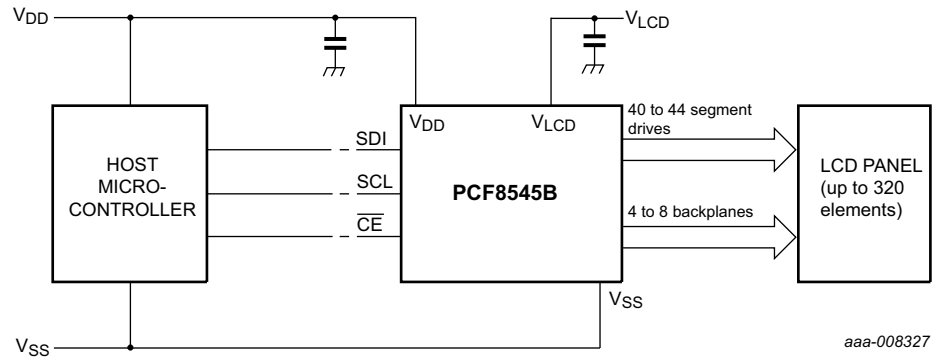


Fig 12. Typical system configuration for the SPI-bus

The host microcontroller maintains the two line I²C-bus or a three line SPI-bus communication channel with the PCF8545. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, V_{LCD}) and the LCD panel selected for the application.

The minimum recommended values for external capacitors on V_{DD} and V_{LCD} are 100 nF respectively. Decoupling of V_{LCD} helps to reduce display artifacts. The decoupling capacitors should be placed close to the IC with short connections to the respective supply pin and V_{SS}.

8.4 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the set-bias-mode command (see Table 16) and the set-MUX-mode command (see Table 15).

Fractional LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 23.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 23. Preferred LCD drive modes: summary of characteristics

LCD multiplex drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ [1]	V_{LCD}[2]
	Backplanes	Levels					
1:4 [3]	4	3	½	0.433	0.661	1.527	$2.309V_{off(RMS)}$
1:4	4	4	⅓	0.333	0.577	1.732	$3.0V_{off(RMS)}$
1:4 [3]	4	5	¼	0.331	0.545	1.646	$3.024V_{off(RMS)}$
1:6 [3]	6	3	½	0.456	0.612	1.341	$2.191V_{off(RMS)}$
1:6	6	4	⅓	0.333	0.509	1.527	$3.0V_{off(RMS)}$
1:6	6	5	¼	0.306	0.467	1.527	$3.266V_{off(RMS)}$
1:8 [3]	8	3	½	0.467	0.586	1.254	$2.138V_{off(RMS)}$
1:8 [3]	8	4	⅓	0.333	0.471	1.414	$3.0V_{off(RMS)}$
1:8	8	5	¼	0.293	0.424	1.447	$3.411V_{off(RMS)}$

[1] Determined from Equation 5.

[2] Determined from Equation 4.

[3] In these examples, the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a reduction of the LCD voltage V_{LCD}.

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

a = 3 for ¼ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (3)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 4 for 1:4 multiplex drive

n = 6 for 1:6 multiplex drive

n = 8 for 1:8 multiplex drive

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \quad (4)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 5:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (5)$$

V_{LCD} is sometimes referred to as the LCD operating voltage.

8.4.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel gets switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 13. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (6)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (7)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 3 to Equation 5) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

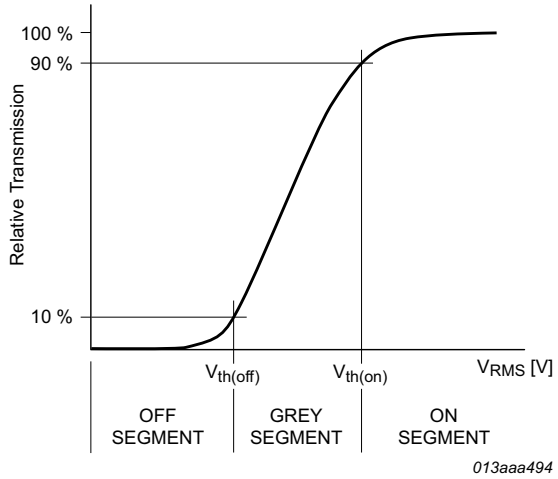
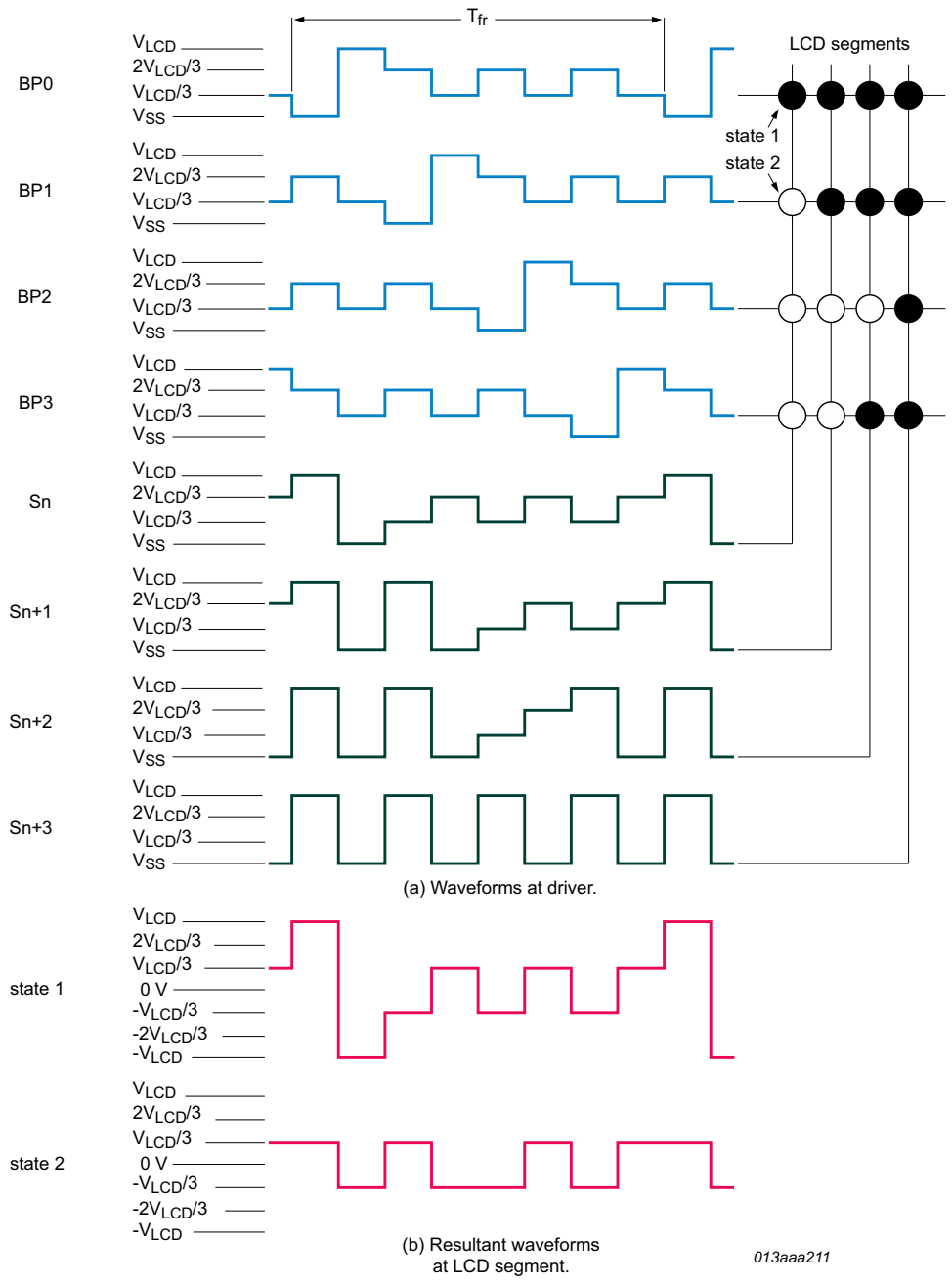


Fig 13. Electro-optical characteristic: relative transmission curve of the liquid

8.5 LCD drive mode waveforms

8.5.1 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 14. This drawing is also showing the case of line inversion (see Section 8.1.3.2).



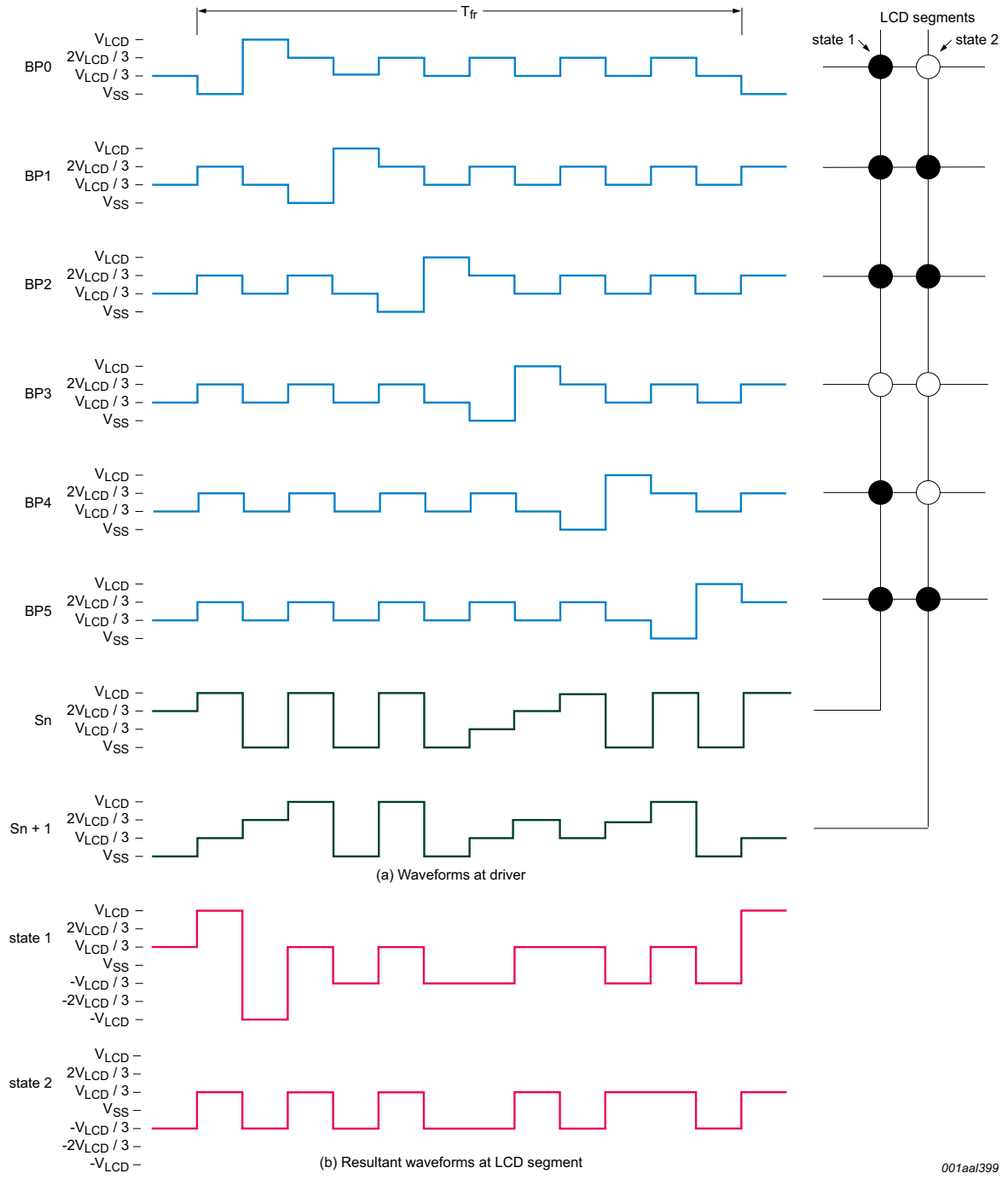
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.577V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 14. Waveforms for the 1:4 multiplex drive mode with ⅓ bias and line inversion

8.5.2 1:6 Multiplex drive mode

When six backplanes are provided in the LCD, the 1:6 multiplex drive mode applies. The PCF8545 allows use of ⅓ bias or ¼ bias in this mode as shown in Figure 15 and Figure 16. These waveforms are drawn for the case of line inversion (see Section 8.1.3.2).



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.509V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 15. Waveforms for 1:6 multiplex drive mode with bias ⅓ and line inversion