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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PCF8553

40 × 4 LCD segment driver

Rev. 3 — 27 March 2015 Product data sheet

1. General description

PCF8553 is an ultra low-power LCD segment driver with 4 backplane- and 40 segment-driver outputs, with either an I^2C- or an SPI-bus interface. It comprises an internal oscillator, bias generation, instruction decoding, and display controller.

For a selection of NXP LCD segment drivers, see Table 24 on page 45.

2. Features and benefits

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with buffers
- 40 segment drives:
  - Up to 20 7-segment numeric characters
  - Up to 10 14-segment alphanumeric characters
  - Any graphics of up to 160 segments/elements
- Auto-incrementing display data and instruction loading
- Versatile blinking modes
- Independent supplies of V_{LCD} and V_{DD}
- Power supply ranges:
  - 1.8 V to 5.5 V for V_{LCD}
  - 1.8 V to 5.5 V for V_{DD}
- Ultra low-power consumption
- 400 kHz I^2C-bus interface
- 5 MHz SPI-bus interface
- Internally generated or externally supplied clock signal

3. Applications

- Metering equipment
- Small appliances
- Consumer healthcare devices
- Battery operated devices
- Measuring equipment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8553DTT	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF8553DTT/A	PCF8553DTT/AJ	935304762118	tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF8553DTT/A	PCF8553D

6. Block diagram

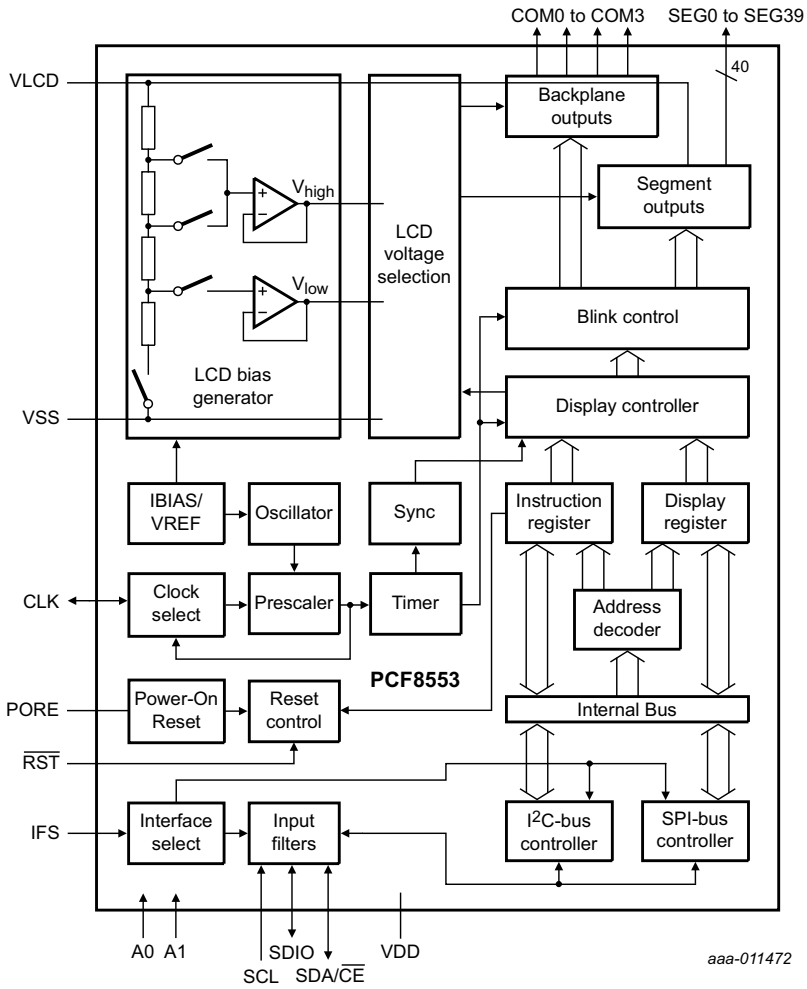


Fig 1. Block diagram of PCF8553

7. Pinning information

7.1 Pinning

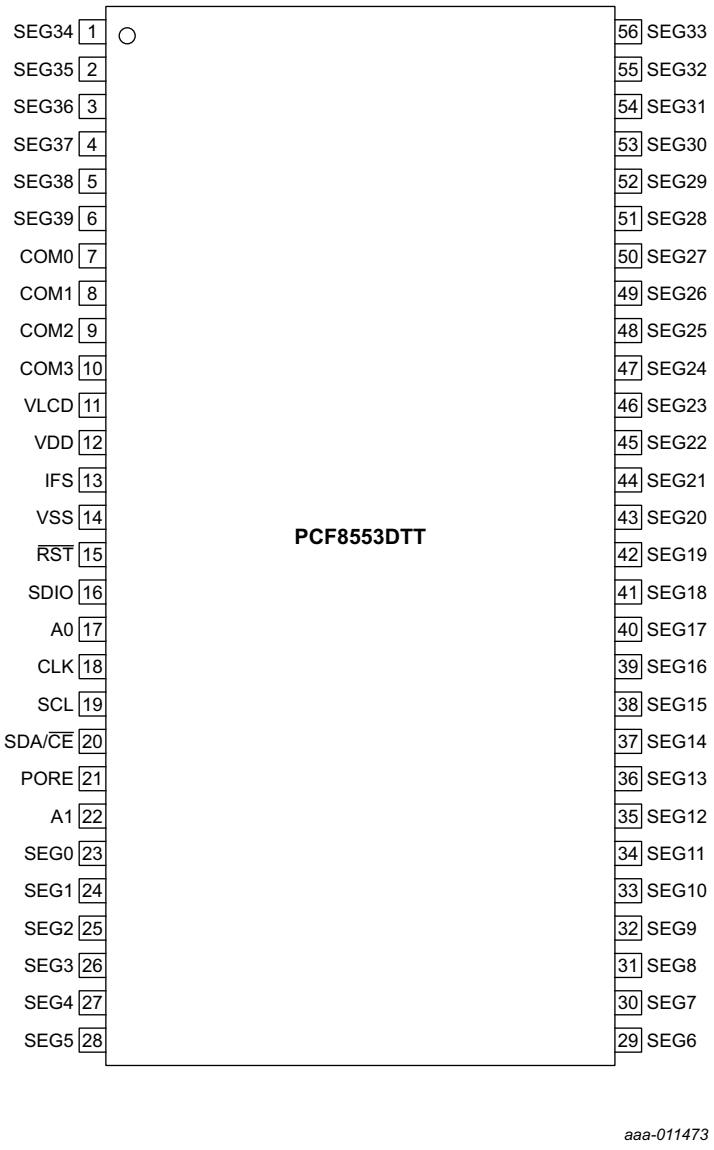


Fig 2. Pin configuration of PCF8553DTT (TSSOP56)

7.2 Pin description

Table 4. Pin description of PCF8553DTT (TSSOP56)

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description	
Backplane and segment outputs				
SEG34 to SEG39	1 to 6	output	LCD segments	
SEG0 to SEG33	23 to 56			
COM0 to COM3	7 to 10	output	LCD backplanes	
Supply pins				
VLCD	11	supply	LCD supply voltage	
VDD	12	supply	supply voltage	
VSS	14	supply	ground supply	
Clock and control pins				
$\overline{RST}$	15	input	reset input, active LOW	
PORE[1]	21	input	Power-On Reset (POR) enable • connect to V_{DD} for enabling POR • connect to V_{SS} (or leave open) for disabling POR	
CLK	18	input/output	internal oscillator output, external oscillator input • must be left open if unused	
Bus-related pins			**I²C-bus**	**SPI-bus**
IFS[1]	13	input	interface selector input	
			• connect to V_{SS} (or leave open)	• connect to V_{DD}
SDIO	16	input/output	unused	serial data input/output
A0[1]	17	input	hardware device address selection; • connect to V_{SS} (or leave open) for logic 0 • connect to V_{DD} for logic 1	unused
A1[1]	22	input		
SCL	19	input	serial clock input	serial clock input
SDA/$\overline{CE}$	20	input/output	serial data output	chip enable input, active LOW

[1] A series resistance between V_{DD} and the pin must not exceed 1 kΩ to ensure proper functionality, see Section 16.3.

8. Functional description

8.1 Registers of the PCF8553

The registers of the PCF8553 are arranged in bytes with 8 bit, addressed by an address pointer. Table 5 depicts the layout.

Table 5. Registers of the PCF8553

Bits labeled as 0 must always be written with logic 0.

Register name	Address	Bits								Reference
	AP[4:0]	7	6	5	4	3	2	1	0	
Command registers										
Software_reset	00h	SR[7:0]								Table 9
Device_ctrl	01h	0	0	0	0	FF[1:0]		OSC	COE	Table 6
Display_ctrl_1	02h	0	0	0	BOOST	MUX[1:0]		B	DE	Table 7
Display_ctrl_2	03h	0	0	0	0	0	BL[1:0]		INV	Table 8
Display data registers[1]										
COM0	04h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	Table 10
	05h	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	
	06h	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16	
	07h	SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24	
	08h	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	
COM1	09h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	:	:	:	:	:	:	:	:	:	
	0Dh	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	
COM2	0Eh	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	:	:	:	:	:	:	:	:	:	
	12h	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	
COM3	13h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	:	:	:	:	:	:	:	:	:	
	17h	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	

[1] See Table 10.

For writing to the registers, send the address byte first, then write the data to the register (see Section 11.1.4 and Section 11.2.1). The address byte works as an address pointer. For the succeeding registers, the address pointer is automatically incremented by 1 (see Figure 3) and all following data are written into these register addresses. After register 17h, the auto-incrementing will stop and data are ignored.

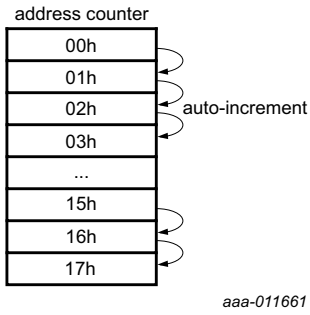


Fig 3. Address counter incrementing

8.2 Command registers of the PCF8553

8.2.1 Command: Device_ctrl

The Device_ctrl command sets the device into a defined state. It should be executed before enabling the display (see bit DE in Table 7).

Table 6. Device_ctrl - device control command register (address 01h) bit description

Bit	Symbol	Value	Description
7 to 4	-	0000	default value
3 to 2	FF[1:0]		**frame frequency selection**
		00	f_{fr} = 32 Hz
		01[1]	f_{fr} = 64 Hz
		10	f_{fr} = 96 Hz
		11	f_{fr} = 128 Hz
1	OSC		**internal oscillator control**
		0[1]	enabled
		1	disabled
0	COE		**clock output enable**
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

8.2.1.1 Internal oscillator and clock output

Bit OSC enables or disables the internal oscillator. When the internal oscillator is used, bit COE allows making the clock signal available on pin CLK. If this is not intended, pin CLK should be left open. The design ensures that the duty cycle of the clock output is 50 : 50 (% HIGH-level time : % LOW-level time).

In applications where an external clock has to be applied to the PCF8553, bit OSC must be set logic 1 and COE logic 0. In this case pin CLK becomes an input.

In power-down mode (see Section 8.3.1)

- if pin CLK is configured as an output, there is no signal on CLK
- if pin CLK is configured as an input, the signal on CLK can be removed.

Remark: A clock signal must always be supplied to the device if the display is enabled (see bit DE in Table 7 on page 8). Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

8.2.2 Command: Display_ctrl_1

The Display_ctrl_1 command allows configuring the basic display set-up.

Table 7. Display_ctrl_1 - display control command 1 register (address 02h) bit description

Bit	Symbol	Value	Description
7 to 5	-	000	default value
4	BOOST		**large display mode support**
		0[1]	standard power drive scheme
		1	enhanced power drive scheme for higher display loads
3 to 2	MUX[1:0]		**multiplex drive mode selection**
		00[1]	1:4 multiplex drive mode; COM0 to COM3 (n_{MUX} = 4)
		01	1:3 multiplex drive mode; COM0 to COM2 (n_{MUX} = 3)
		10	1:2 multiplex drive mode; COM0 and COM1 (n_{MUX} = 2)
		11	static drive mode; COM0 (n_{MUX} = 1)
1	B[2]		**bias mode selection**
		0[1]	⅓ bias (a_{bias} = 2)
		1	½ bias (a_{bias} = 1)
0	DE		**display enable**[3]
		0[1]	display disabled; device is in power-down mode
		1	display enabled; device is in power-on mode

[1] Default value.

[2] Not applicable for static drive mode.

[3] See Section 8.3.1.

8.2.2.1 Enhanced power drive mode

By setting the BOOST bit to logic 1, the driving capability of the display signals is increased to cope with large displays with a higher effective capacitance. Setting this bit increases the current consumption on V_{LCD}.

8.2.2.2 Multiplex drive mode

MUX[1:0] sets the multiplex driving scheme and the associated backplane drive signals, which are active. For further details, see Section 9.2 on page 16.

8.2.3 Command: Display_ctrl_2

Table 8. Display_ctrl_2 - display control command 2 register (address 03h) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	default value
2 to 1	BL[1:0]		**blink control**
		00[1]	blinking off
		01	blinking on, f_{blink} = 0.5 Hz
		10	blinking on, f_{blink} = 1 Hz
		11	blinking on, f_{blink} = 2 Hz
0	INV		**inversion mode selection**
		0[1]	line inversion (driving scheme A)
		1	frame inversion (driving scheme B)

[1] Default value.

8.2.3.1 Blinking

The whole display blinks at frequencies selected by the blink control bits BL[1:0], see Table 8. The blink frequencies are derived from the clock frequency. During the blank-out phase of the blinking period, the display is turned off.

If an external clock with frequency $f_{clk(ext)}$ is used, the blinking frequency is determined by Equation 1. For notation, see Section 9.2.

$$f_{blink(eff)} = \frac{2 \times n_{MUX} \times f_{fr} \times f_{blink}}{f_{clk(ext)}} \quad (1)$$

8.2.3.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The waveforms used to drive LCD inherently produce a DC voltage across the display cell. The PCF8553 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the INV bit.

8.3 Starting and resetting the PCF8553

If the internal Power-On Reset (POR) is enabled by connecting pin PORE to V_{DD}, the chip resets automatically when V_{DD} rises above the minimum supply voltage. No further action is required.

If the internal POR is disabled by connecting pin PORE to V_{SS}, the chip must be reset by driving the $\overline{RST}$ pin to logic 0 for at least 10 μs, see Figure 4.

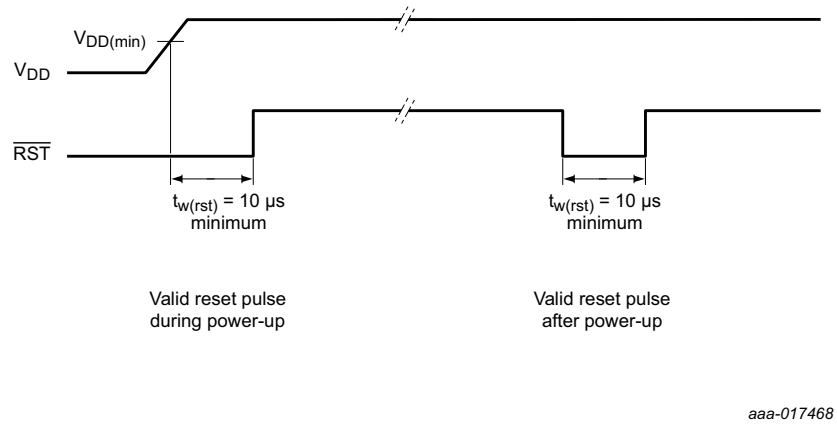


Fig 4. Reset pulse timing

Alternatively a software reset can be applied (see Section 8.3.4).

Following a reset, the register 00h has to be rewritten with 0h by the next command byte or the address pointer AP[4:0] has to be set to the required address after a new START procedure.

8.3.1 Power-down mode

After a reset, the PCF8553 remains in power-down mode. In power-down mode the oscillator is switched off and there is no output on pin CLK. The register settings remain unchanged and the bus remains active. To enable the PCF8553, bit DE (command Display_ctrl_1, see Table 7 on page 8) must be set to logic 1.

8.3.2 Power-On Reset (POR)

If pin PORE is connected to V_{DD}, the PCF8553 comprises an internal POR, which puts the device into the following starting conditions:

- All backplane and segment outputs are set to V_{SS}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- The address pointer is cleared (set to logic 0)
- The display and the internal oscillator are disabled
- The display registers are set to logic 0

Remark: The internal POR can be disabled by connecting pin PORE to V_{SS}. In this case, the internal registers are not defined and require a hardware reset according to Section 8.3.3 or a software reset, see Section 8.3.4.

8.3.3 Hardware reset: $\overline{\text{RST}}$ pin

At power-on the PCF8553 can be reset to the following starting conditions by pulling pin $\overline{\text{RST}}$ low:

- All backplane and segment outputs are set to V_{SS}
- The selected drive mode is: 1:4 multiplex with $^1/_3$ bias
- Blinking is switched off
- The bus interface is initialized
- The address pointer is cleared (set to logic 0)
- The display and the internal oscillator are disabled
- The display registers are set to logic 0

Remark: The hardware reset overrides the POR see Section 8.3.2.

8.3.4 Command: Software_reset

The internal registers including the display registers and the address pointer (set to logic 0) of the device are reset by the Software_reset command.

Table 9. Software_reset - software reset command register (address 00h) bit description

Bit	Symbol	Value	Description
7 to 0	SR[7:0]		**software reset**
		00000000[1]	no reset
		00101100	software reset

[1] Default value.

8.4 Display data register mapping

The example in Table 10 and Figure 5 illustrates the segment and backplane mapping of the display in relation to the display RAM.

For example, in 1:4 multiplex drive mode, the backplanes are served by signals COM0 to COM3 and the segments are driven by signals SEG0 to SEG39. Contents of addresses 04h to 08h are allocated to the first row (COM0) starting with the LSB driving the leftmost element and moving forward to the right with increasing bit position. If a bit is logic 0, the element is off, if it is logic 1 the element is turned on. All register content is LSB to MSB left to right. Addresses 09h to 0Dh serve COM1 signals, addresses 0Eh to 12h serve COM2 signals, and addresses 13h to 17h serve COM3 signals.

For displays with fewer segments/elements the unused bits are ignored.

Table 10. Register to segment and backplane mapping

Backplanes[1]	Segments									
	SEG0 to SEG7		SEG8 to SEG15		SEG16 to SEG23		SEG24 to SEG31		SEG32 to SEG39	
	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB
1:4 multiplex drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	
COM1	content of 09h		content of 0Ah		content of 0Bh		content of 0Ch		content of 0Dh	
COM2	content of 0Eh		content of 0Fh		content of 10h		content of 11h		content of 12h	
COM3	content of 13h		content of 14h		content of 15h		content of 16h		content of 17h	
1:3 multiplex drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	
COM1	content of 09h		content of 0Ah		content of 0Bh		content of 0Ch		content of 0Dh	
COM2	content of 0Eh		content of 0Fh		content of 10h		content of 11h		content of 12h	
1:2 multiplex drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	
COM1	content of 09h		content of 0Ah		content of 0Bh		content of 0Ch		content of 0Dh	
static drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	

[1] See also Section 9.3.1 on page 24.

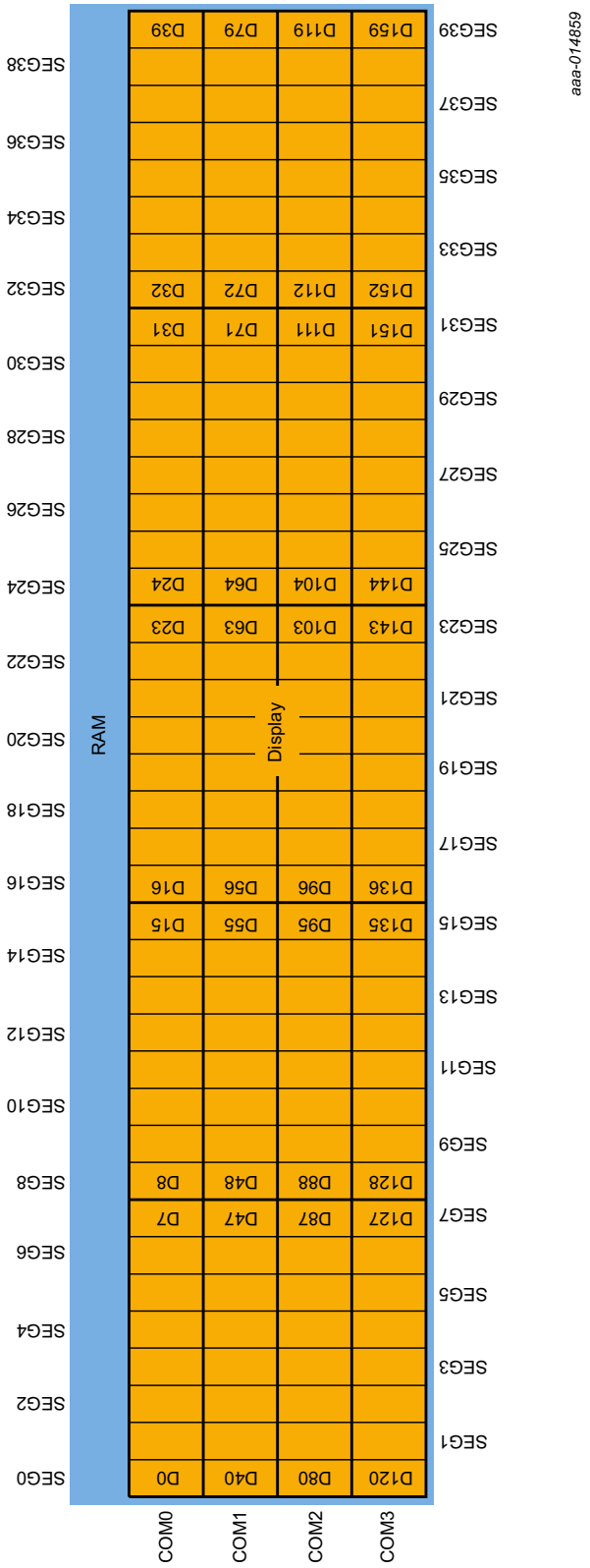


Fig 5. Display RAM organization bitmap for MUX 1:4

9. Possible display configurations

The possible display configurations of the PCF8553 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 11. All of these configurations can be implemented in the typical systems shown in Figure 7 or Figure 8.

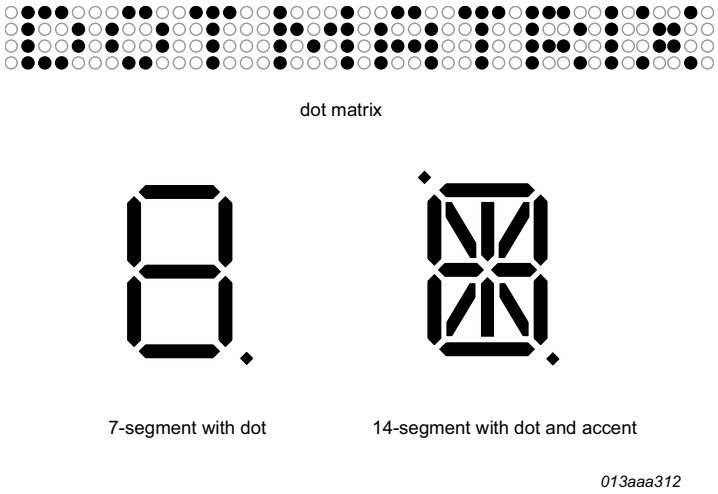


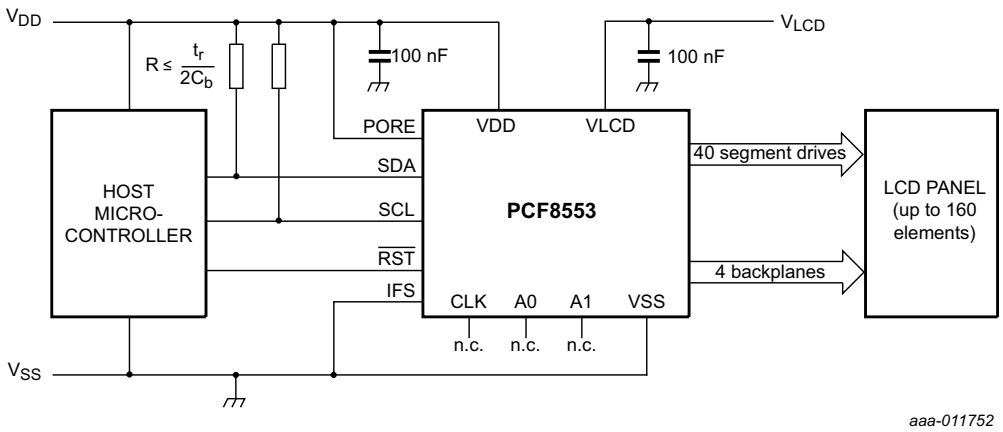
Fig 6. Example of displays suitable for PCF8553

Table 11. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix: segments/ elements**
		7-segment[1]	**14-segment[2]**	
4	160	20	10	160 dots (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 dots (2 × 40)
1	40	5	2	40 dots (1 × 40)

[1] 7 segment display has 8 segments/elements including the decimal point.

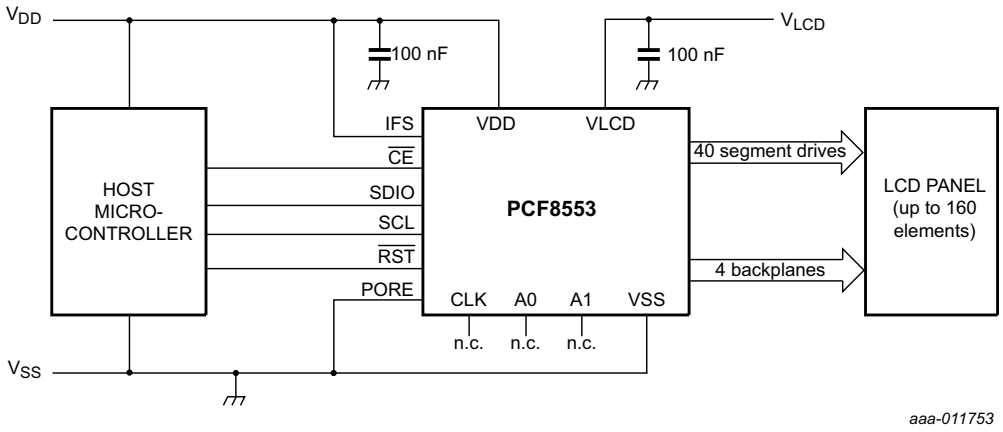
[2] 14 segment display has 16 segments/elements including decimal point and accent dot.



The resistance of the power lines must be kept to a minimum. A decoupling capacitor of at least 100 nF is recommended for the supplies.

Fig 7. Typical system configuration using I²C-bus, internal power-on reset enabled

The host microcontroller manages the 2-line I²C-bus communication channel with the PCF8553. The internal oscillator is used and the internal POR is enabled in the example. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the reset, the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.



The resistance of the power lines must be kept to a minimum. A decoupling capacitor of at least 100 nF is recommended for the supplies.

Fig 8. Typical system configuration using SPI-bus, internal power-on reset disabled

The host microcontroller manages the 3-line SPI-bus communication channel with the PCF8553. The internal oscillator is enabled. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are reset, the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

9.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between V_{LCD} and V_{SS}. These intermediate levels are tapped off at positions of ⅓ and ⅔, or ½, depending on the bias mode chosen. To keep current consumption to a minimum, on-chip low-power buffers provide these levels to the display.

9.2 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the Display_ctrl_1 command (see Table 7). The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 12.

Table 12. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated with Equation 2

$$\frac{1}{1 + a_{bias}} \tag{2}$$

The values for a_{bias} are:

a_{bias} = 1 for ½ bias

a_{bias} = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a_{bias}^2 + 2a_{bias} + n_{MUX}}{n_{MUX} \times (1 + a_{bias})^2}} \tag{3}$$

where the values for n are

n_{MUX} = 1 for static drive mode

n_{MUX} = 2 for 1:2 multiplex drive mode

n_{MUX} = 3 for 1:3 multiplex drive mode

n_{MUX} = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a_{bias}^2 - 2a_{bias} + n_{MUX}}{n_{MUX} \times (1 + a_{bias})^2}} \quad (4)$$

Discrimination is a term which is defined as the ratio of the on and off RMS voltages ($V_{on(RMS)}$ to $V_{off(RMS)}$) across a segment. It can be thought of as a measurement of contrast. Discrimination is determined from Equation 5:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a_{bias}^2 + 2a_{bias} + n_{MUX}}{a_{bias}^2 - 2a_{bias} + n_{MUX}}} \quad (5)$$

Using Equation 5, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

9.2.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 9. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (6)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (7)$$

$V_{on(RMS)}$ (see Equation 3) and $V_{off(RMS)}$ (see Equation 5) are properties of the display driver and are affected by the selection of a_{bias}, n_{MUX}, and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

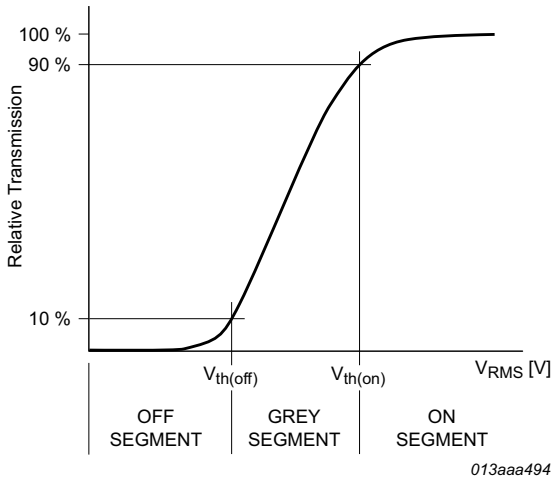
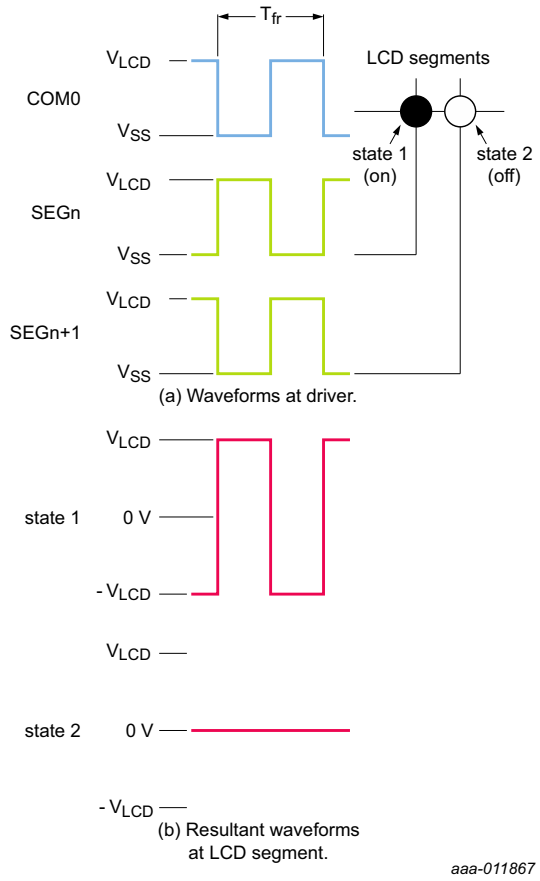


Fig 9. Electro-optical characteristic: relative transmission curve of the liquid

9.2.2 LCD drive mode waveforms

9.2.2.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (COMn) and segment (SEGn) drive waveforms for this mode are shown in Figure 10.



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

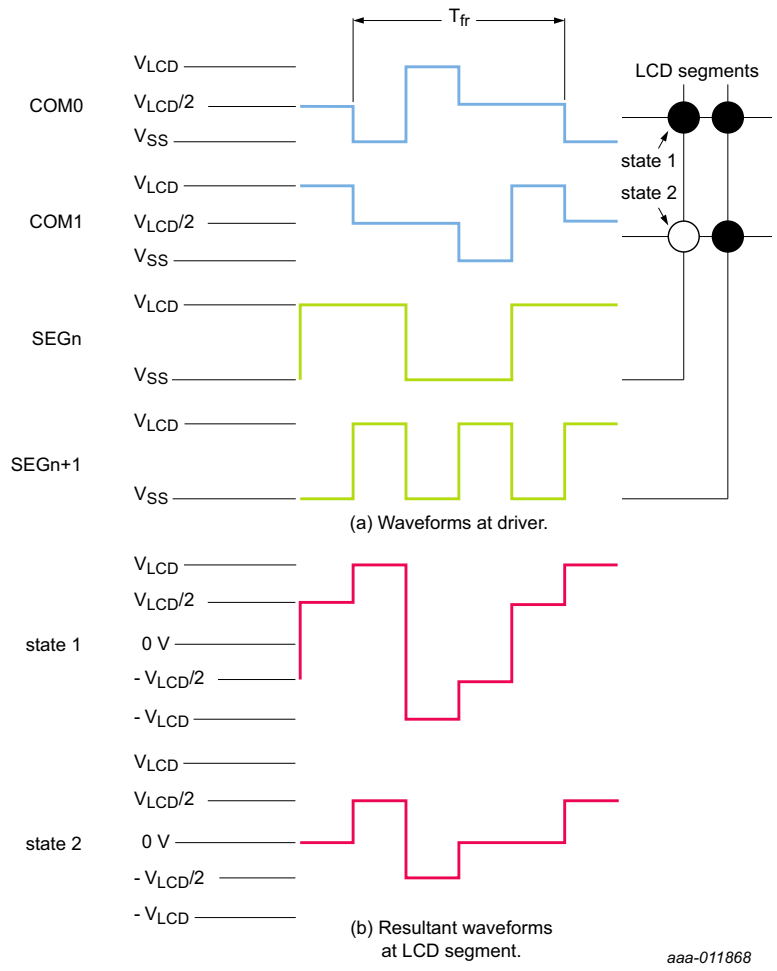
$V_{state2}(t) = V_{(SEGn + 1)}(t) - V_{COM0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 10. Static drive mode waveforms

9.2.2.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8553 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 11 and Figure 12.



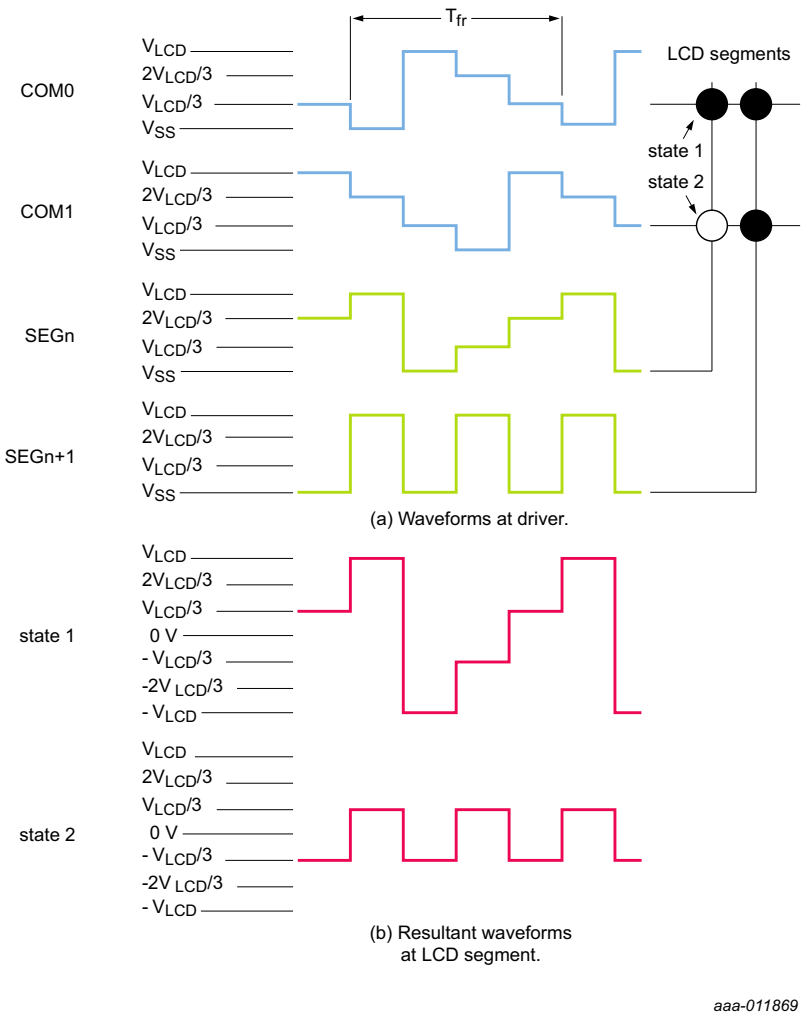
$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 11. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

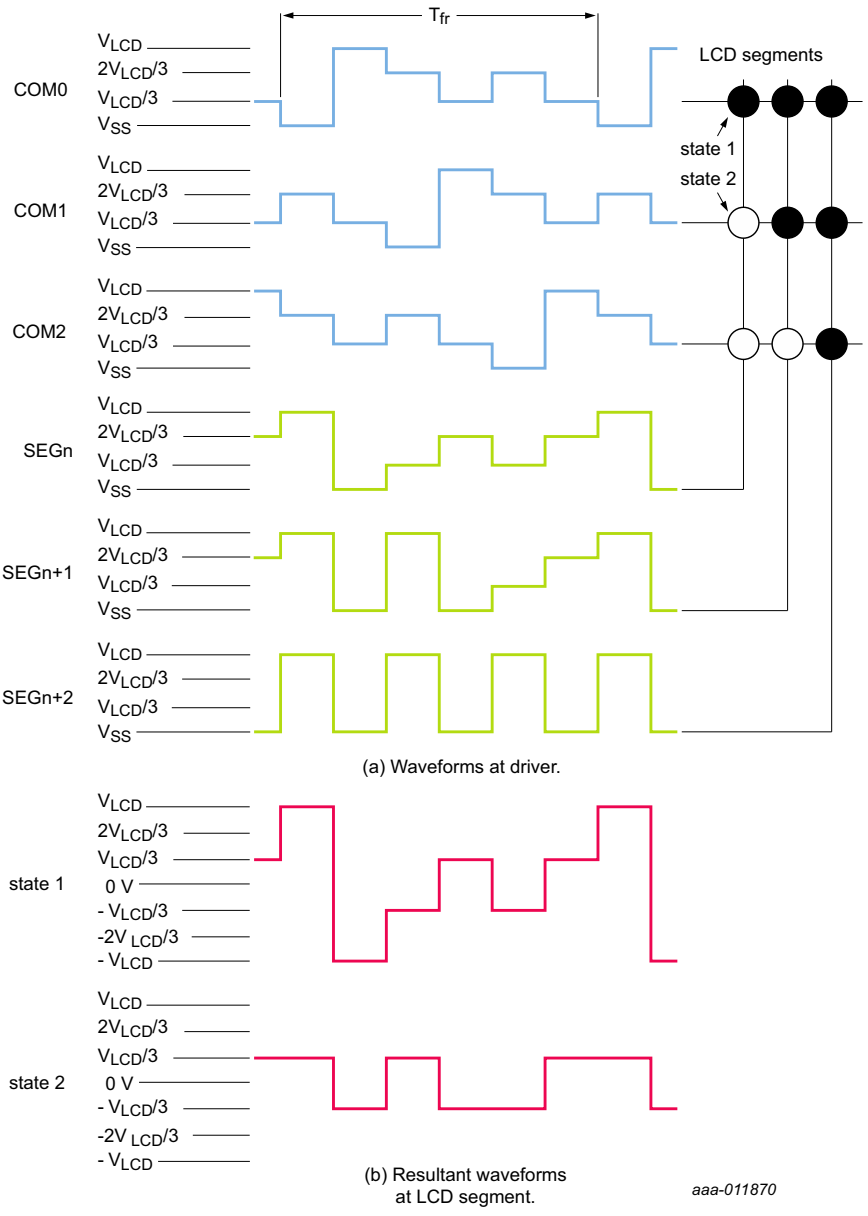
$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 12. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

9.2.2.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 13.



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

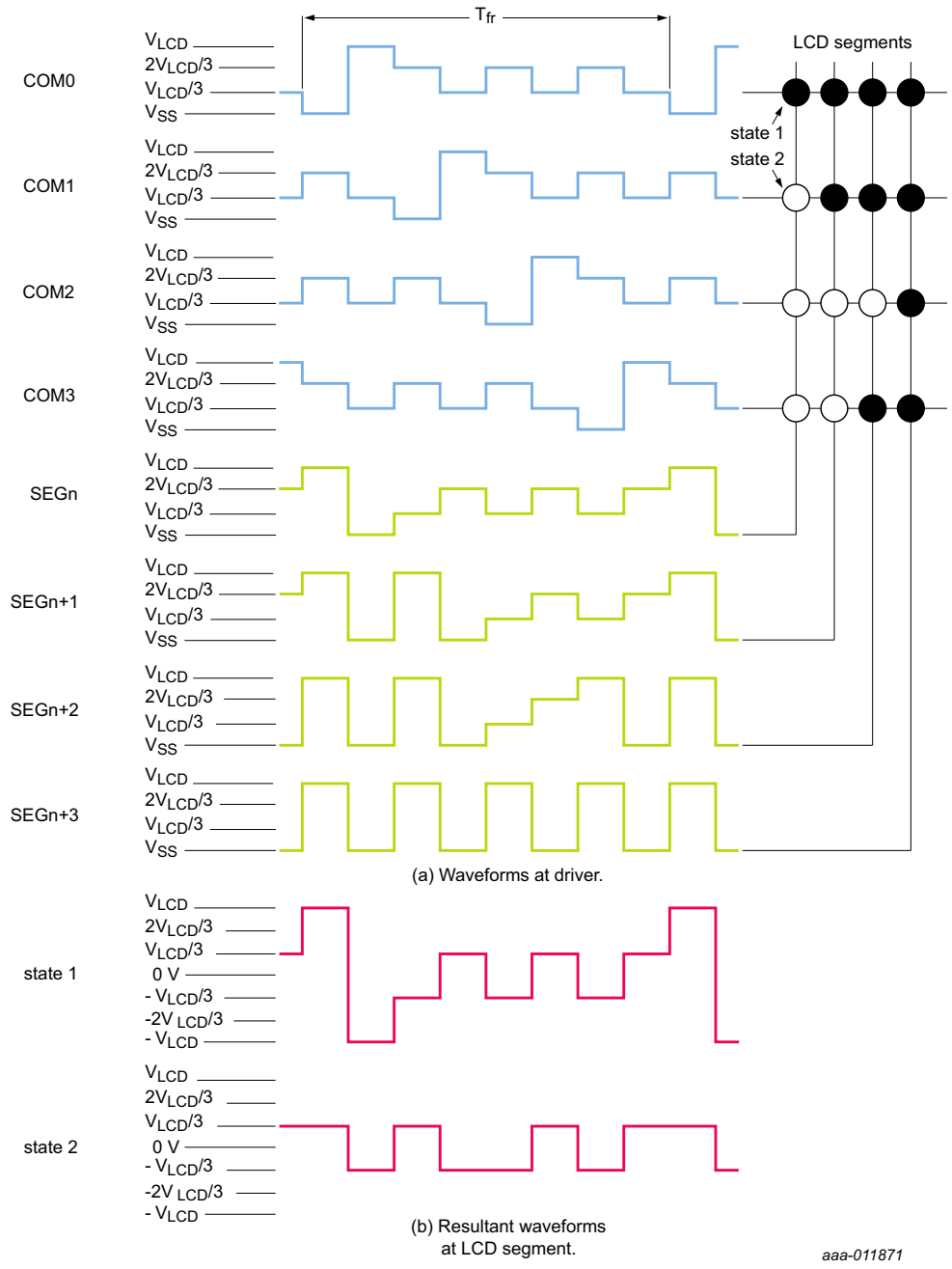
$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 13. Waveforms for the 1:3 multiplex drive mode with $^1/_3$ bias

9.2.2.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 14.



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 14. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

9.3 Backplane and segment outputs

9.3.1 Backplane outputs

The LCD drive section includes four backplane outputs COM0 to COM3, which must be directly connected to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, COM3 carries the same signal as COM1, therefore these two outputs can be tied together to give enhanced drive capabilities
- In 1:2 multiplex drive mode, COM0 and COM2, respectively, COM1 and COM3 all carry the same signals and may also be paired to increase the drive capabilities
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements

9.3.2 Segment outputs

The LCD drive section includes 40 segment outputs SEG0 to SEG39, which must be directly connected to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display registers. When less than 39 segment outputs are required, the unused segment outputs must be left open-circuit.

10. Power Sequencing

10.1 Power-on

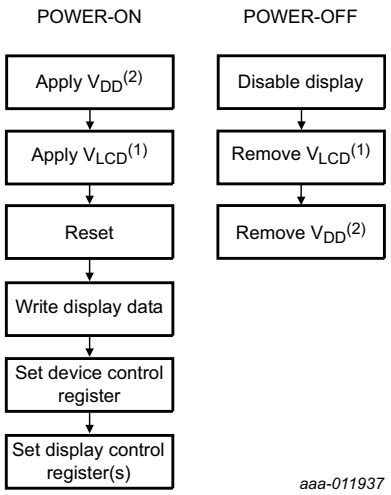
To avoid unwanted artifacts on the display, V_{LCD} must never be asserted before V_{DD}, it is permitted to assert V_{DD} and V_{LCD} at the same time.

10.2 Power-off

Before turning the power to the device off, the display must be disabled by setting bit DE to logic 0. To avoid unwanted artifacts on the display, V_{LCD} must never be connected, while V_{DD} is switched off. It is permitted to switch off V_{DD} and V_{LCD} simultaneously.

10.3 Power sequences

Figure 15 depicts the recommended power-up and power-off sequence.



(1) Can be simultaneous with V_{DD}.

(2) Can be simultaneous with V_{LCD}.

Fig 15. Recommended power-up and power-off sequence