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PCF8564A

Real time clock and calendar

Rev. 3 — 26 August 2013

Product data sheet

1. General description

The PCF8564A is a CMOS¹ real-time clock and calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All addresses and data are transferred serially via the two-line bidirectional I²C-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Wide clock operating voltage: 1.0 V to 5.5 V
- Low back-up current typical 250 nA at 3.0 V and 25 °C
- 400 kHz two-wire I²C interface (1.8 V to 5.5 V)
- Low-voltage detector
- Alarm and timer functions
- Two integrated oscillator capacitors
- Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz, and 1 Hz)
- Internal Power-On Reset (POR)
- I²C slave address: read A3h, write A2h

3. Applications

- Timing devices
 - ◆ Time of the day tracking
 - ◆ Process timing
 - ◆ Alarm
- Portable instruments
- Electronic metering
- Battery powered products

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 20](#).



4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8564AU	bare die	wire bond die; 9 bonding pads	PCF8564AU
PCF8564AUG	bare die	9 bumps	PCF8564AUG

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8564AU/10AB/1	935289478005	PCF8564AU/10AB/1,0	1	wafer, sawn, on FFC
PCF8564AU/5BB/1	935289319015	PCF8564AU/5BB/1,01	1	unsawn wafer
PCF8564AU/5GB/1	935289477015	PCF8564AU/5GB/1,01	1	unsawn wafer
PCF8564AU/5GC/1	935293569015	PCF8564AU/5GC/1,01	1	unsawn wafer
PCF8564AUG/12HB/1	935301011005	PCF8564AUG/12HB/1V	1	wafer, sawn, on 8 inch metal FFC; chips with soft bumps ^[1]

[1] Bump hardness, see [Table 36](#).

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF8564AU	PC8564A-1
PCF8564AUG	PC8564A-1

6. Block diagram

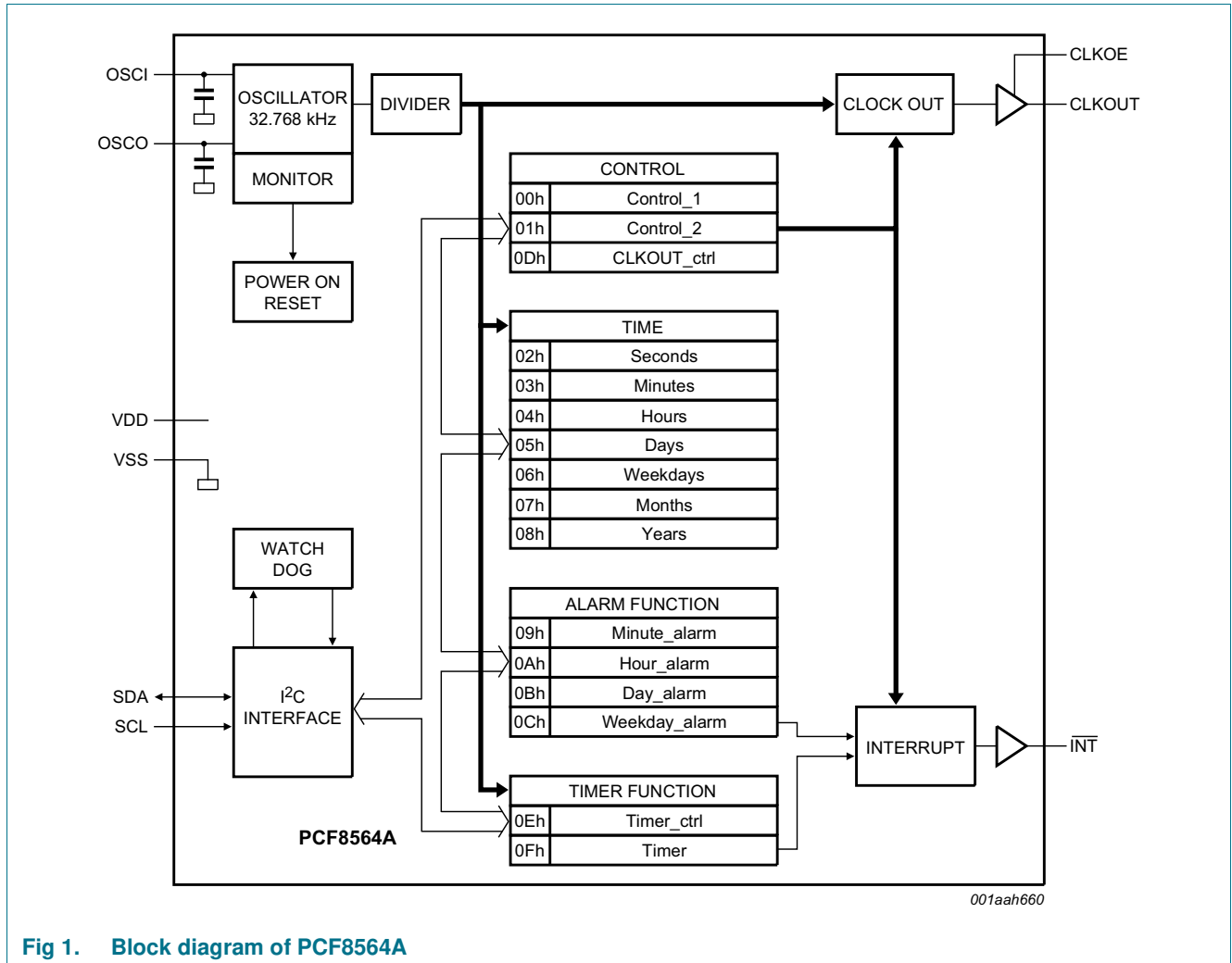
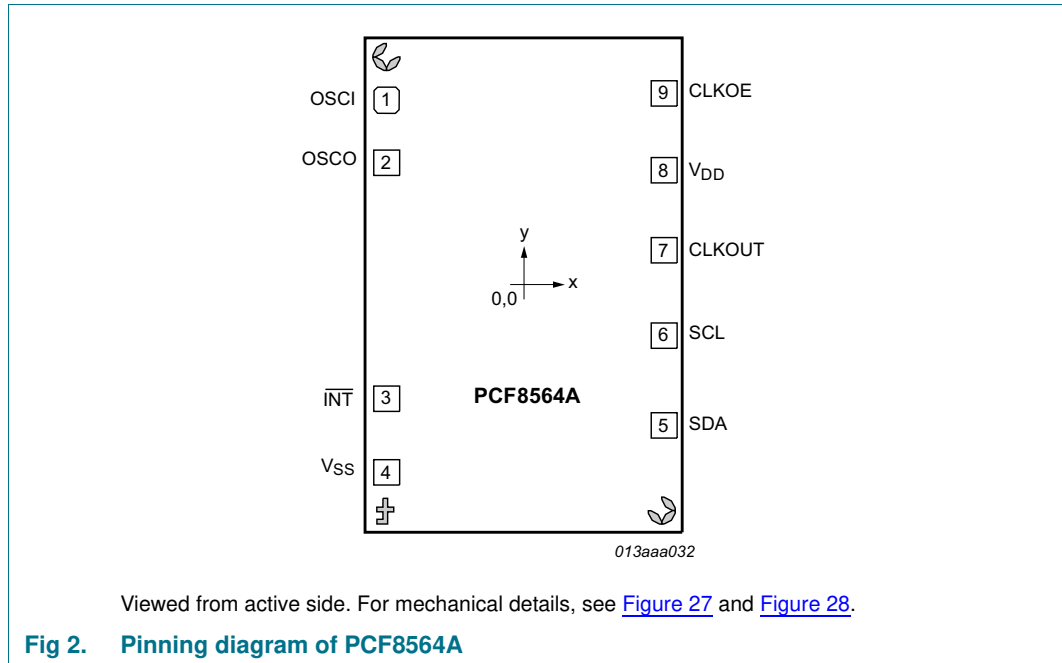


Fig 1. Block diagram of PCF8564A

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
$\overline{\text{INT}}$	3	interrupt output, open-drain, active LOW
V_{SS}	4	ground ^[1]
SDA	5	serial data input and output
SCL	6	serial clock input
CLKOUT	7	clock output, push-pull
V_{DD}	8	supply voltage
CLKOE	9	CLKOUT enable input

[1] The substrate (rear side of the die) is at V_{SS} potential and must not be connected.

8. Functional description

The PCF8564A contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the RTC, a programmable clock output, a timer, a voltage low detector, and a 400 kHz I²C-bus interface.

All sixteen registers (see [Table 5](#)) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm. Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, months, years, as well as the minute alarm, hour alarm, and day alarm registers are all coded in BCD format.

8.1 CLKOUT output

A programmable square wave is available at the CLKOUT pin. Frequencies of 32.768 kHz, 1.024 kHz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is a CMOS push-pull output, and if disabled it becomes logic 0.

8.2 Register organization

Table 5. Register overview

Bit positions labelled as - are not implemented. Bit positions labelled as N should always be written with logic 0. After reset, all registers are set according to [Table 28](#).

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control registers									
00h	Control_1	TEST1	N	STOP	N	TESTC	N	N	N
01h	Control_2	N	N	N	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	Seconds	VL	SECONDS (0 to 59)						
03h	Minutes	-	MINUTES (0 to 59)						
04h	Hours	-	-	HOURS (0 to 23)					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS		
07h	Months	C	-	-	MONTH (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AEN_H	-	HOUR_ALARM (0 to 23)					
0Bh	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM		
CLKOUT control register									
0Dh	CLKOUT_ctrl	FE	-	-	-	-	-	FD[1:0]	
Timer registers									
0Eh	Timer_ctrl	TE	-	-	-	-	-	TD[1:0]	
0Fh	Timer	TV[7:0]							

8.3 Control registers

8.3.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	TEST1	0 ^[1]	normal mode; <ul style="list-style-type: none"> must be set to logic 0 during normal operations 	Section 8.9
		1	EXT_CLK test mode (see Section 8.9)	
6	N	0 ^[2]	default value	
5	STOP	0 ^[1]	RTC source clock runs	Section 8.10
		1	<ul style="list-style-type: none"> RTC divider chain flip-flops are asynchronously set to logic 0 the RTC clock is stopped (CLKOUT at 32.768 kHz is still available) 	
4	N	0 ^[2]	default value	
3	TESTC	0	Power-On Reset (POR) override facility is disabled; <ul style="list-style-type: none"> set to logic 0 for normal operation (see Section 8.11.1) 	Section 8.11.1
		1 ^[1]	Power-On Reset (POR) override is enabled	
2 to 0	N	000 ^[2]	default value	

[1] Default value.

[2] Bits labeled as N should always be written with logic 0.

8.3.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit description

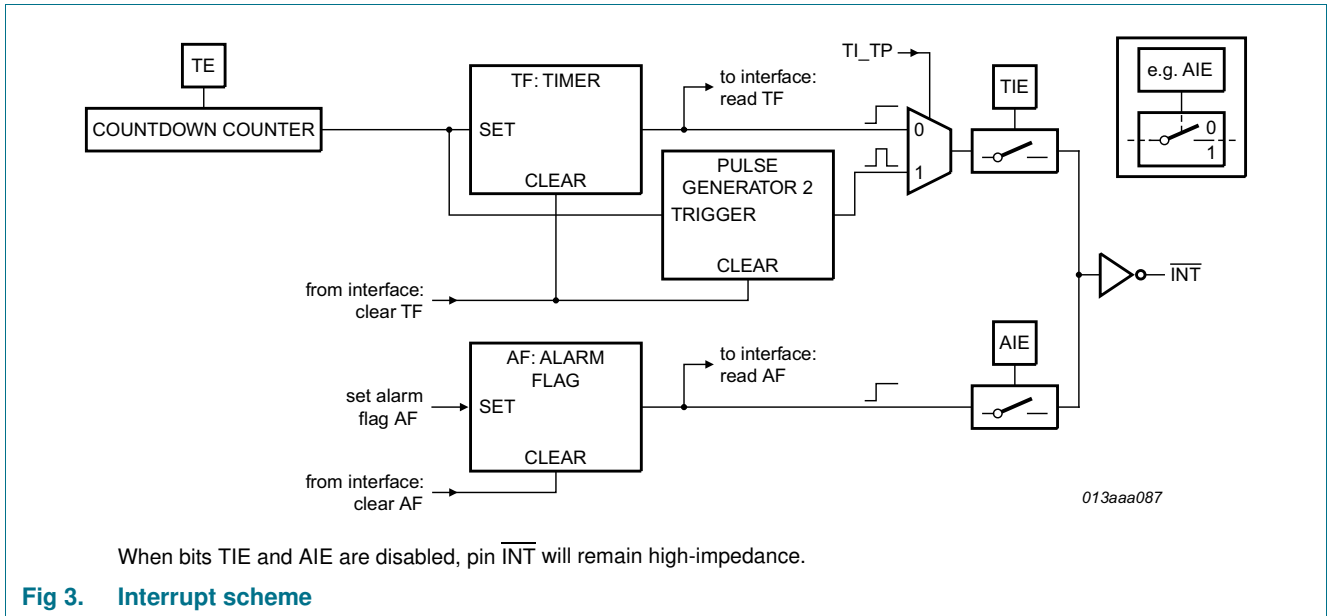
Bit	Symbol	Value	Description	Reference
7 to 5	N	000 ^[1]	default value	
4	TI_TP	0 ^[2]	$\overline{\text{INT}}$ is active when TF is active (subject to the status of TIE)	Section 8.3.2.1 and Section 8.8
		1	$\overline{\text{INT}}$ pulses active according to Table 8 (subject to the status of TIE); <ul style="list-style-type: none"> Remark: note that if AF and AIE are active then $\overline{\text{INT}}$ will be permanently active 	
3	AF	0 ^[2]	alarm flag inactive	Section 8.3.2.1
		1	alarm flag active	
2	TF	0 ^[2]	timer flag inactive	Section 8.3.2.1
		1	timer flag active	
1	AIE	0 ^[2]	alarm interrupt disabled	Section 8.3.2.1
		1	alarm interrupt enabled	
0	TIE	0 ^[2]	timer interrupt disabled	Section 8.3.2.1
		1	timer interrupt enabled	

[1] Bits labeled as N should always be written with logic 0.

[2] Default value.

8.3.2.1 Interrupt output

Bits TF and AF: When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value until overwritten by command. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.



Bits TIE and AIE: These bits activate or deactivate the generation of an interrupt when TF or AF is asserted respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

Countdown timer interrupts: The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value TV. As a consequence, the width of the interrupt pulse varies (see [Table 8](#)).

Table 8. $\overline{\text{INT}}$ operation (bit TI_TP = 1)^[1]

Source clock (Hz)	INT period (s)	
	TV = 1 ^[2]	TV > 1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1] TF and $\overline{\text{INT}}$ become active simultaneously.

[2] TV = loaded countdown value. Timer is stopped when TV = 0.

8.4 Time and date registers

The majority of the registers are coded in the BCD format to simplify application use.

8.4.1 Register Seconds

Table 9. Seconds - seconds and clock integrity status register (address 02h) bit description

Bit	Symbol	Value	Place value	Description
7	VL	0	-	clock integrity is guaranteed
		1 ^[1]	-	integrity of the clock information is not guaranteed
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format, see Table 10
3 to 0		0 to 9	unit place	

[1] Start-up value.

Table 10. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:							
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:							
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.4.1.1 Voltage low detector and clock monitor

The PCF8564A has an on-chip voltage low detector. When V_{DD} drops below V_{low} the VL (Voltage Low) flag is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by command.

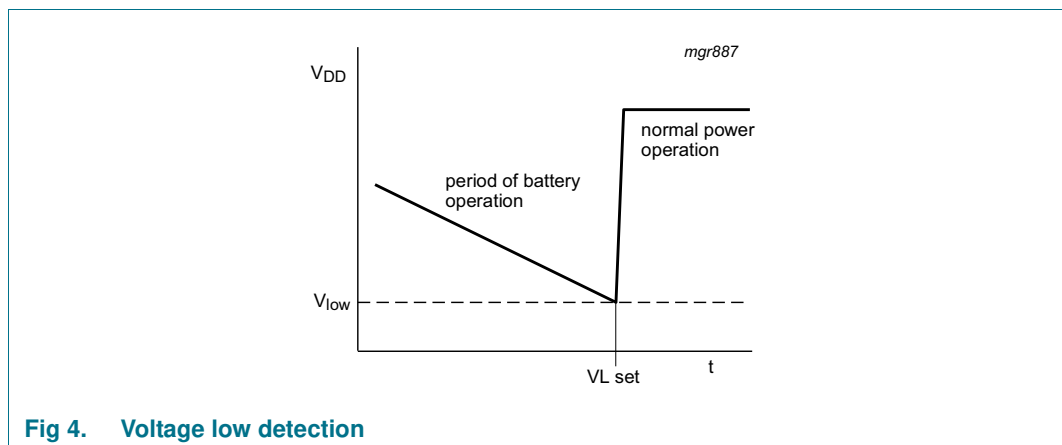


Fig 4. Voltage low detection

The VL flag is intended to detect the situation when V_{DD} is decreasing slowly, for example under battery operation. Should the oscillator stop or V_{DD} reach V_{low} before power is re-asserted, then the VL flag will be set. This indicates that the time is possibly corrupted.

8.4.2 Register Minutes

Table 11. Minutes - minutes register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.4.3 Register Hours

Table 12. Hours - hours register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	HOURS	0 to 2	ten's place	actual hours coded in BCD format
3 to 0		0 to 9	unit place	

8.4.4 Register Days

Table 13. Days - days register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS ^[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCF8564A compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.4.5 Register Weekdays

Table 14. Weekdays - weekdays register (address 06h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday values, see Table 15

Table 15. Weekday assignments

Day ^[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be re-assigned by the user.

8.4.6 Register Months

Table 16. Months - months and century flag register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7	C ^[1]	0 ^[2]	-	indicates the century is x
		1	-	indicates the century is x + 1
6 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 17
3 to 0		0 to 9	unit place	

[1] This bit may be re-assigned by the user.

[2] This bit is toggled when the register Years overflows from 99 to 00.

Table 17. Month assignments coded in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.4.7 Register Years

Table 18. Years - years register (08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format ^[1]
3 to 0		0 to 9	unit place	

[1] When the register Years overflows from 99 to 00, the century bit C in the register Months is toggled.

The PCF8564A compensates for leap years by adding a 29th day to February if the year counter contains a value which is divisible by 4, including the year 00.

8.5 Setting and reading the time

Figure 5 shows the data flow and data dependencies starting from the 1 Hz clock tick.

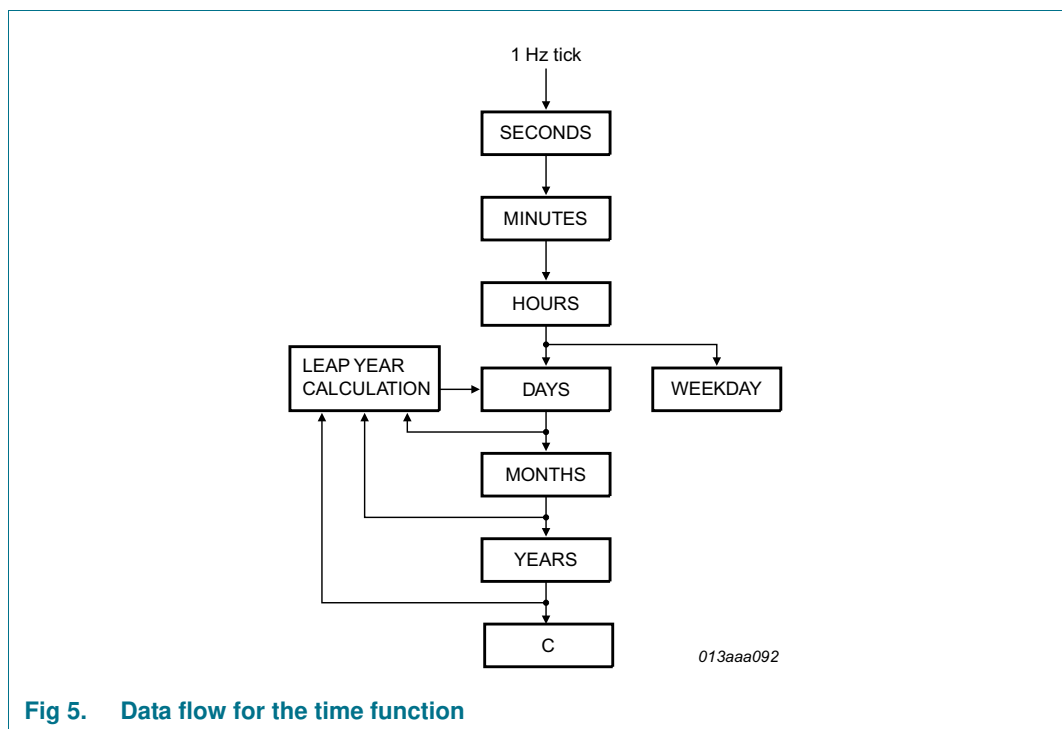


Fig 5. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty writing or reading of the clock and calendar during a carry condition
- Incrementing the time registers, during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters, that occurred during the read access, is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 6).

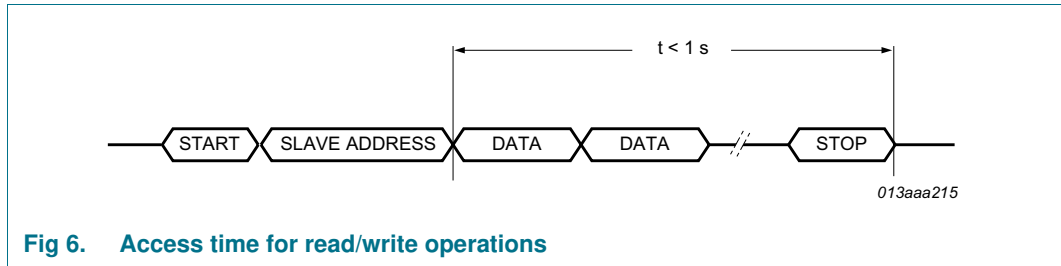


Fig 6. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h).
2. Set the address pointer to 2 (seconds) by sending 02h.
3. Send a RE-START condition or STOP followed by START.
4. Send the slave address for read (A3h).
5. Read the seconds.
6. Read the minutes.
7. Read the hours.
8. Read the days.
9. Read the weekdays.
10. Read the century and month.
11. Read the years.
12. Send a STOP condition.

8.6 Alarm registers

8.6.1 Register Minute_alarm

Table 19. Minute_alarm - minute alarm register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_M	0	-	minute alarm is enabled
		1 ^[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.6.2 Register Hour_alarm

Table 20. Hour_alarm - hour alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_H	0	-	hour alarm is enabled
		1 ^[1]	-	hour alarm is disabled
6	-	-	-	unused
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.6.3 Register Day_alarm

Table 21. Day_alarm - day alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_D	0	-	day alarm is enabled
		1 ^[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.6.4 Register Weekday_alarm

Table 22. Weekday_alarm - weekday alarm register (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1 ^[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

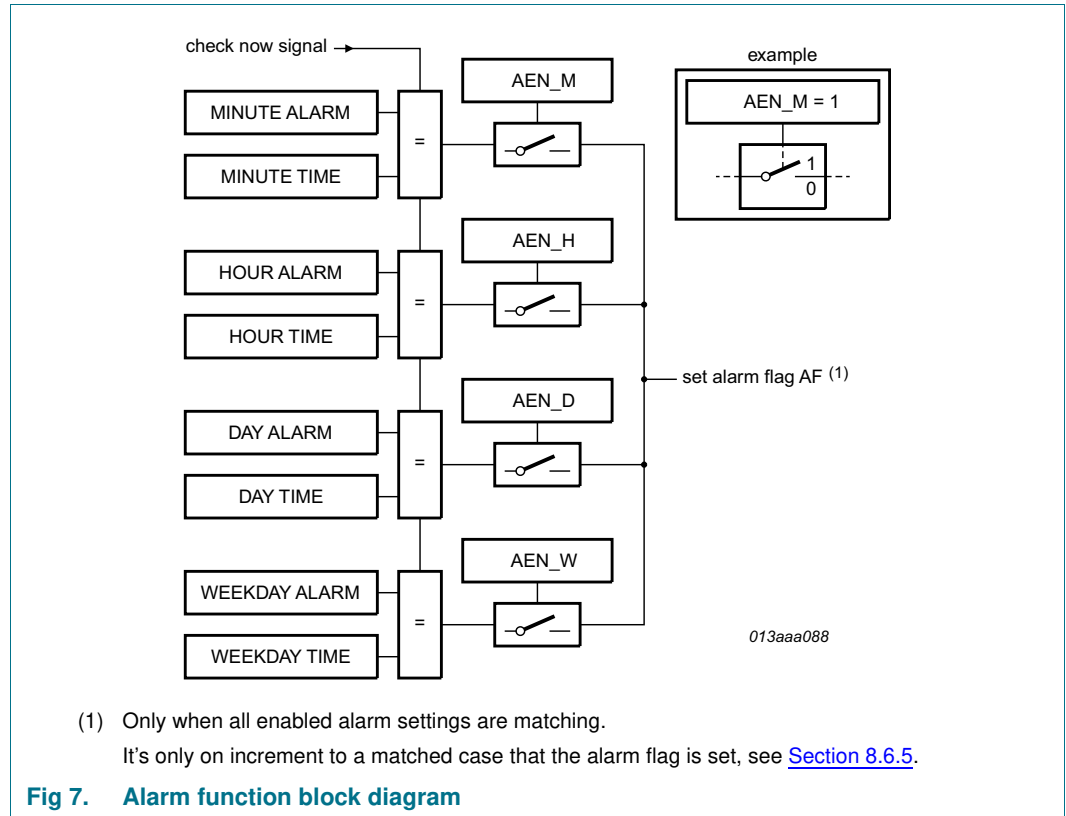
[1] Default value.

8.6.5 Alarm flag

By clearing the MSB of one or more of the alarm registers AEN_x (Alarm Enable), the corresponding alarm condition(s) are active. When an alarm occurs, AF is set to logic 1. The asserted AF can be used to generate an interrupt (INT). The AF is cleared by command.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with a valid minute, hour, day, or weekday and its corresponding Alarm Enable bit (AEN_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF in register Control_2) is set to logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{\text{INT}}$ pin follows the condition of bit AF. AF will remain set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN_x bit at logic 1 are ignored.



8.7 Register CLKOUT_ctrl and clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the FE bit in register CLKOUT_ctrl at address 0Dh and the CLKOUT output enable pin (CLKOE). To enable pin CLKOUT pin CLKOE must be set HIGH.

Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Table 23. CLKOUT_ctrl - CLKOUT control register (address 0Dh) bit description

Bit	Symbol	Value	Description
7	FE	0	the CLKOUT output is inhibited and CLKOUT output is set to logic 0
		1 ^[1]	the CLKOUT output is activated
6 to 2	-	-	unused
1 to 0	FD[1:0]		frequency output at pin CLKOUT
		00 ^[1]	32.768 kHz
		01	1.024 kHz
		10	32 Hz
		11	1 Hz

[1] Default value.

8.8 Timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $\frac{1}{60}$ Hz) and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the TF (Timer Flag) to logic 1. The TF may only be cleared using the interface.

The generation of interrupts from the timer function is controlled via bit TIE. If bit TIE is enabled the $\overline{\text{INT}}$ pin follows the condition of bit TF. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of the timer flag TF. TI_TP is used for this mode control. When reading the timer, the current countdown value is returned.

8.8.1 Register Timer_ctrl

Table 24. Timer_ctrl - timer control register (address 0Eh) bit description

Bit	Symbol	Value	Description
7	TE	0 ^[1]	timer is disabled
		1	timer is enabled
6 to 2	-	-	unused
1 to 0	TD[1:0]		timer source clock frequency select ^[2]
		00	4.096 kHz
		01	64 Hz
		10	1 Hz
		11 ^[2]	$\frac{1}{60}$ Hz

[1] Default value.

[2] These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to $\frac{1}{60}$ Hz for power saving.

8.8.2 Register Timer

Table 25. Timer - timer register (address 0Fh) bit description

Bit	Symbol	Value	Description
7 to 0	TV[7:0]	0h to FFh	countdown timer value ^[1]

[1] Countdown period in seconds: $CountdownPeriod = \frac{TV}{SourceClockFrequency}$ where TV is the countdown timer value.

Table 26. Timer register bits value range

Bit							
7	6	5	4	3	2	1	0
128	64	32	16	8	4	2	1

The timer register is an 8-bit binary countdown timer. It is enabled or disabled via the timer control register. The source clock for the timer is also selected by the timer control register. Other timer properties such as single or periodic interrupt generation are controlled via the register Control_2 (address 01h).

For accurate read back of the count down value, the I²C-bus clock (SDA) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

8.9 EXT_CLK test mode

The test mode is entered by setting the TEST1 bit of register Control_1 to logic 1. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with that applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT then generates an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2⁶ divide chain called a prescaler. The prescaler can be set to a known state by using the STOP bit. When the STOP bit is set, the prescaler is reset to logic 0. (STOP must be cleared before the prescaler can operate.)

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

8.9.1 Operation example

1. Set EXT_CLK test mode (Bit 7 Control_1 = 1).
2. Set STOP (Bit 5 Control_1 = 1).
3. Clear STOP (Bit 5 Control_1 = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.

6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.10 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated (see [Figure 8](#)). The time circuits can then be set and will not increment until the STOP bit is released (see [Figure 9](#) and [Table 27](#)).

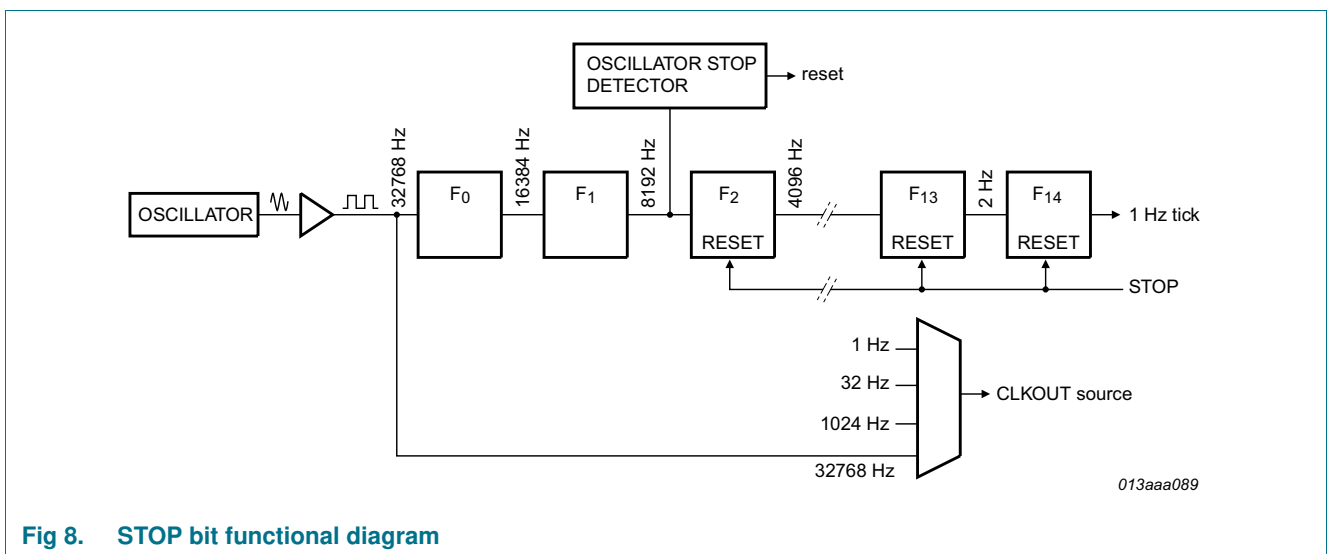


Fig 8. STOP bit functional diagram

The STOP bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz and 1 Hz.

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8.192 kHz cycle (see [Figure 9](#)).

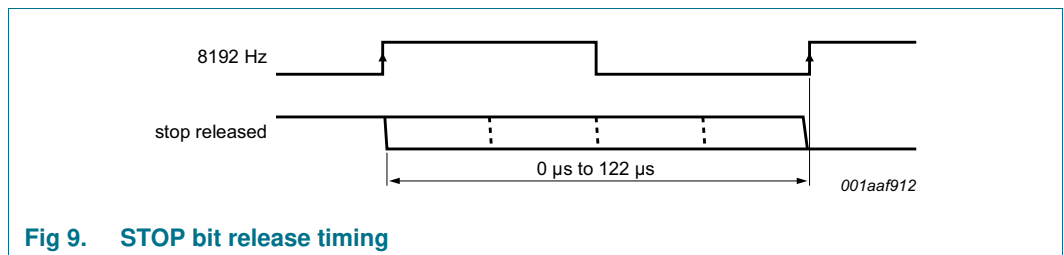


Fig 9. STOP bit release timing

Table 27. First increment of time circuits after STOP bit release

Bit	Prescaler bits [1]	1 Hz tick	Time	Comment
STOP	F₀F₁-F₂ to F₁₄		hh:mm:ss	
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP bit is activated by user. F₀F₁ are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F ₁₄ increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	-
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F ₁₄ increments the time circuits

013aaa076

[1] F₀ is clocked at 32.768 kHz.

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F₀ and F₁ not being reset (see [Table 27](#)) and the unknown state of the 32 kHz clock.

8.11 Reset

The PCF8564A includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I²C-bus logic is initialized including the address pointer and all registers are set according to [Table 28](#). I²C-bus communication is not possible during reset.

Table 28. Register reset values^[1]

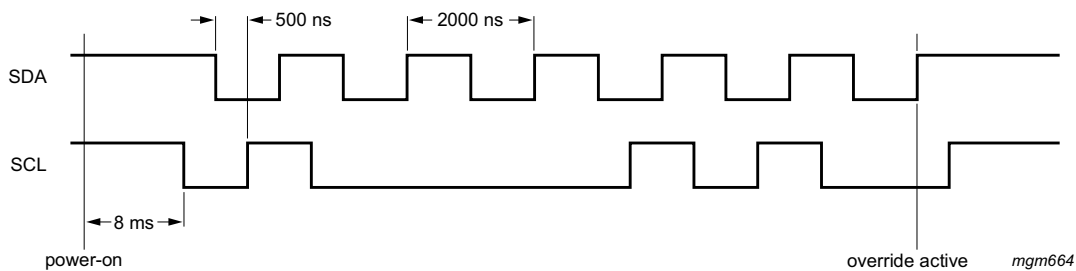
Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	1	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	x	x	x	x	x	x	x
03h	Minutes	x	x	x	x	x	x	x	x
04h	Hours	x	x	x	x	x	x	x	x
05h	Days	x	x	x	x	x	x	x	x
06h	Weekdays	x	x	x	x	x	x	x	x
07h	Months	x	x	x	x	x	x	x	x
08h	Years	x	x	x	x	x	x	x	x
09h	Minute_alarm	1	x	x	x	x	x	x	x
0Ah	Hour_alarm	1	x	x	x	x	x	x	x
0Bh	Day_alarm	1	x	x	x	x	x	x	x
0Ch	Weekday_alarm	1	x	x	x	x	x	x	x
0Dh	CLKOUT_ctrl	1	x	x	x	x	x	0	0
0Eh	Timer_ctrl	0	x	x	x	x	x	1	1
0Fh	Timer	x	x	x	x	x	x	x	x

[1] Registers marked 'x' are undefined at power-on and unchanged by subsequent resets.

8.11.1 Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a circuit has been implemented to disable the POR and speed up functional test of the module. The setting of this mode requires that the I²C signals on the pins SDA and SCL are toggled as illustrated in Figure 10. All timings shown are required minimums.

Once the override mode has been entered, the chip immediately stops, being reset, and normal operation may begin, i.e., entry into the EXT_CLK test mode via I²C access. The override mode may be cleared by writing logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect, except to prevent entry into the POR override mode.



Allow 500 ns between the edges of either signal.

Fig 10. POR override sequence

9. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DATA line (SDA) and a Serial CLOCK line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see [Figure 11](#)).

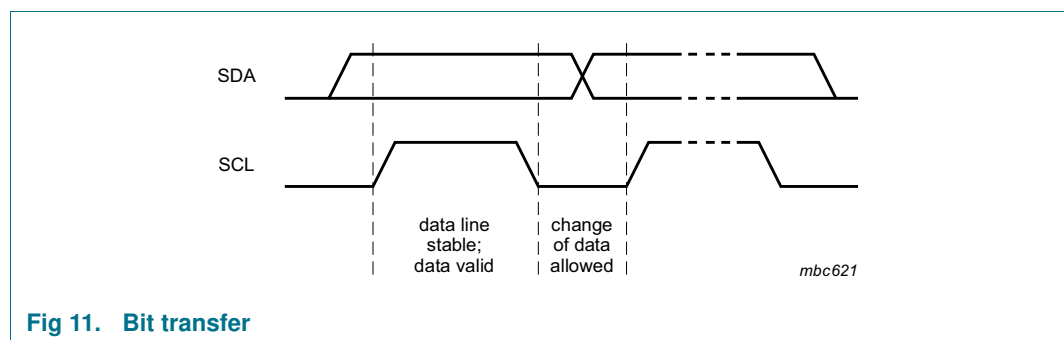


Fig 11. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P), see [Figure 12](#).

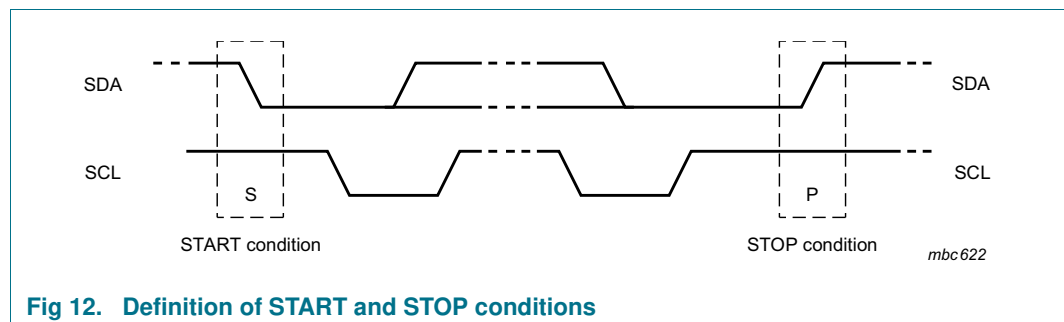


Fig 12. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see [Figure 13](#)).

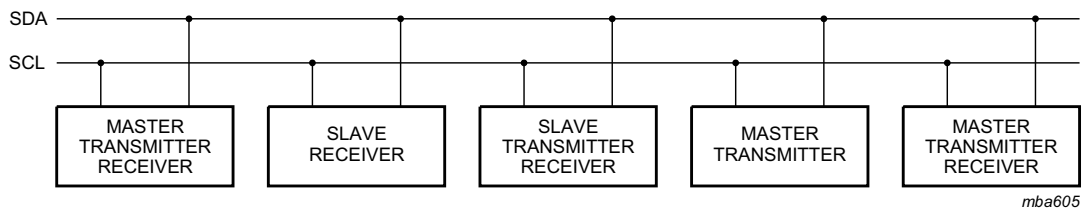


Fig 13. System configuration

9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is shown in [Figure 14](#).

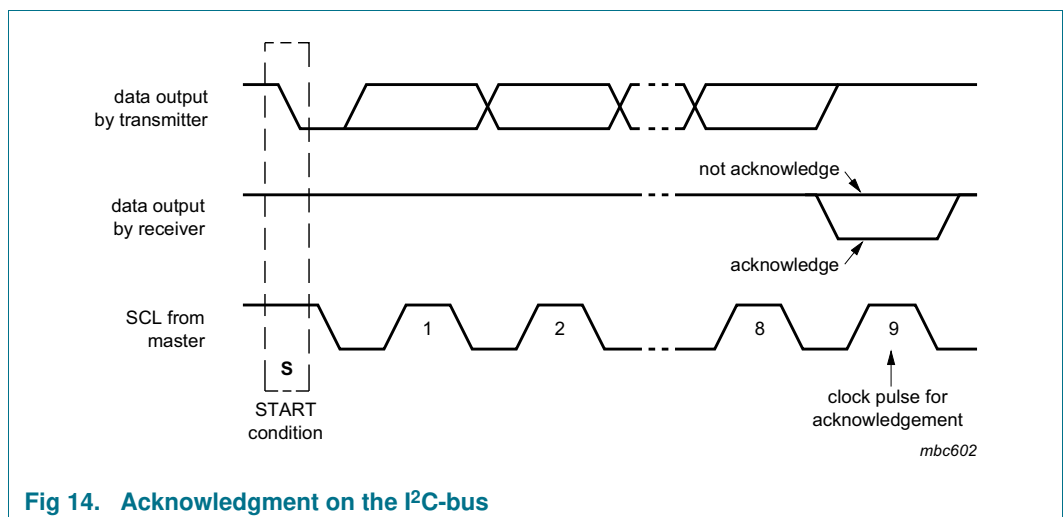


Fig 14. Acknowledgment on the I²C-bus

10. I²C-bus protocol

10.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8564A acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

Two slave addresses are reserved for the PCF8564A:

Read: A3h (1010 0011)

Write: A2h (1010 0010)

The PCF8564A slave address is shown in [Figure 14](#).

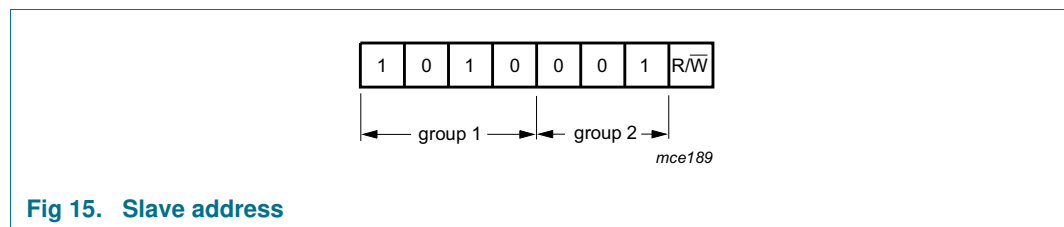


Fig 15. Slave address

10.2 Clock and calendar READ or WRITE cycles

[Figure 16](#), [Figure 17](#), and [Figure 18](#) show the I²C-bus configuration for the different PCF8564A READ and WRITE cycles. The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

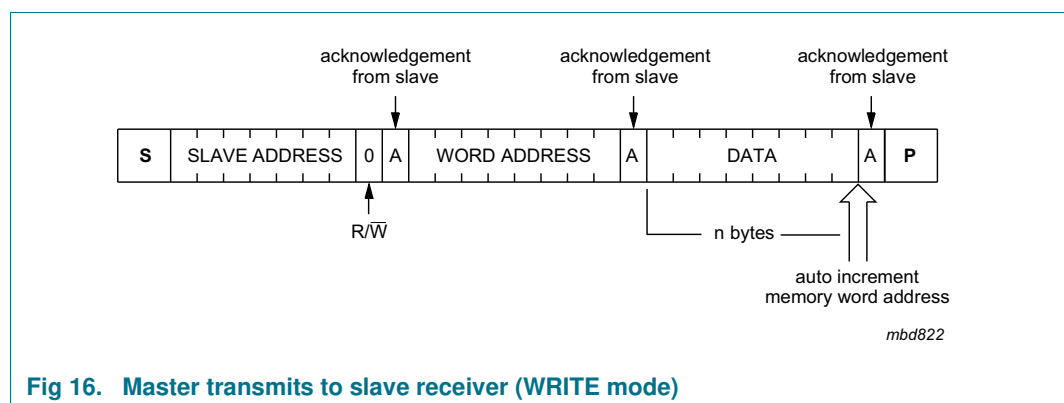


Fig 16. Master transmits to slave receiver (WRITE mode)

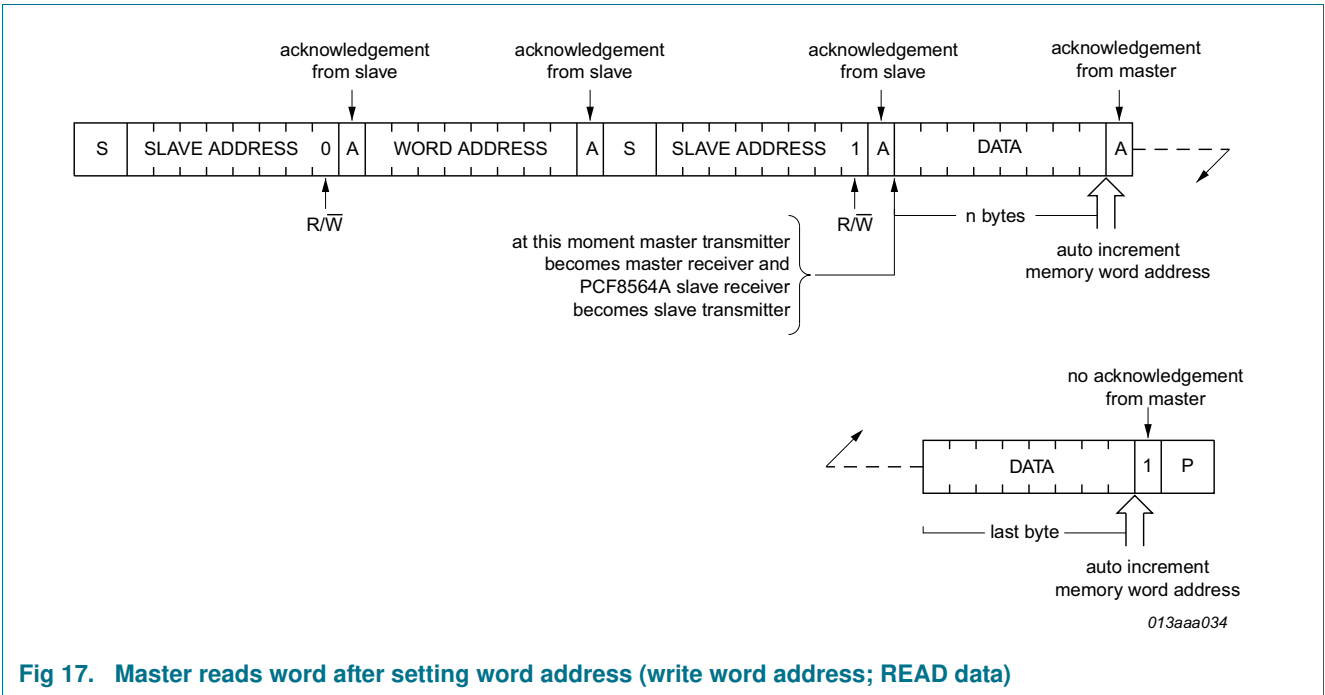


Fig 17. Master reads word after setting word address (write word address; READ data)

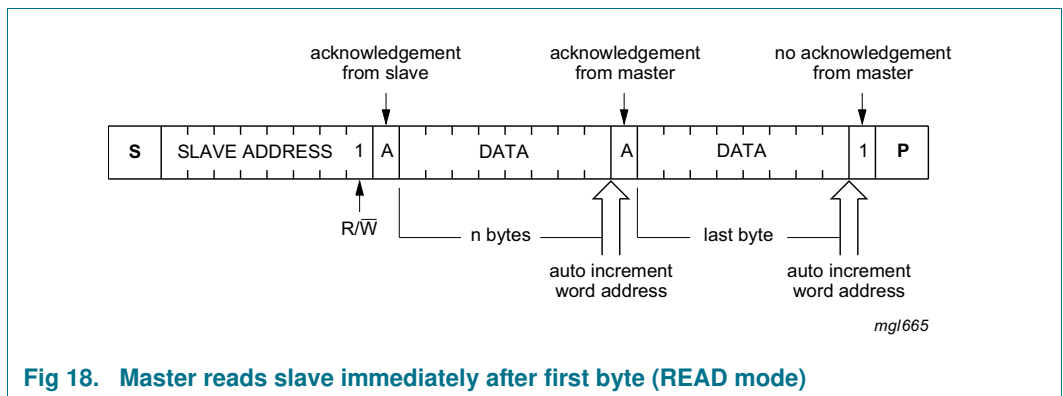


Fig 18. Master reads slave immediately after first byte (READ mode)

10.3 Interface watchdog timer

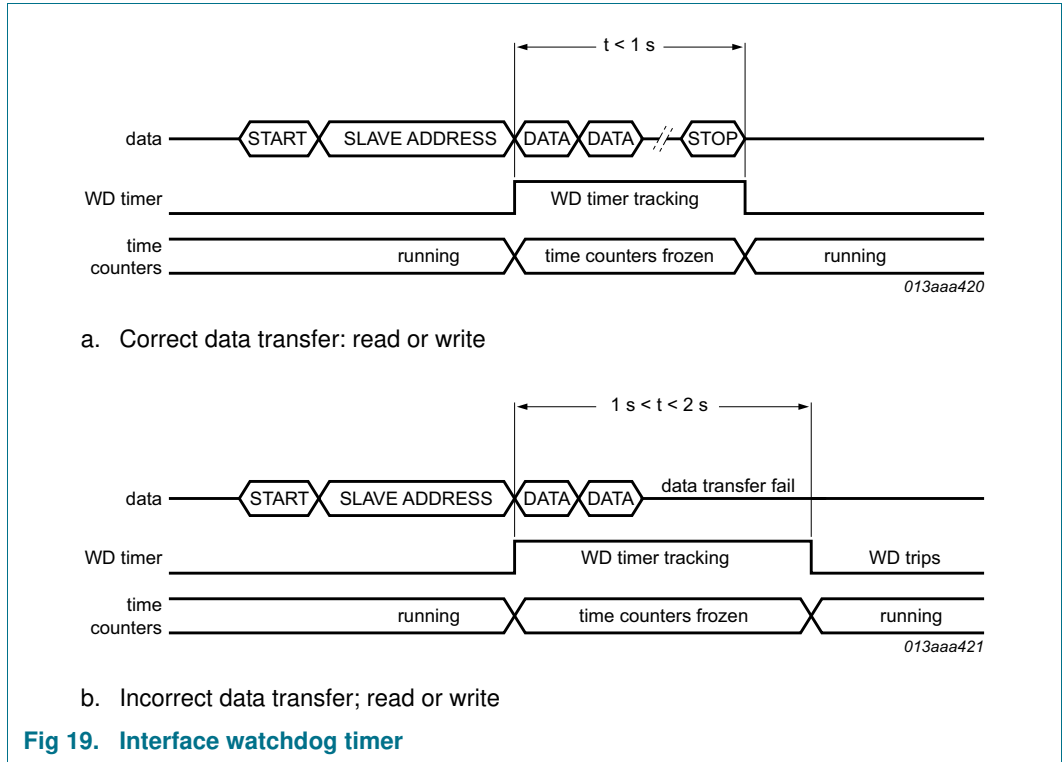


Fig 19. Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface, the PCF8564A has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid slave address is transmitted, then the PCF8564A will automatically clear the interface and allow the time counting circuits to continue counting. The watchdog will trigger between 1 s and 2 s after receiving a valid slave address. Each time the watchdog period is exceeded, 1 s will be lost from the time counters.

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.