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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PCF8576D

Universal LCD driver for low multiplex rates

Rev. 7 — 18 December 2008 Product data sheet

1. General description

The PCF8576D is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCF8576D is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

AEC-Q100 compliant (PCF8576DH/2) for automotive applications.

2. Features

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to twenty 7-segment numeric characters
  - Up to ten 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components
- Compatible with chip-on-glass and chip-on-board technology
- Manufactured in silicon gate CMOS process

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8576DH/2	TQFP64	plastic thin quad flat package, 64 leads; body 10 × 10 × 1.0 mm	SOT357-1
PCF8576DT/2	TSSOP56	plastic thin shrink small outline package, 56 leads; body width 6.1 mm	SOT364-1
PCF8576DU/DA/2	PCF8576DU/DA	wire bond die; 59 bonding pads; 2.26 × 2.01 × 0.38 mm[1]	PCF8576DU/DA
PCF8576DU/2DA/2	PCF8576DU/2DA	bare die; 59 bumps; 2.26 × 2.01 × 0.40 mm[1]	PCF8576DU/2DA

[1] Chips in tray.

[1] Chips with bumps in tray.

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF8576DH/2	PCF8576DH
PCF8576DT/2	PCF8576DT
PCF8576DU/DA/2	PC8576D-2
PCF8576DU/2DA/2	PC8576D-2

5. Block diagram

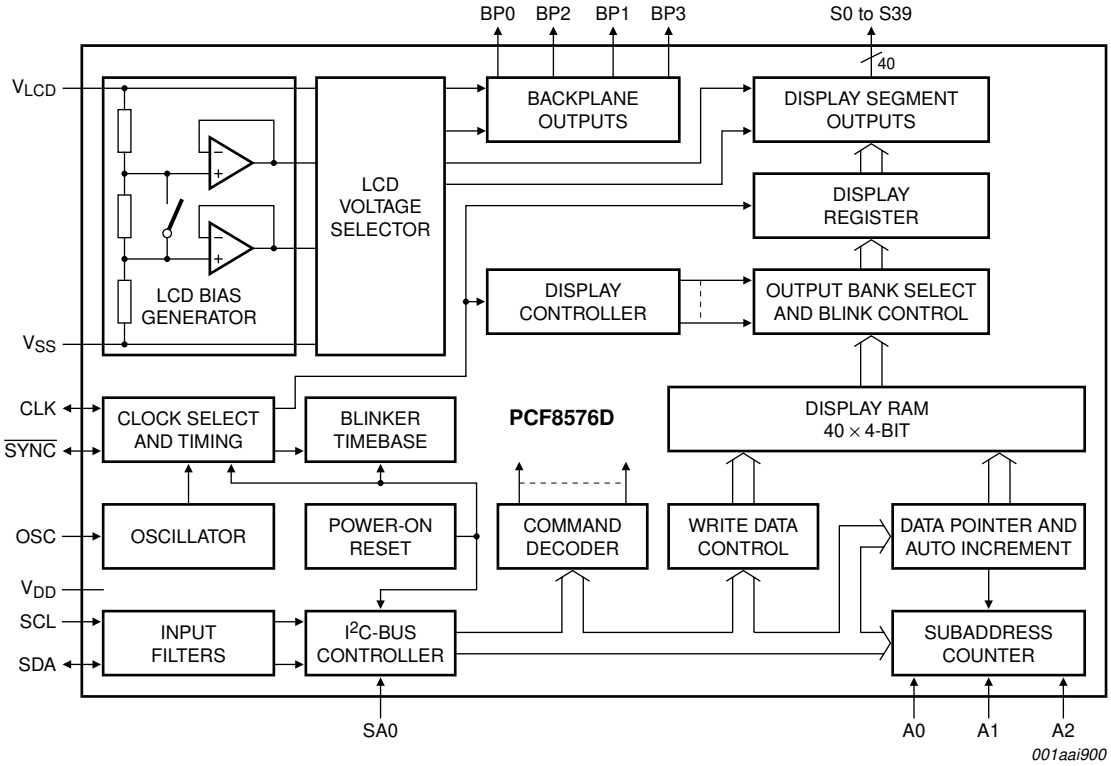
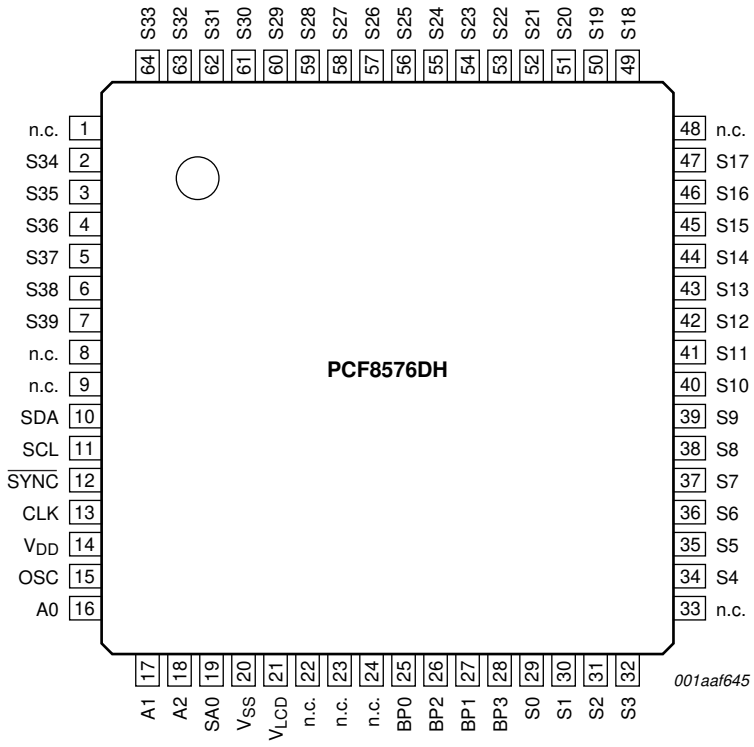


Fig 1. Block diagram of PCF8576D

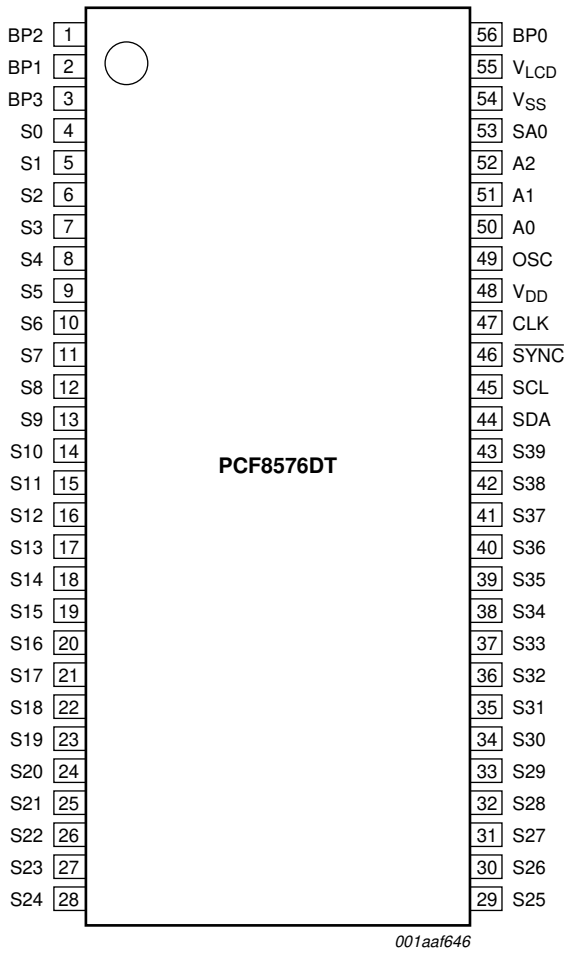
6. Pinning information

6.1 Pinning



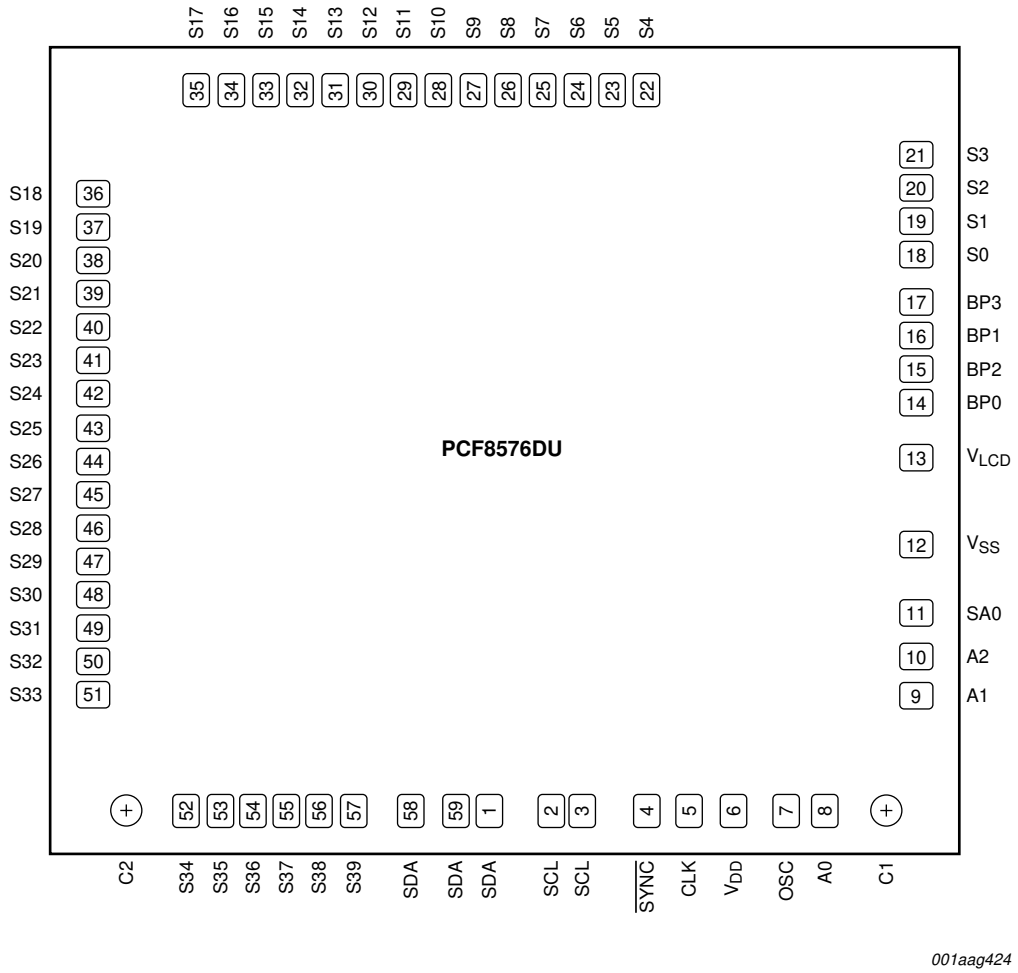
Top view. For mechanical details, see Figure 24.

Fig 2. Pinning diagram for PCF8576DH/2



Top view. For mechanical details, see Figure 25.

Fig 3. Pinning diagram for PCF8576DT/2



Top view. C1 and C2 are alignment marks. For mechanical details, see Figure 26 and Figure 27.

Fig 4. Pinning diagram for PCF8576DUx

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	PCF8576DH/2	PCF8576DT/2	PCF8576DUx	
SDA	10	44	1, 58 and 59	I^2C-bus serial data input and output
SCL	11	45	2 and 3	I^2C-bus serial clock input
CLK	13	47	5	external clock input or output
V_{DD}	14	48	6	supply voltage
$\overline{SYNC}$	12	46	4	cascade synchronization input or output
OSC	15	49	7	internal oscillator enable input
A0 to A2	16 to 18	50 to 52	8 to 10	subaddress inputs
SA0	19	53	11	I^2C-bus address input; bit 0
V_{SS}	20	54	12[1]	ground supply voltage
V_{LCD}	21	55	13	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	56, 1, 2, 3	14 to 17	LCD backplane outputs
S0 to S39	29 to 32, 34 to 47, 49 to 64, 2 to 7	4 to 43	18 to 57	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	not connected

[1] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

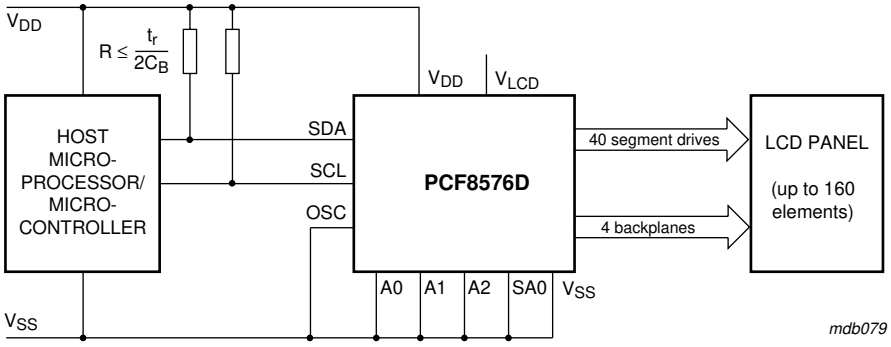
7. Functional description

The PCF8576D is a versatile peripheral device designed to interface any microprocessor or microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

The possible display configurations of the PCF8576D depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 4. All of these configurations can be implemented in the typical system shown in Figure 5.

Table 4. Display configurations

Number of:		7-segment numeric		14-segment numeric		Dot matrix
Backplanes	Segments	Digits	Indicator symbols	Characters	Indicator symbols	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)



The resistance of the power lines must be kept to a minimum.

For chip-on-glass applications, due to the Indium Tin Oxide (ITO) track resistance, each supply line must be routed separately between the chip and the connector.

Fig 5. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576D. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

7.1 Power-on reset

At power-on the PCF8576D resets to the following starting conditions:

- All backplane outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with ⅓ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I²C-bus interface is initialized
- The data pointer and the subaddress counter are cleared
- Display is disabled

Data transfers on the I²C-bus must be avoided for 1 ms following power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between V_{LCD} and V_{SS}. The middle resistor can be bypassed to provide a ½ bias voltage level for the 1:2 multiplex configuration. The LCD voltage can be temperature compensated externally using the supply to pin V_{LCD}.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see Section 7.17) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 5.

Table 5. Discrimination ratios

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with the equation

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{\frac{1}{n}+\left[(n-1)\times\left(\frac{1}{1+a}\right)\right]^2}{n}} \quad (1)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with the equation:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2-(2a+n)}{n\times(1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from the equation:

$$\frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

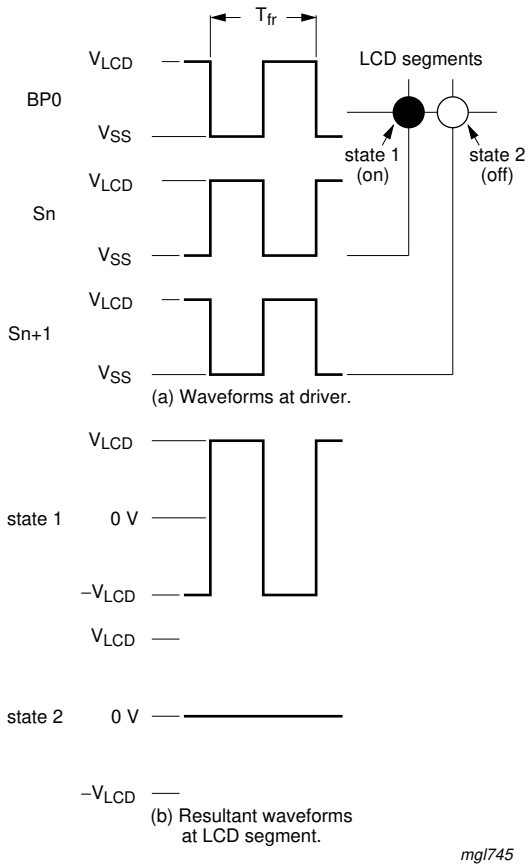
These compare with $V_{LCD} = 3 V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (S_n) waveforms for this mode are shown in Figure 6.



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = V_{LCD}$.

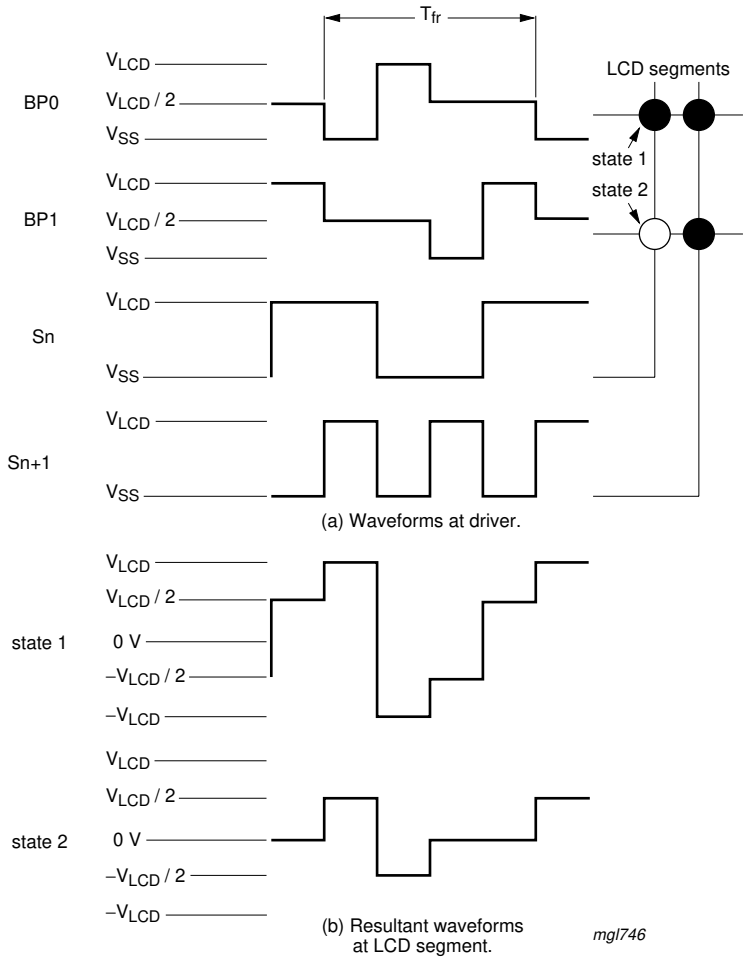
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

(4) $V_{off(RMS)} = 0$ V.

Fig 6. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 7 and Figure 8.



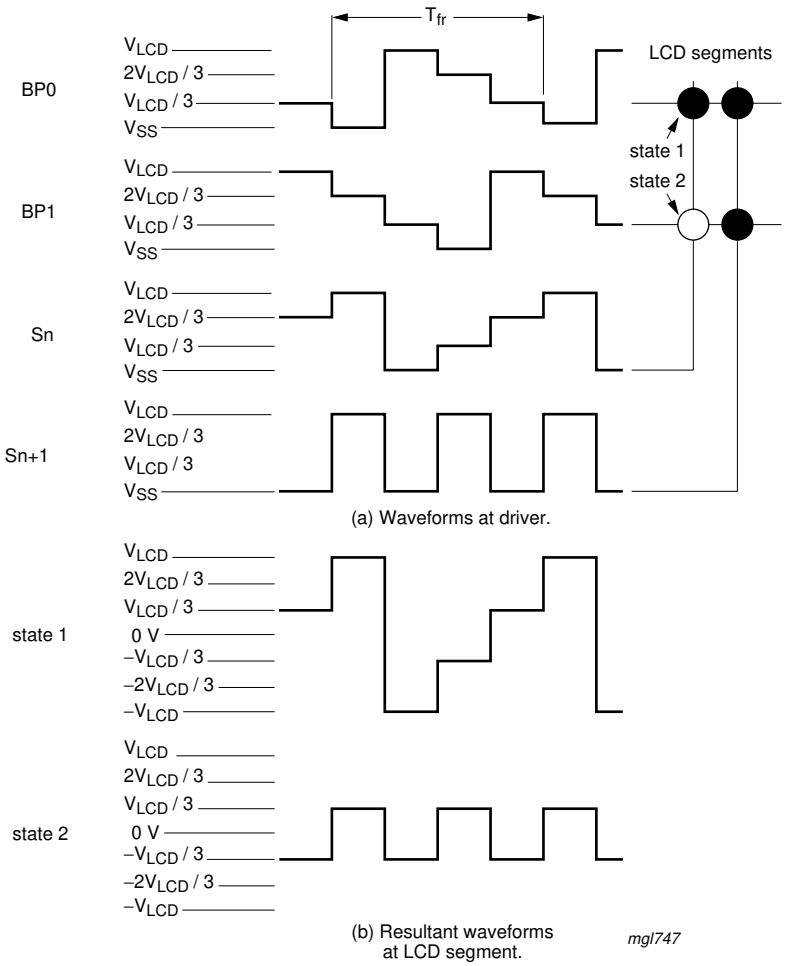
(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.791 V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.354 V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ½ bias



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.745V_{LCD}$.

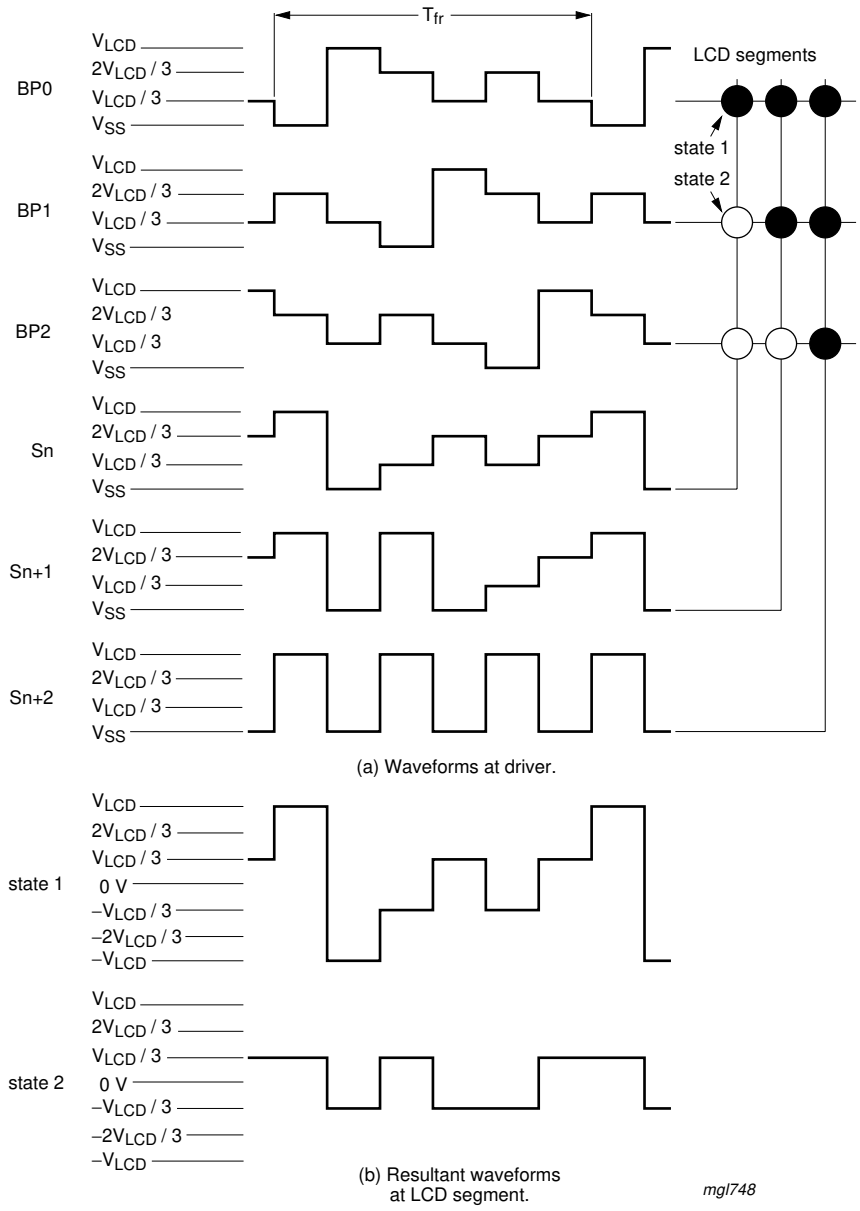
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with $^1/_3$ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies (see Figure 9).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.638V_{LCD}$.

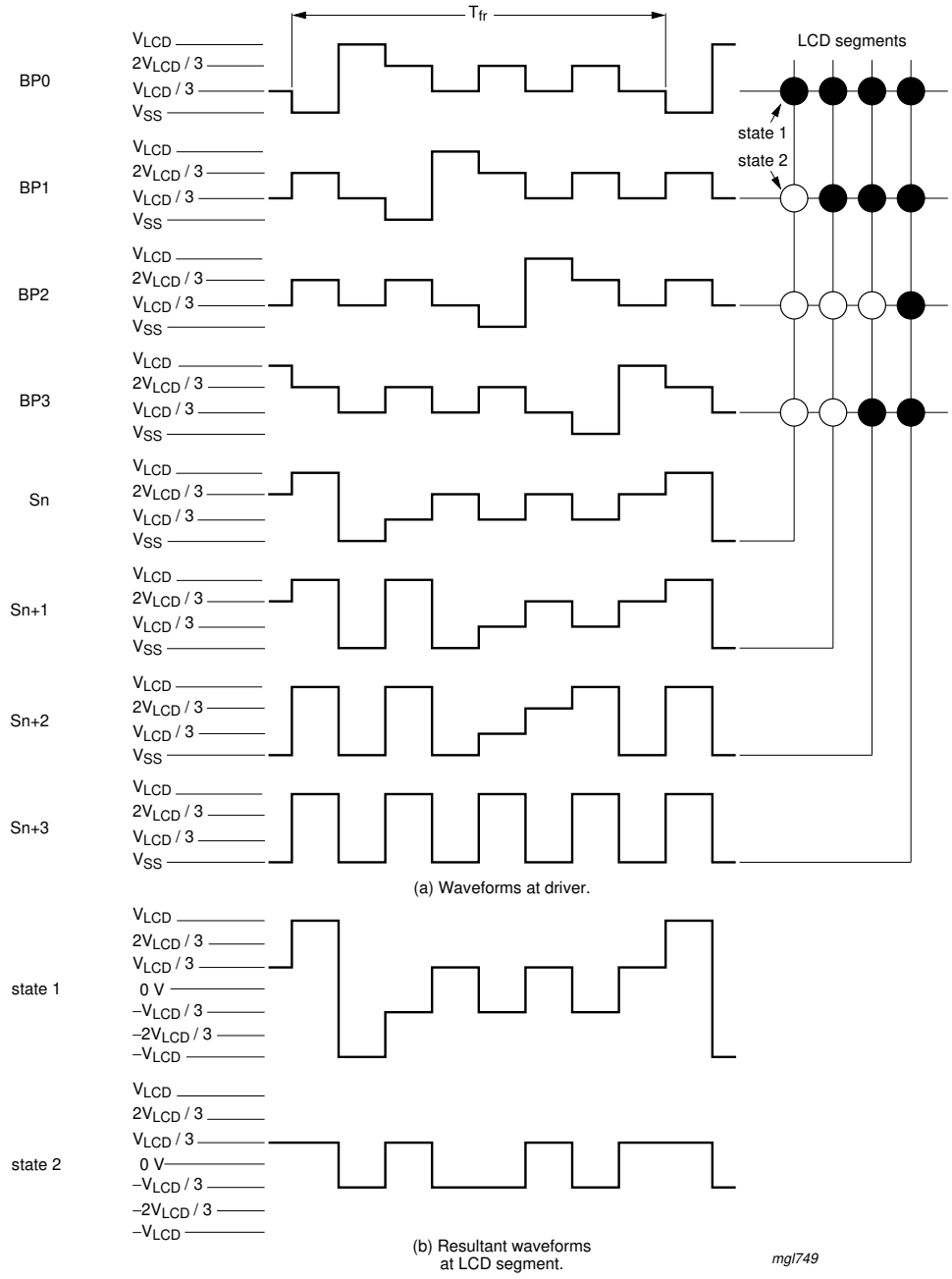
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:3 multiplex drive mode with $^1/_3$ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies (see Figure 10).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.577V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.5 Oscillator

7.5.1 Internal clock

The internal logic of the PCF8576D and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF8576Ds in the system that are connected in cascade. After power-on, pin SDA must be HIGH to guarantee that the clock starts.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

The LCD frame signal frequency is determined by the clock frequency (f_{clk}).

A clock signal must always be supplied to the device; removing the clock freezes the LCD in a DC state.

7.6 Timing

The PCF8576D timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF8576D in the system is maintained by the synchronization signal at pin $\overline{SYNC}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$.

7.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and each column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

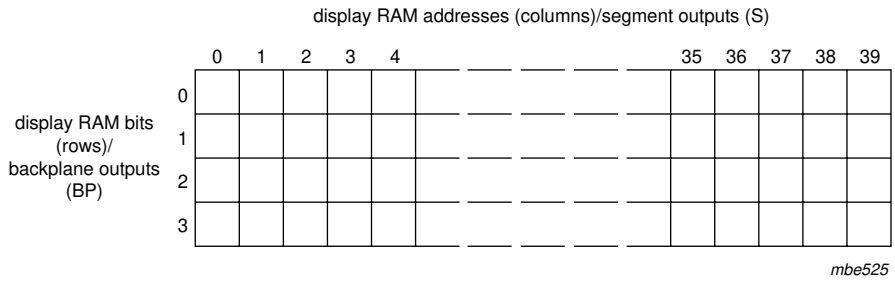
In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.

In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.

In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map Figure 11 shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3 respectively.



Display RAM bit map showing direct relationship between RAM addresses and segment outputs; also between bits in a RAM word and the backplane outputs.

Fig 11. Display RAM bit map

When display data is transmitted to the PCF8576D, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. For example, in the 1:2 mode, the RAM data is stored every second bit. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.

With reference to Figure 12, in the static drive mode, the eight transmitted data bits are placed in row 0 of eight successive display RAM addresses.

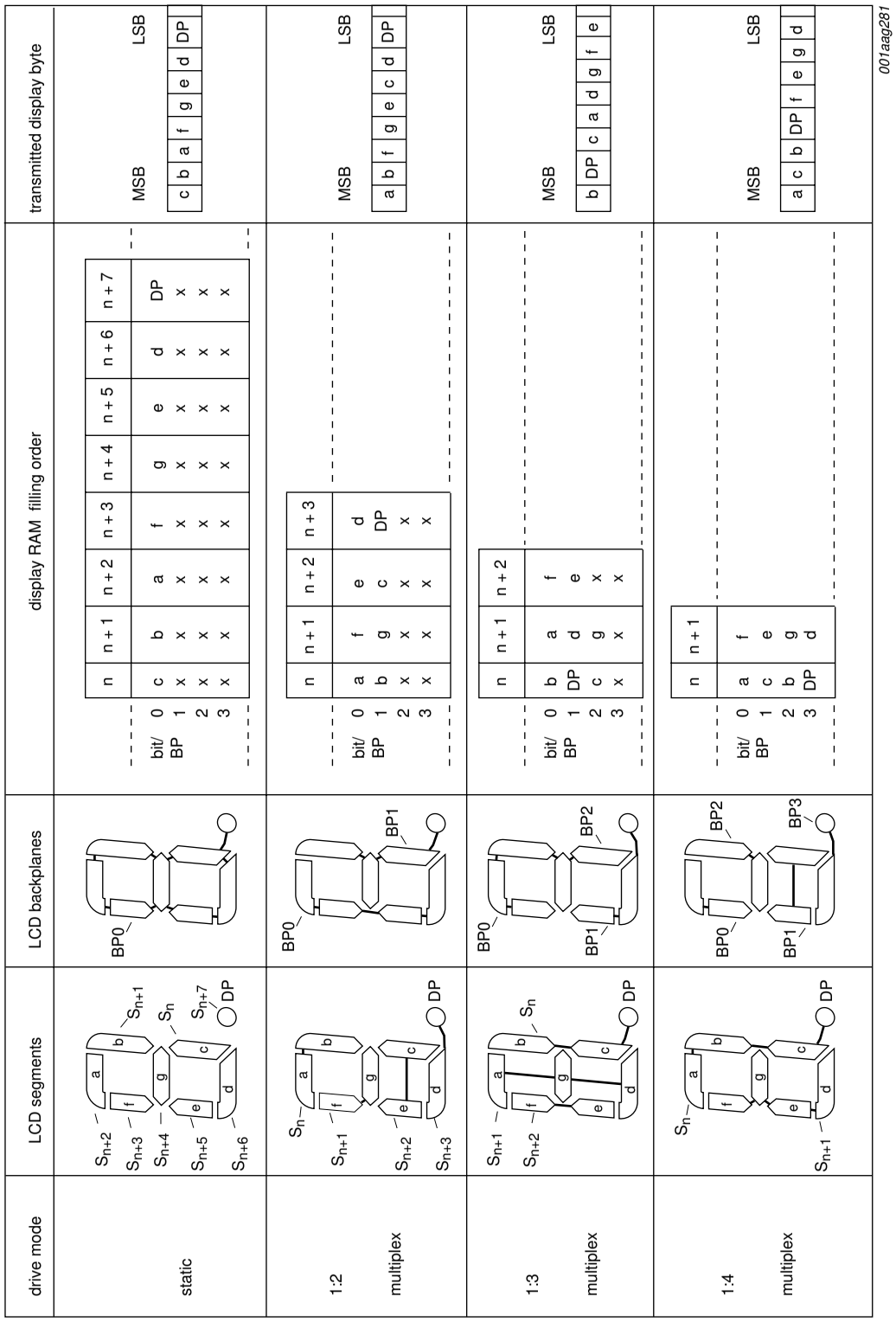
In the 1:2 mode, the eight transmitted data bits are placed in row 0 and 1 of four successive display RAM addresses.

In the 1:3 mode, these bits are placed in row 0, 1 and 2 to three successive addresses, display RAM words, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted; otherwise this segment should not be connected to the module.

In the 1:4 mode, the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Section 7.17). Following this, an arriving data byte is stored at the display RAM address indicated by the data pointer in accordance with the filling order shown in Figure 12. After each byte is stored, the contents of the data pointer are automatically incremented by a value dependent on the selected LCD drive mode: eight (static drive mode), four (1:2 mode), three (1:3 mode) or two (1:4 mode). If an I^2C-bus data access is terminated early then the state of the data pointer will be unknown. The data pointer should be re-written prior to further RAM access.



x = data bit unchanged.

Fig 12. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

7.12 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 mode, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3.
- In 1:3 mode, bits 0, 1 and 2 are selected sequentially
- In 1:2 mode, bits 0 and 1 are selected
- In static mode, bit 0 is selected

The $\overline{\text{SYNC}}$ signal resets these sequences to the following starting points:

- Bit 3 for 1:4 mode
- Bit 2 for 1:3 mode
- Bit 1 for 1:2 mode
- Bit 0 for static mode

The PCF8576D includes a RAM bank switching feature in the static and 1:2 drive modes. In the static drive mode, the bank-select command (see Section 7.17) may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.13 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration.

The bank-select command (see Section 7.17) can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

7.14 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device-select command (see Section 7.17). If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576D occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14^{th} display data byte transmitted in 1:3 mode).

The hardware subaddress must not be changed while the device is being accessed on the I²C-bus interface.

7.15 Blinker

The PCF8576D has a very versatile display blinking capability. The whole display can blink at a frequency selected by the blink-select command (see Section 7.17). Each blink frequency is a fraction of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected (see Table 6).

An additional feature allows an arbitrary selection of LCD segments to blink in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the blink-select command (see Section 7.17).

In the 1:3 and 1:4 drive modes, where no alternative RAM bank is available, groups of LCD segments can blink selectively by changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the mode-set command (see Section 7.17).

Table 6. Blinking frequencies[1]

Blink mode	Normal operating mode ratio	Nominal blink frequency
off	-	blinking off
1	$\frac{f_{clk}}{768}$	2 Hz
2	$\frac{f_{clk}}{1536}$	1 Hz
3	$\frac{f_{clk}}{3072}$	0.5 Hz

[1] Blink modes 1, 2 and 3 and the nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency (f_{clk}) of 1536 Hz (see Section 11).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 13).

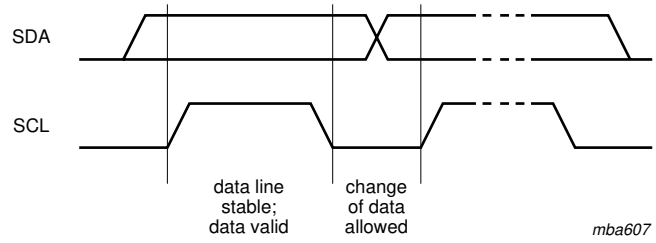


Fig 13. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 14).

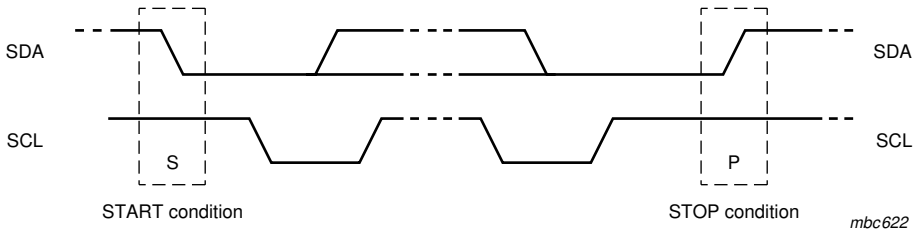


Fig 14. Definition of START and STOP conditions

7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 15).

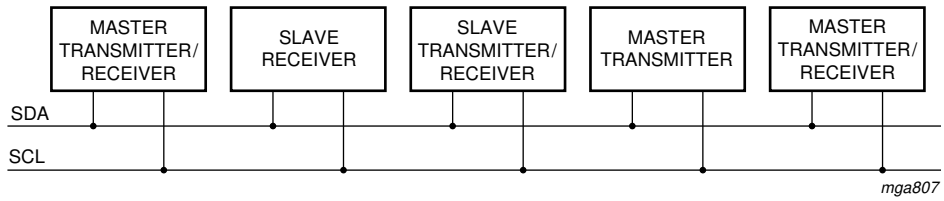


Fig 15. System configuration

7.16.4 Acknowledge

The number of data bytes that can be transferred from transmitter to receiver between the START and STOP conditions is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal on the bus that is asserted by the transmitter during which time the master generates an extra acknowledge related clock pulse. An addressed slave receiver must generate an acknowledge after receiving each byte. Also a master receiver must generate an acknowledge after receiving each byte that has been clocked out of the slave transmitter. The acknowledging device must pull-down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Figure 16).

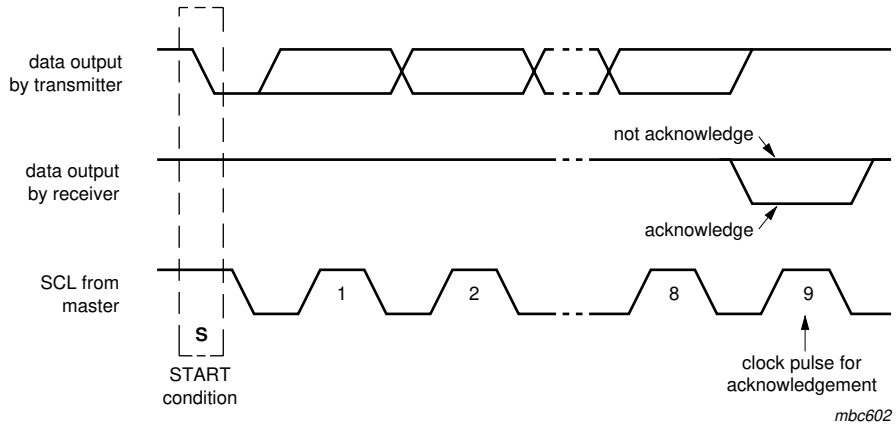


Fig 16. Acknowledgement of the I²C-bus

7.16.5 I²C-bus controller

The PCF8576D acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576D are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCF8576D. The least significant bit of the slave address that a PCF8576D will respond to is defined by the level tied to its SA0 input. The PCF8576D is a write-only device and will not respond to a read access. Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCF8576Ds for very large LCD applications
- The use of two types of LCD multiplex drive.

The I²C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCF8576D slave addresses available. All PCF8576Ds whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF8576Ds whose SA0 inputs are set to the alternative level.

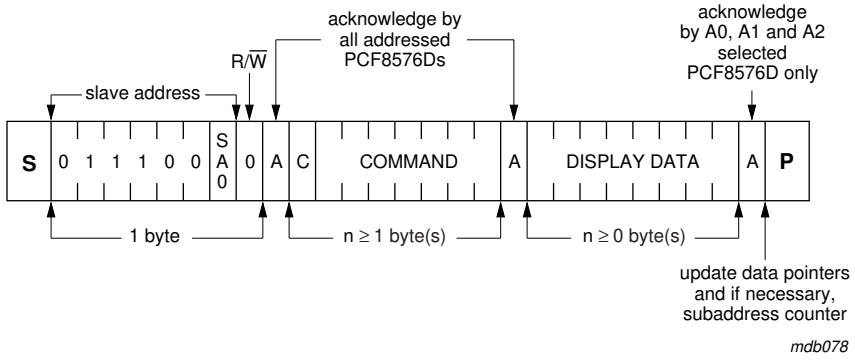


Fig 17. I²C-bus protocol

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCF8576D.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Figure 18). The command bytes are also acknowledged by all addressed PCF8576Ds on the bus.

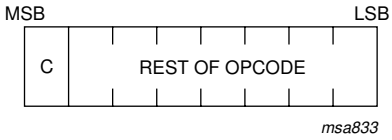


Fig 18. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCF8576D device.

An acknowledgement after each byte is asserted only by the PCF8576Ds that are addressed via address lines A0, A1 and A2. After the last display byte, the I^2C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I^2C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus.

The commands available to the PCF8576D are defined in Table 7.

Table 7. Definition of PCF8576D commands

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	[1]	E	B	M1	M0	Table 9
load-data-pointer	C	0	P5	P4	P3	P2	P1	P0	Table 10
device-select	C	1	1	0	0	A2	A1	A0	Table 11
bank-select	C	1	1	1	1	0	I	O	Table 12
blink-select	C	1	1	1	0	A	BF1	BF0	Table 13

[1] Not used.

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 18. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see Table 8).

Table 8. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too