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PCF8577C

LCD direct/duplex driver with I²C-bus interface

Rev. 5 — 10 October 2014 Product data sheet

1. General description

The PCF8577C is an LCD driver which drives up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).To allow partial V_{DD} shutdown, the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

For a selection of NXP LCD segment drivers, see Table 13 on page 25.

2. Features and benefits

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 V to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display
- I²C-bus address: 0111 0100.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158-1

3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF8577CT/3	PCF8577CT/3,112	935278866112	tube	3
PCF8577CT/3	PCF8577CT/3,118	935278866118	tape and reel, 13 inch	3

4. Marking

Table 3. Marking codes

Type number	Marking code
PCF8577CT/3	PCF8577CT

5. Block diagram

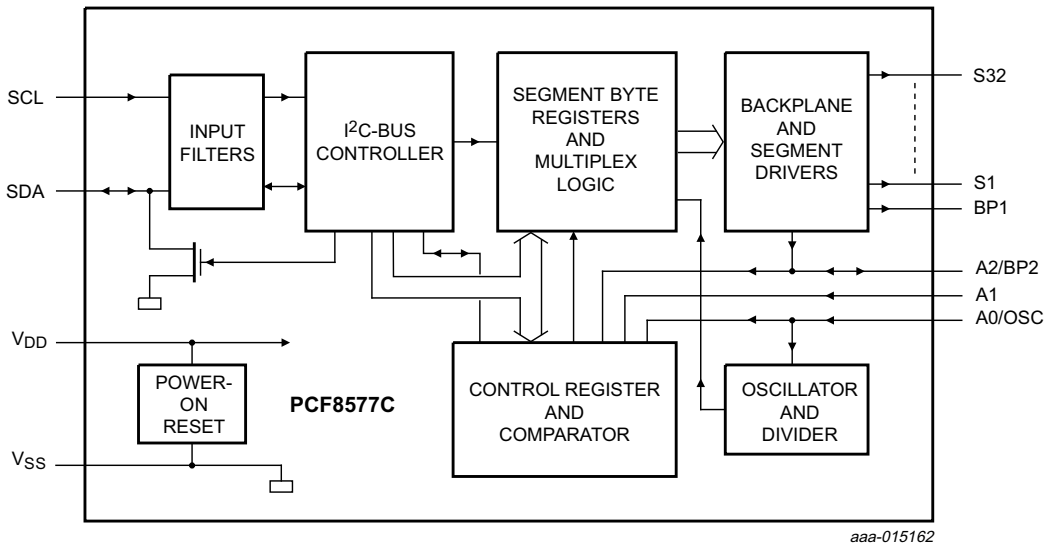


Fig 1. Block diagram of PCF8577C

6. Pinning information

6.1 Pinning

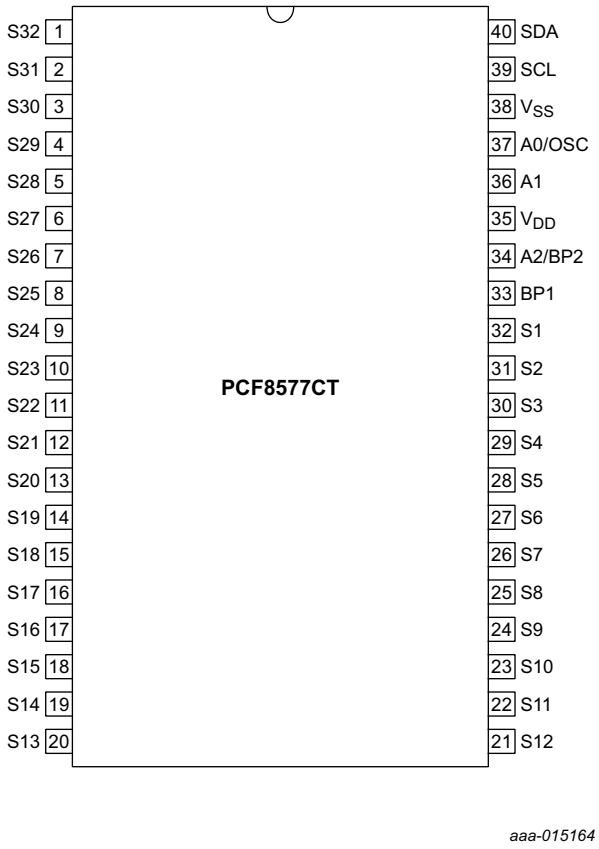


Fig 2. Pin configuration for PCF8577CT

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
S32 to S1	1 to 32	outputs	segment outputs
BP1	33	input/output	cascaded sync input/backplane output
A2/BP2	34	input/output	hardware address line and cascade sync input/backplane output
V_{DD}	35	supply	supply voltage
A1	36	input	hardware address line input
A0/OSC	37	input	hardware address line and oscillator pin input
V_{SS}	38	supply	ground supply
SCL	39	input	I²C-bus clock line input
SDA	40	input/output	I²C-bus data line input/output

7. Functional description

7.1 Hardware subaddress lines A0, A1, and A2

The hardware subaddress lines A0, A1, and A2 are used to program the device subaddress for each PCF8577C connected to the I²C-bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pinout requirements.

1. Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.
2. Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.
3. In the direct drive mode, the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.
4. In the duplex drive mode, the second backplane signal BP2 is required and the A2 signal is undefined. In this mode, device selection is made exclusively from lines A0 and A1.

7.2 Oscillator A0/OSC

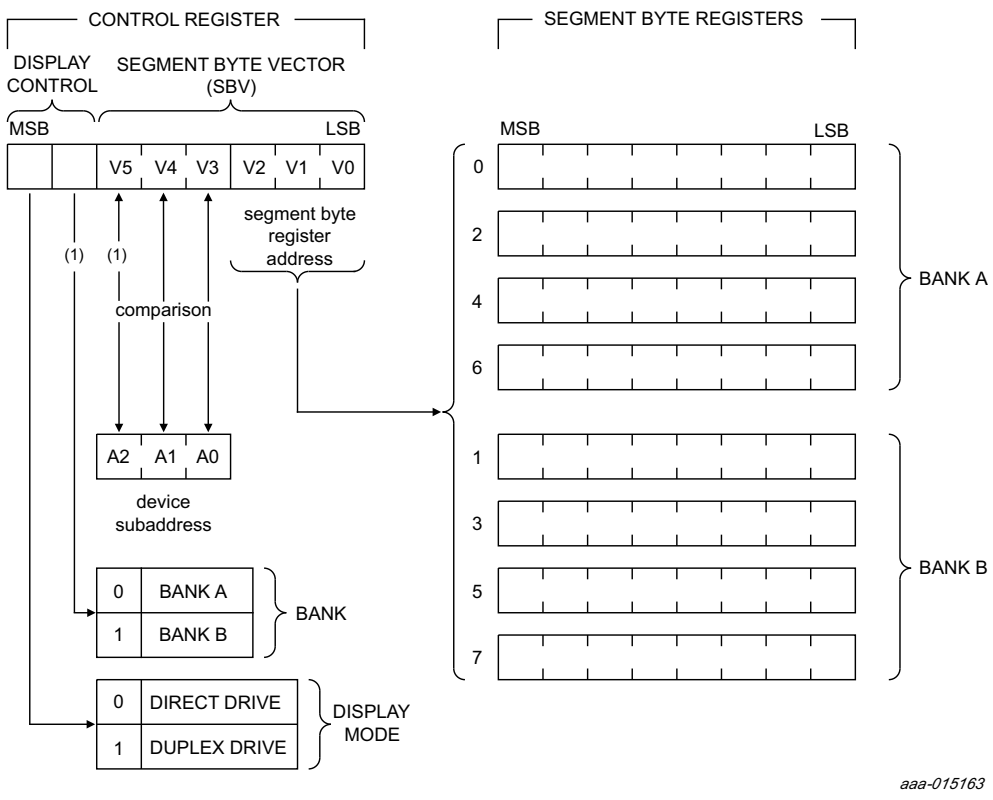
The PCF8577C has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator (see Figure 13 and Figure 14). For correct start-up of the oscillator after power-on, the resistor and capacitor must be connected to the same V_{SS}/V_{DD} as the chip. In an expanded system containing more than one PCF8577C the backplane signals are usually common to all devices and only one oscillator is required. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode, each PCF8577C is synchronized from the backplane signals.

7.3 User-accessible registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even-numbered segment byte registers is called BANK A. Odd-numbered segment byte registers are called BANK B.

There is one slave address for the PCF8577C (see Table 7). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register always (see I²C-bus protocol, Figure 10), i.e. all addressed devices respond to control commands sent on the I²C-bus.

The control register is shown in more detail in Figure 3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).



(1) Bits ignored in duplex mode.

Fig 3. PCF8577C register organization

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same, then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

7.4 Auto-incremented loading

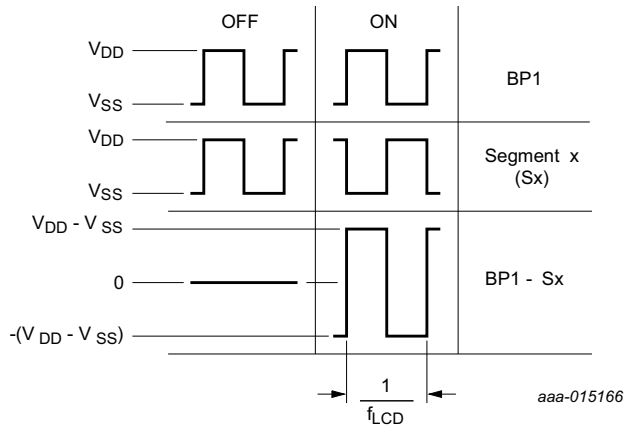
After each segment byte is loaded, the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries if the hardware subaddresses are arranged contiguously.

7.5 Direct drive mode

The PCF8577C is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode, only four bytes are required to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A), setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode, the SBV is auto-incremented by two after the loading of each segment byte register. This means, that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Figure 4.



$V_{on(RMS)} = V_{DD} - V_{SS}$; $V_{off(RMS)} = 0$.

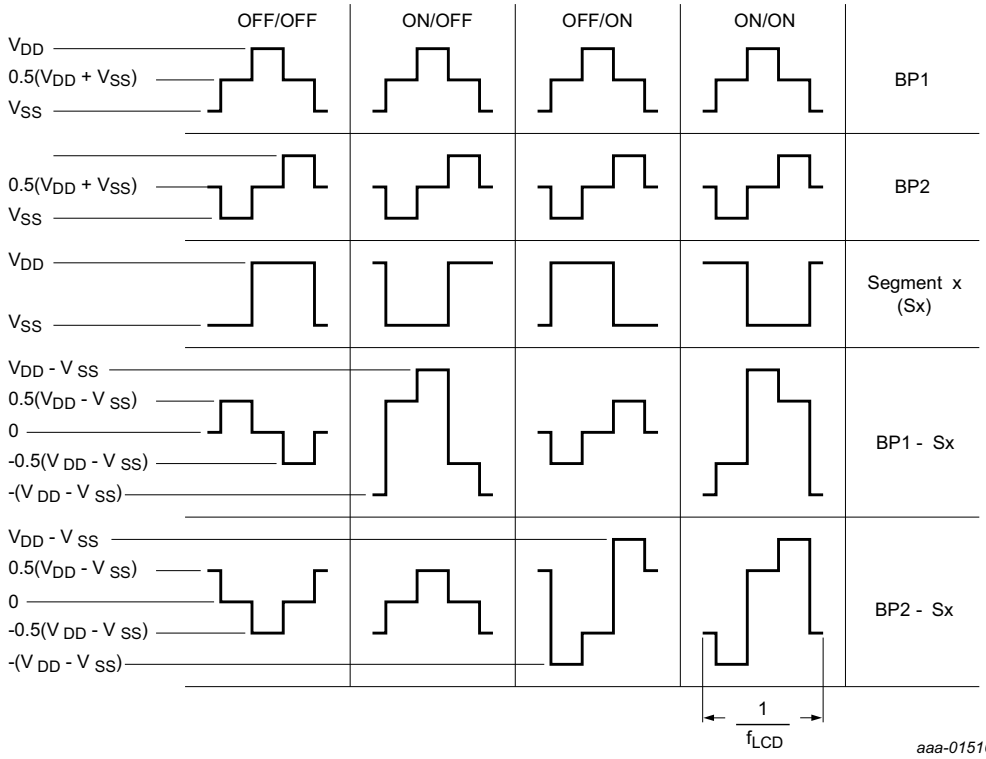
Fig 4. Direct drive mode display output waveforms

7.6 Duplex mode

The PCF8577C is set to the duplex mode by loading the MODE bit with logic 1. In this mode, a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are required to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Figure 5.



$V_{on(RMS)} = 0.791(V_{DD} - V_{SS})$; $V_{off(RMS)} = 0.354(V_{DD} - V^{SS})$.

Fig 5. Duplex mode display output waveforms

7.7 Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is given in Table 5 and Table 6.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0, even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode. In duplex mode, even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 5. Segment byte-segment driver mapping in direct drive mode

Mode	Bank	V2	V1	V0	Segment/ Bit/ Register	7 MSB	6	5	4	3	2	1	0 LSB	Backplane
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

Table 6. Segment byte-segment driver mapping in duplex mode

Mode	Bank	V2	V1	V0	Segment/ Bit/ Register	7 MSB	6	5	4	3	2	1	0 LSB	Backplane
1	X[1]	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	X[1]	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	X[1]	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	X[1]	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	X[1]	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	X[1]	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	X[1]	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	X[1]	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

[1] Don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

7.8 Power-on reset

At power-on reset the PCF8577C resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode
2. All segment outputs are set to V_{SS}
3. The segment byte registers and control register are cleared
4. The I²C-bus interface is initialized.

8. I²C-bus interface

8.1 Characteristics of the I²C-Bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the I²C-bus is not busy.

8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals.

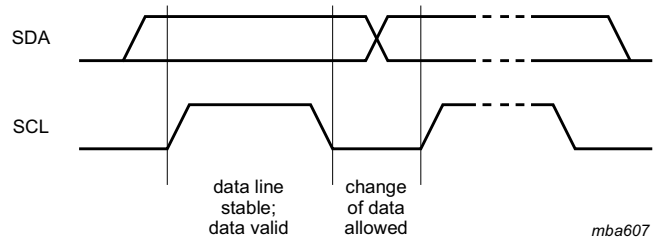


Fig 6. Bit transfer

8.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the I²C-bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

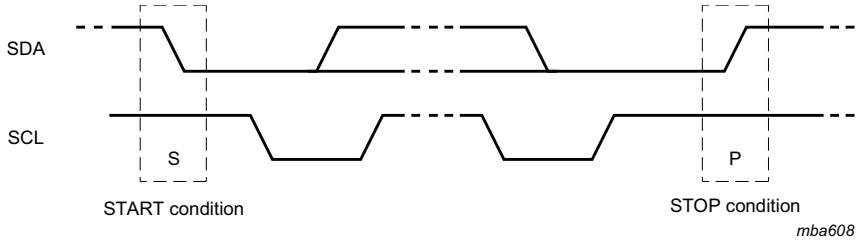


Fig 7. Definition of START and STOP conditions

8.1.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

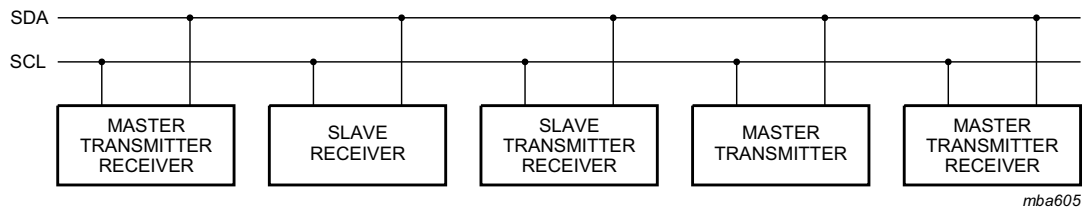


Fig 8. System configuration

8.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the I²C-bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

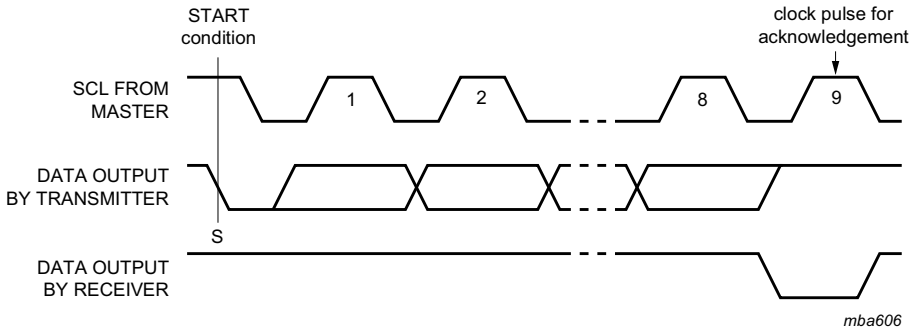


Fig 9. Acknowledgement of the I²C-bus

8.2 Slave address

The PCF8577C slave address is shown in Table 7.

Table 7. I²C slave address byte

	Slave address							R/$\overline{W}$
Bit	**7 MSB**	**6**	**5**	**4**	**3**	**2**	**1**	**0 LSB**
	0	1	1	1	0	1	0	0

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

8.3 I²C-bus protocol

The PCF8577C I²C-bus protocol is shown in Figure 10.

The PCF8577C is a slave receiver and has a fixed slave address (see Table 7). All PCF8577Cs with the same slave address acknowledge the slave address in parallel.

The second byte is always the control byte and is loaded into the control register of each PCF8577C connected to the I²C-bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a STOP (P) condition is given after the control byte acknowledge, the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data, only the selected PCF8577C gives an acknowledge. Loading is terminated by generating a STOP (P) condition.

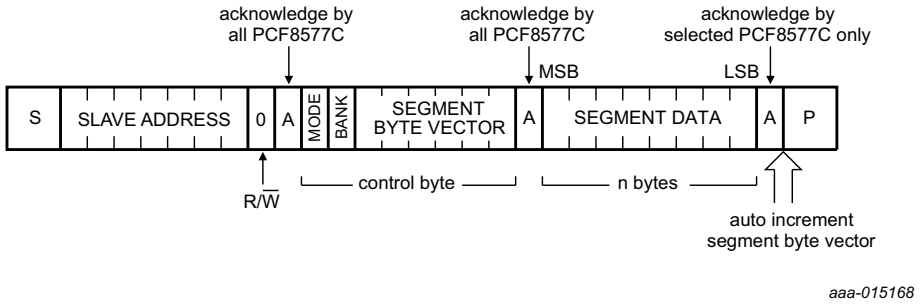


Fig 10. I²C-bus protocol

9. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

10. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+8.0	V
V_{LCD}	LCD supply voltage	[1]	V_{DD} − 8.0	V_{DD}	V
V_I	input voltage		−0.5	V_{DD} + 0.5	V
V_O	output voltage	on each of the pins S1 to S32 and BP1 and BP2 [1]	−0.5	+8.0	V
I_I	input current		−20	+20	mA
I_O	output current		−25	+25	mA
I_{DD}	supply current		−50	+50	mA
I_{SS}	ground supply current		−50	+50	mA
$I_{DD(LCD)}$	LCD supply current		−50	+50	mA
P_{tot}	total power dissipation		-	500	mW
P_o	output power		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM [2]	-	±2000	V
		MM [3]	-	±200	V
I_{lu}	latch-up current	[4]	-	100	mA
T_{stg}	storage temperature	[5]	−65	+150	°C
T_{amb}	ambient temperature	operating device	−40	+85	°C

[1] Values with respect to V_{DD}.

[2] Pass level; Human Body Model (HBM), according to Ref. 6 “JESD22-A114”.

[3] Pass level; Machine Model (MM), according to Ref. 7 “JESD22-A115”.

[4] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[5] According to the store and transport requirements (see Ref. 12 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

11. Static characteristics

Table 9. Static characteristics

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to 85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.5	-	6	V
I_{DD}	supply current	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF [1]				
		f_{SCL} = 100 kHz [1]	-	50	125	μA
		f_{SCL} = 0 Hz [1]	-	25	75	μA
		V_{DD} = 5 V; T_{amb} = 25 °C [1]	-	25	40	μA
		no load; f_{SCL} = 0 Hz; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C [1]	-	10	20	μA
V_{POR}	power-on reset voltage	[2]	-	1.1	2.0	V
Logic						
V_{IL}	LOW-level input voltage	on pin A0	0	-	0.05	V
		on pins A1, SCL, SDA	0	-	$0.3V_{DD}$	V
		on pin A2	0	-	0.1	V
V_{IH}	HIGH-level input voltage	on pin A0	V_{DD} − 0.05	-	V_{DD}	V
		on pin A1	$0.7V_{DD}$	-	V_{DD}	V
		on pin A2	V_{DD} − 0.1	-	V_{DD}	V
		on pins SCL, SDA	$0.7V_{DD}$	-	6	V
C_I	input capacitance	[3]	-	-	7	pF
I_{OL}	LOW-level output current	output sink current; on pin SDA; V_{OL} = 0.4 V; V_{DD} = 5 V;	3	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}				
		on pins A1, SCL, SDA	−1	-	+1	μA
		on pins A2/BP2, BP1	−5	-	+5	μA
		$V_I = V_{DD}$; on pin A0/OSC	−1	-	-	μA
I_{pd}	pull-down current	$V_I = V_{DD}$; on pin A2/BP2	−5	−1.5	-	μA
$I_{startup}$	startup current	oscillator; $V_I = V_{SS}$	-	1.2	5	μA

Table 9. Static characteristics *...continued*

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to 85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LCD outputs						
V_{DC}	DC component of LCD driver		-	±20	-	mV
I_{OL}	LOW-level output current	on pins S1 to S32; [4] V_{DD} = 5 V; V_{OL} = 0.8 V	0.3	-	-	mA
I_{OH}	HIGH-level output current	on pins S1 to S32; [4] V_{DD} = 5 V; V_{OH} = V_{DD} − 0.8 V	-	-	−0.3	mA
R_o	output resistance	on pins BP1, BP2; [5] V_o = V_{SS} or V_{DD} or ½(V_{SS} + V_{DD})	-	0.4	5	kΩ

[1] Inputs at V_{SS} or V_{DD}.

[2] Resets all logic when V_{DD} < V_{POR}.

[3] Periodically sampled, not 100 % tested.

[4] Outputs measured one at a time.

[5] Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.

12. Dynamic characteristics

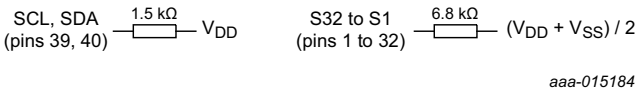
Table 10. Dynamic characteristics

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to 85 °C; unless otherwise specified. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{LCD}	display frequency	R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	65	90	120	Hz
t_{BS}	driver delays with test loads	V_{DD} = 5 V [2]	-	20	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{SW}	tolerable spike width on I²C-bus	T_{amb} = 25 °C	-	-	100	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.0	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	-	µs
t_r	rise time of both SDA and SCL signals		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	-	µs

[1] Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

[2] Test loads:.



aaa-015184

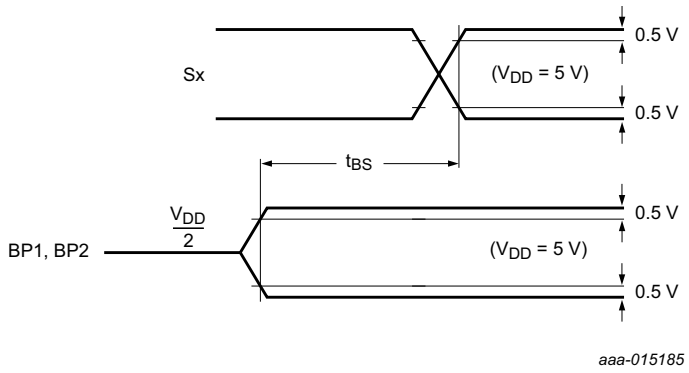


Fig 11. Driver timing waveforms

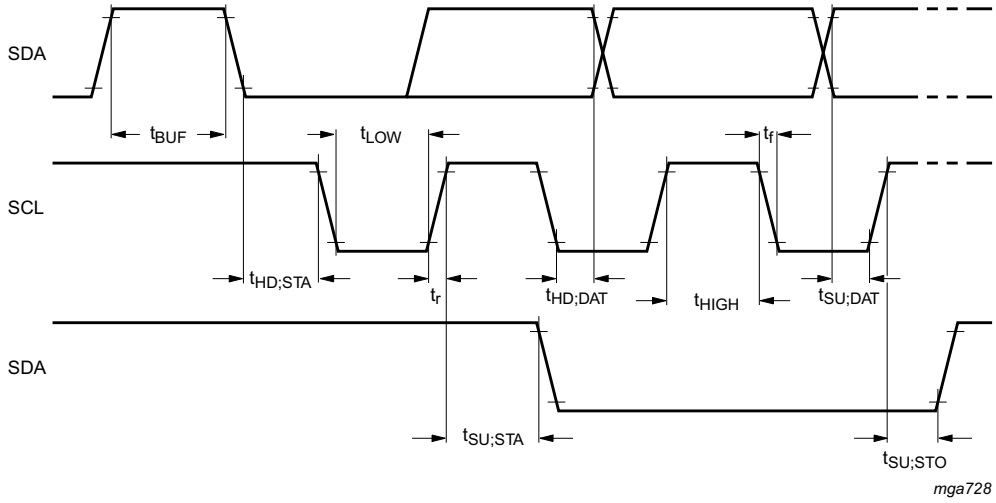


Fig 12. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

13. Application information

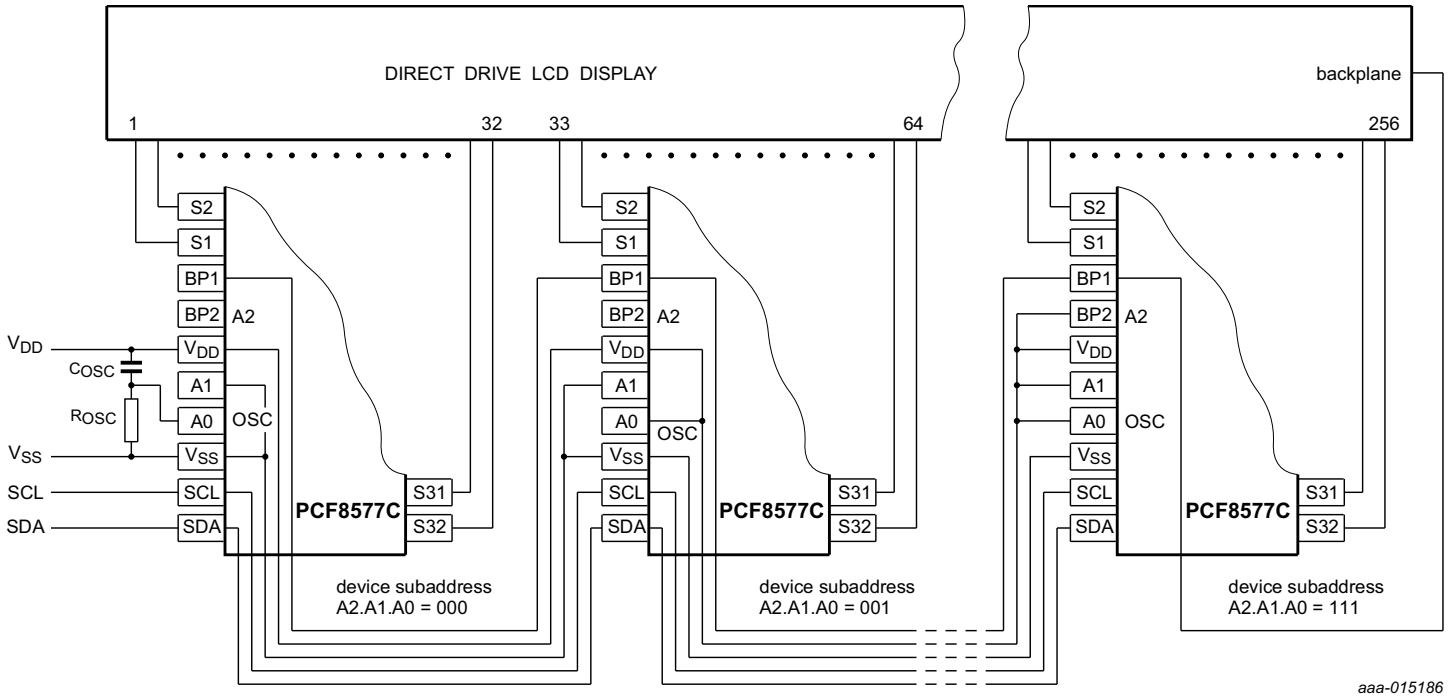


Fig 13. Direct display driver; expansion to 256 segments using eight PCF8577Cs

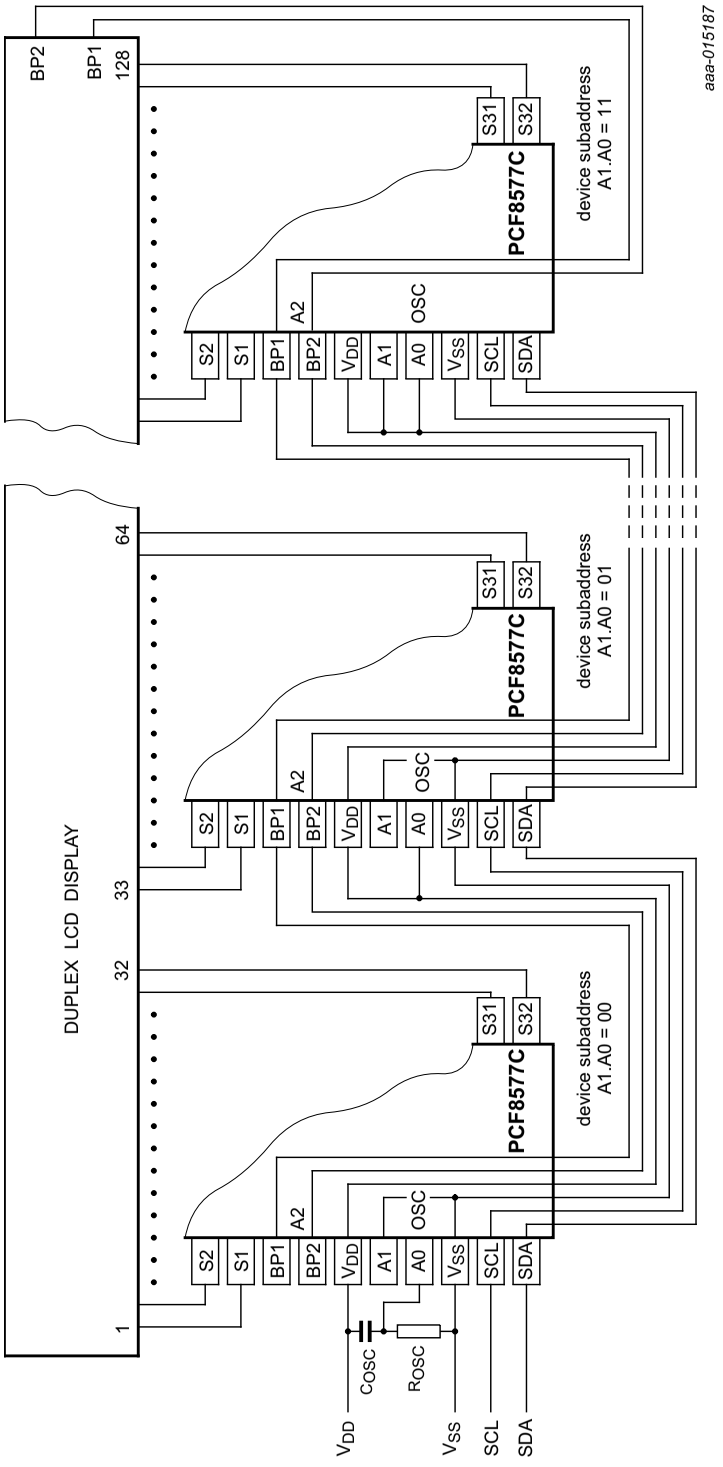
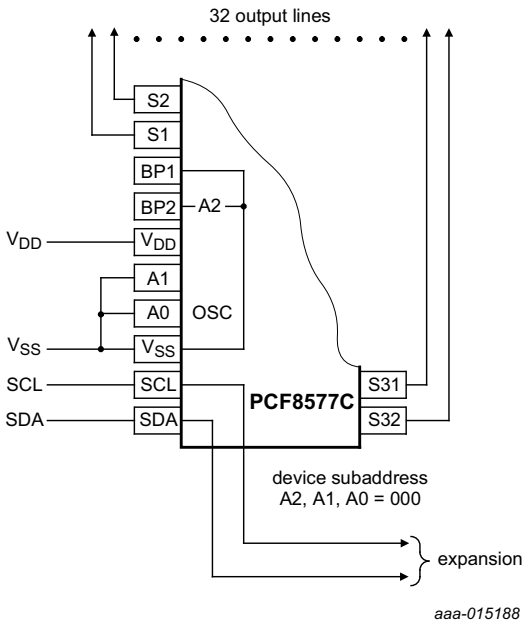


Fig 14. Duplex display; expansion to 2 × 128 segments using four PCF8577Cs



MODE bit must always be set to logic 0 (direct drive).

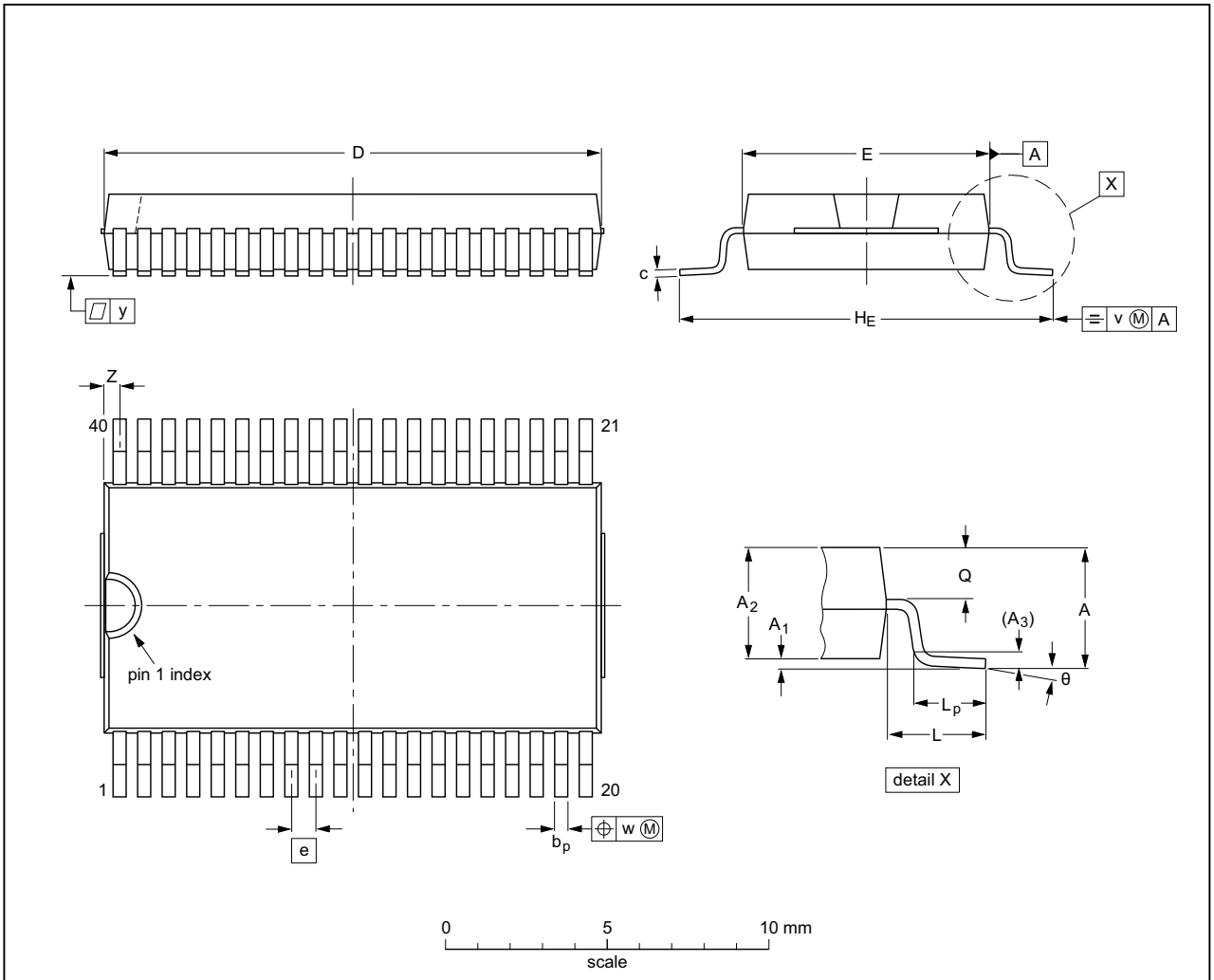
Bank switching is permitted.

BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig 15. Use of PCF8577C as a 32-bit output expander in an I²C-bus application

14. Package outline

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.7	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.01	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm (0.016 inch) maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT158-1						~~95-01-24~~ 03-02-19

Fig 16. Package outline SOT158-1 (VSO40) of PCF8577CT

15. Packing information

15.1 Tape and reel information

For tape and reel packing information, see Ref. 10 “SOT158-1_118” on page 27.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020D)

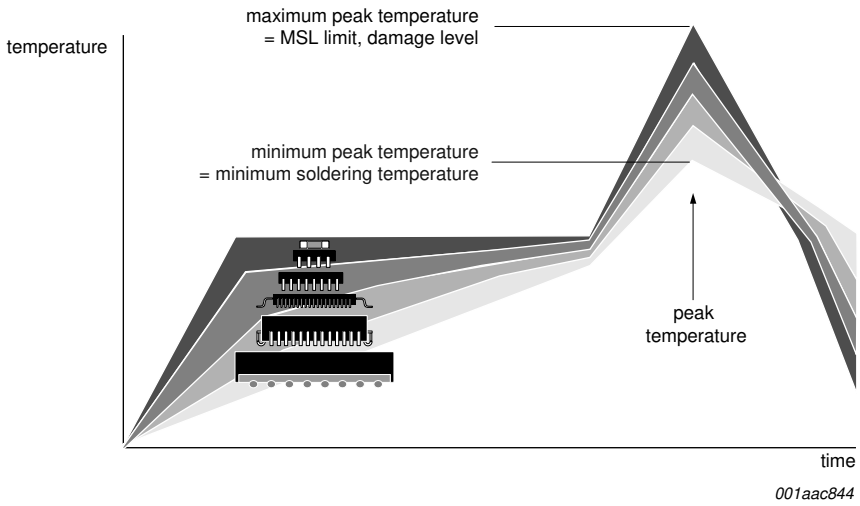
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



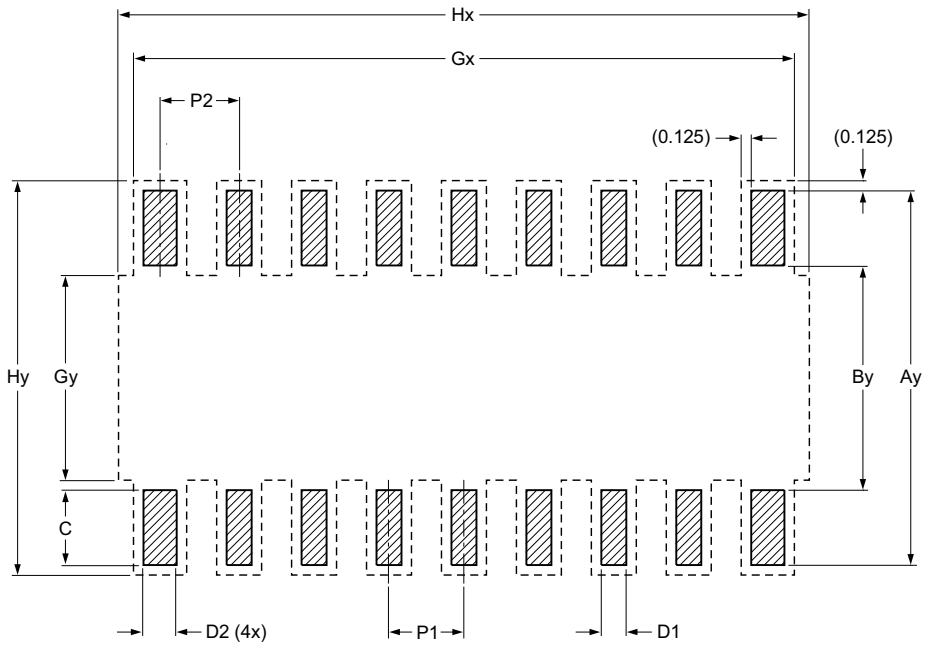
MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

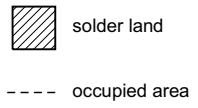
17. Footprint information

Footprint information for reflow soldering of VSO40 package **SOT158-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.760	0.835	12.700	8.300	2.200	0.450	0.600	15.440	8.100	16.100	12.950

sot158-1_fr

Fig 18. Footprint information for reflow soldering of SOT158-1 (VSO40) of PCF8577CT

18. Appendix

18.1 LCD segment driver selection

Table 13. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8553DTT	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	−40 to 105	I²C / SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	−40 to 95	I²C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	−40 to 95	SPI	TSSOP56	Y
PCA8547AHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 95	I²C	TQFP64	Y
PCA8547BHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	−40 to 85	I²C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	−40 to 95	I²C	LQFP80	Y
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 105	I²C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	−40 to 85	I²C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	−40 to 85	SPI	TSSOP56	N
PCF8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	−40 to 85	I²C	TSSOP56	N
PCF8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	−40 to 85	SPI	TSSOP56	N
PCA8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	−40 to 95	I²C	TSSOP56	Y
PCA8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	−40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 85	I²C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 95	I²C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 105	I²C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	−40 to 105	I²C	Bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	−40 to 85	I²C	Bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	−40 to 85	I²C	Bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	−40 to 105	I²C	Bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	−40 to 85	I²C	Bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	−40 to 95	I²C	Bare die	Y