Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

DATA SHEET

I²C
BUS

PCF8578

LCD row/column driver for dot matrix graphic displays

Product specification

Supersedes data of 1998 Sep 08

2003 Apr 14

PHILIPS

PHILIPS

LCD row/column driver for dot matrix graphic displays

PCF8578

CONTENTS

| LCD row/column driver for dot matrix graphic displays | PCF8578 |

1 FEATURES

- Single chip LCD controller/driver

- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)

- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns

- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32

- Externally selectable bias configuration, 5 or 6 levels

- 1280-bit RAM for display data storage and scratch pad

- Display memory bank switching

- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)

- Provides display synchronization for PCF8579

- On-chip oscillator, requires only 1 external resistor

- Power-on reset blanks display

- Logic voltage supply range 2.5 to 6 V

- Maximum LCD supply voltage 9 V

- Low power consumption

- I²C-bus interface

- TTL/CMOS compatible

- Compatible with most microcontrollers

- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)

- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack

- Compatible with chip-on-glass technology.

2 APPLICATIONS

- Automotive information systems

- Telecommunication systems

- Point-of-sale terminals

- Computer terminals

- Instrumentation.

3 GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U/2	–	chip with bumps in tray	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

LCD row/column driver for
dot matrix graphic displays

PCF8578

5 BLOCK DIAGRAM

C39 - C32
R31/C31 - R8/C8
R7 - R0

17 - 56
(29 to 35, 37, 38 to 46
48 to 62, 63, 64, 1 to 6)

V_{DD} 9 (20)
V_2 10 (21)
V_3 11 (22)
V_4 12 (23)
V_5 13 (24)
V_{LCD} 14 (25)
TEST 6 (12)

ROW/COLUMN [(1)]
DRIVERS

PCF8578

DISPLAY
MODE
CONTROLLER

OUTPUT
CONTROLLER

Y DECODER
AND SENSING
AMPLIFIERS

32 x 40-BIT
DISPLAY RAM

DISPLAY
DECODER

X DECODER

POWER-ON
RESET

SUBADDRESS
COUNTER

RAM DATA POINTER
Y   X

TIMING
GENERATOR

(9) 3 → $\overline{SYNC}$
(10) 4 → CLK

SCL 2 (8)
SDA 1 (7)

INPUT
FILTERS

I²C-BUS
CONTROLLER

COMMAND
DECODER

OSCILLATOR

(16) 8 → OSC
R_{OSC}
(11) 5 → V_{SS}

15, 16

(14, 15, 17 to 19
26 to 28 36, 47)

7 (13)

n.c.   n.c.   SA0

MSA842

(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

6   PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

SDA	1	56	R0
SCL	2	55	R1
$\overline{SYNC}$	3	54	R2
CLK	4	53	R3
V_{SS}	5	52	R4
TEST	6	51	R5
SA0	7	50	R6
OSC	8	49	R7
V_{DD}	9	48	R8/C8
V_2	10	47	R9/C9
V_3	11	46	R10/C10
V_4	12	45	R11/C11
V_5	13	44	R12/C12
V_{LCD}	14	43	R13/C13
n.c.	15	42	R14/C14
n.c.	16	41	R15/C15
C39	17	40	R16/C16
C38	18	39	R17/C17
C37	19	38	R18/C18
C36	20	37	R19/C19
C35	21	36	R20/C20
C34	22	35	R21/C21
C33	23	34	R22/C22
C32	24	33	R23/C23
R31/C31	25	32	R24/C24
R30/C30	26	31	R25/C25
R29/C29	27	30	R26/C26
R28/C28	28	29	R27/C27

PCF8578T

MSA839
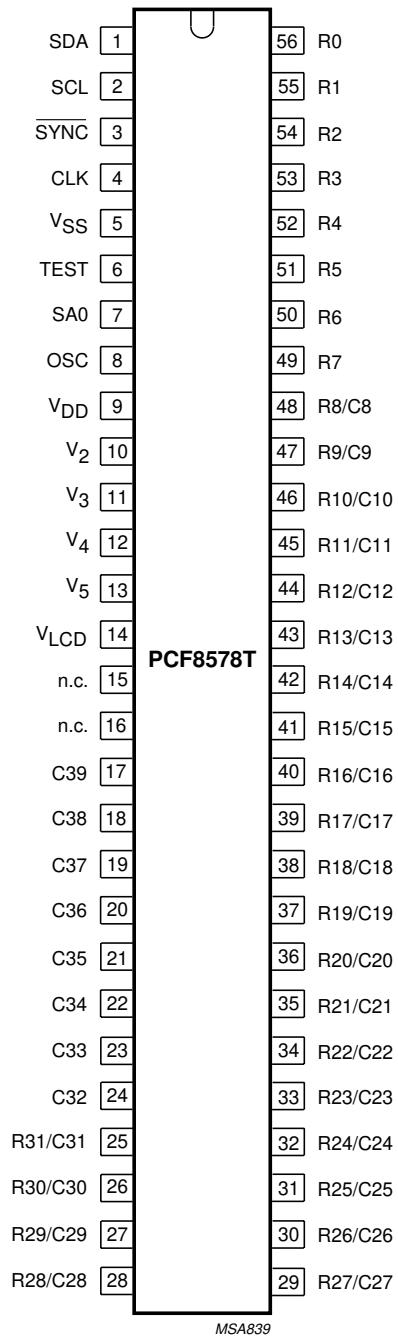
Fig.2 Pin configuration (VSO56).

LCD row/column driver for
dot matrix graphic displays   PCF8578
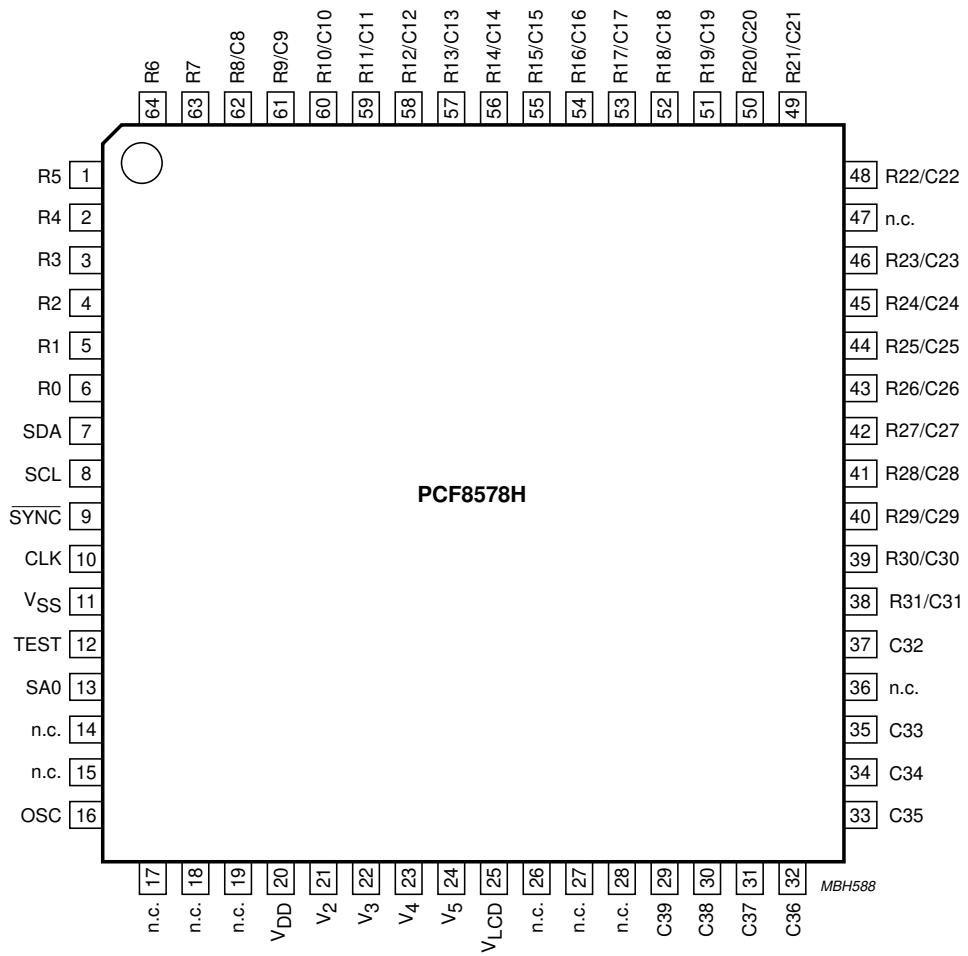
Fig.3 Pin configuration (LQFP64).

7 FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (mixed mode).

7.1 Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See Table 1 for common display configurations.

7.2 Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^{2}C-bus from the host microcontroller set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.5 (a stand-alone system would be identical but without the PCF8579s).

Table 1 Possible displays configurations

APPLICATION	MULTIPLEX RATE	MIXED MODE		ROW MODE		TYPICAL APPLICATIONS
		ROWS	COLUMNS	ROWS	COLUMNS	
Stand alone	1 : 8	8	32	–	–	small digital or alphanumerical displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
With PCF8579	1 : 8	8[1]	632[1]	8 × 4[2]	640[2]	alphanumeric displays and dot matrix graphic displays
	1 : 16	16[1]	624[1]	16 × 2[2]	640[2]	
	1 : 24	24[1]	616[1]	24[2]	640[2]	
	1 : 32	32[1]	608[1]	24[2]	640[2]	

Notes

1. Using 15 PCF8579s.

2. Using 16 PCF8579s.

7.3 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}. Figure 4 shows the first 4 rows of Table 2 as graphs. Table 3 shows the relative values of the resistors required in the configuration of Fig.5 to produce the standard multiplex rates.

Table 2 Optimum LCD voltages

PARAMETER	MULTIPLEX RATE			
	1 : 8	**1 : 16**	**1 : 24**	**1 : 32**
$\dfrac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\dfrac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\dfrac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\dfrac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\dfrac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\dfrac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \dfrac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\dfrac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190

Table 3 Multiplex rates and resistor values for Fig.5

RESISTORS	MULTIPLEX RATE (n)	
	n = 8	**n = 16, 24, 32**
R1	R	R
R2	$(\sqrt{n} - 2)R$	R
R3	$(3 - \sqrt{n})R$	$(\sqrt{n} - 3)R$

7.4 Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1 : 32 multiplex rate, row mode
3. Start bank, 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I²C-bus interface is initialized.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

$V_{bias} = V_2, V_3, V_4, V_5$. See Table 2.

Fig.4 V_{bias}/V_{op} as a function of the multiplex rate.
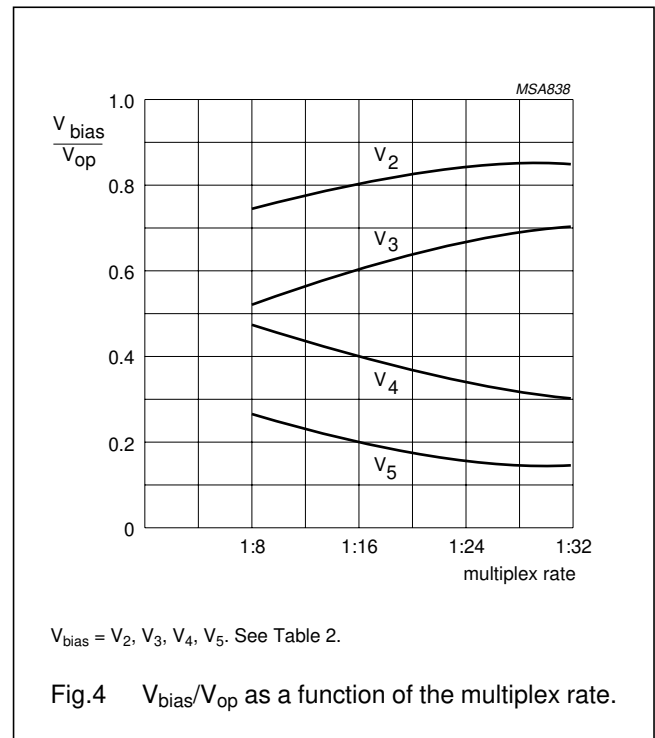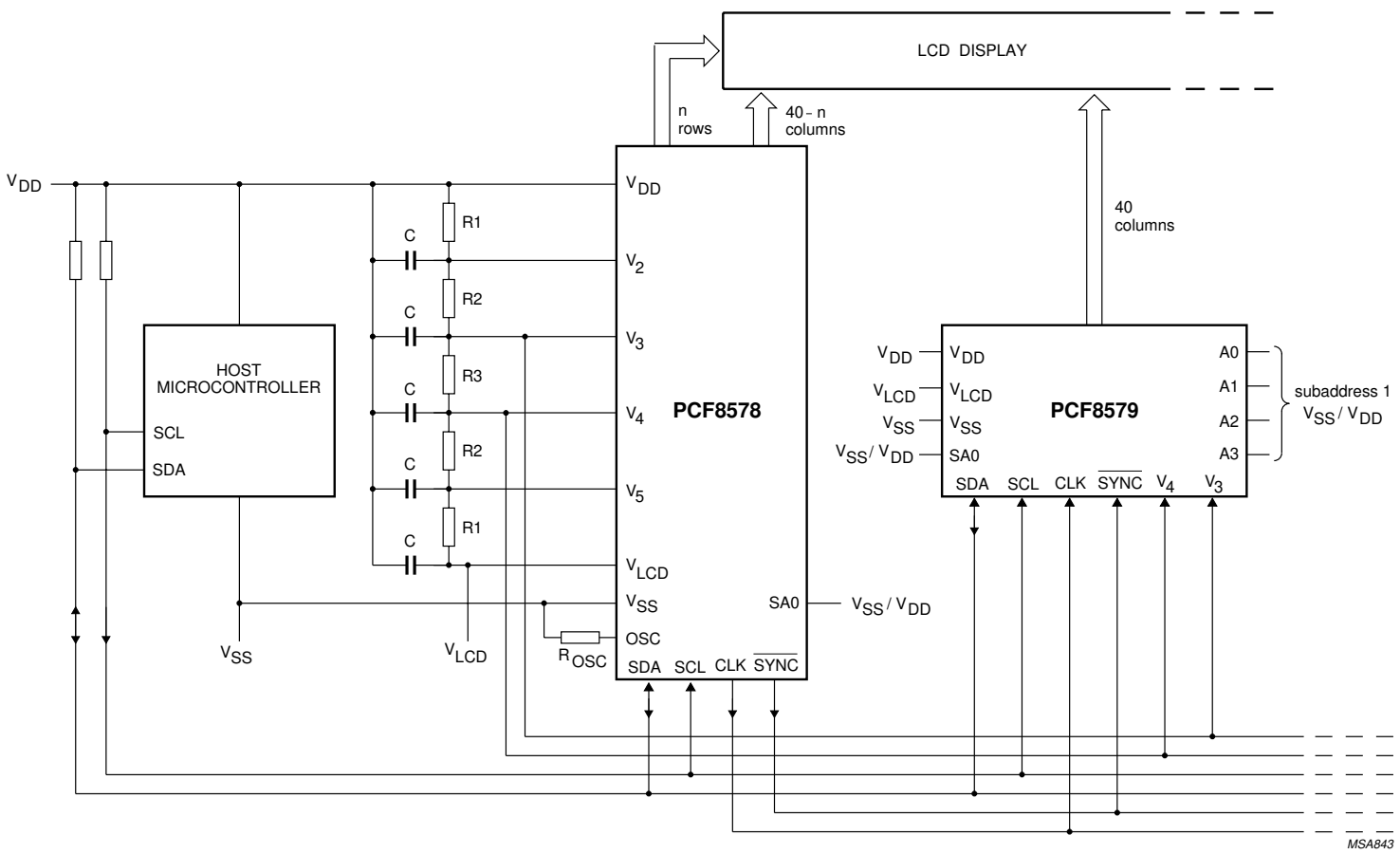
Fig.5 Typical mixed mode configuration.
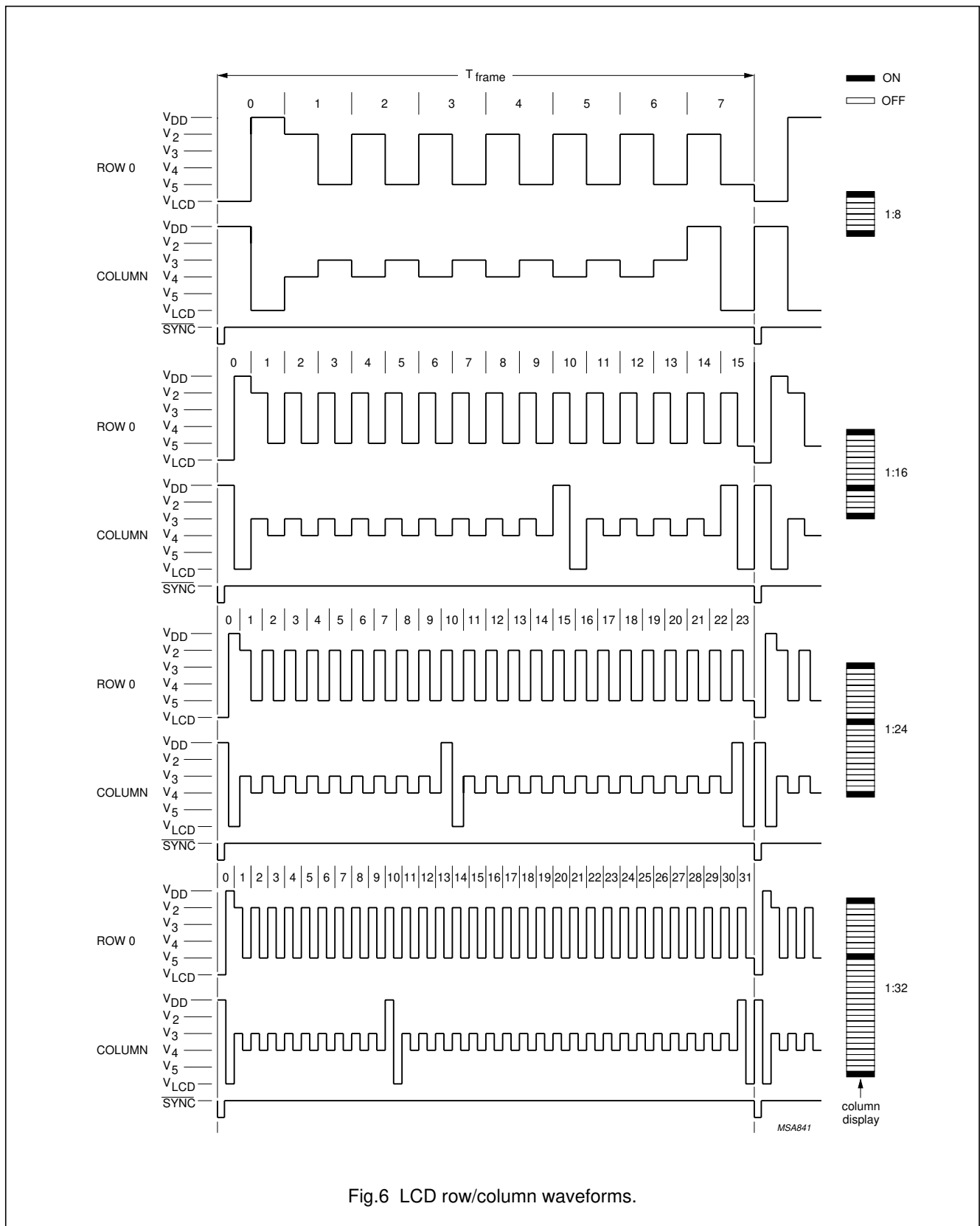
Fig.6 LCD row/column waveforms.
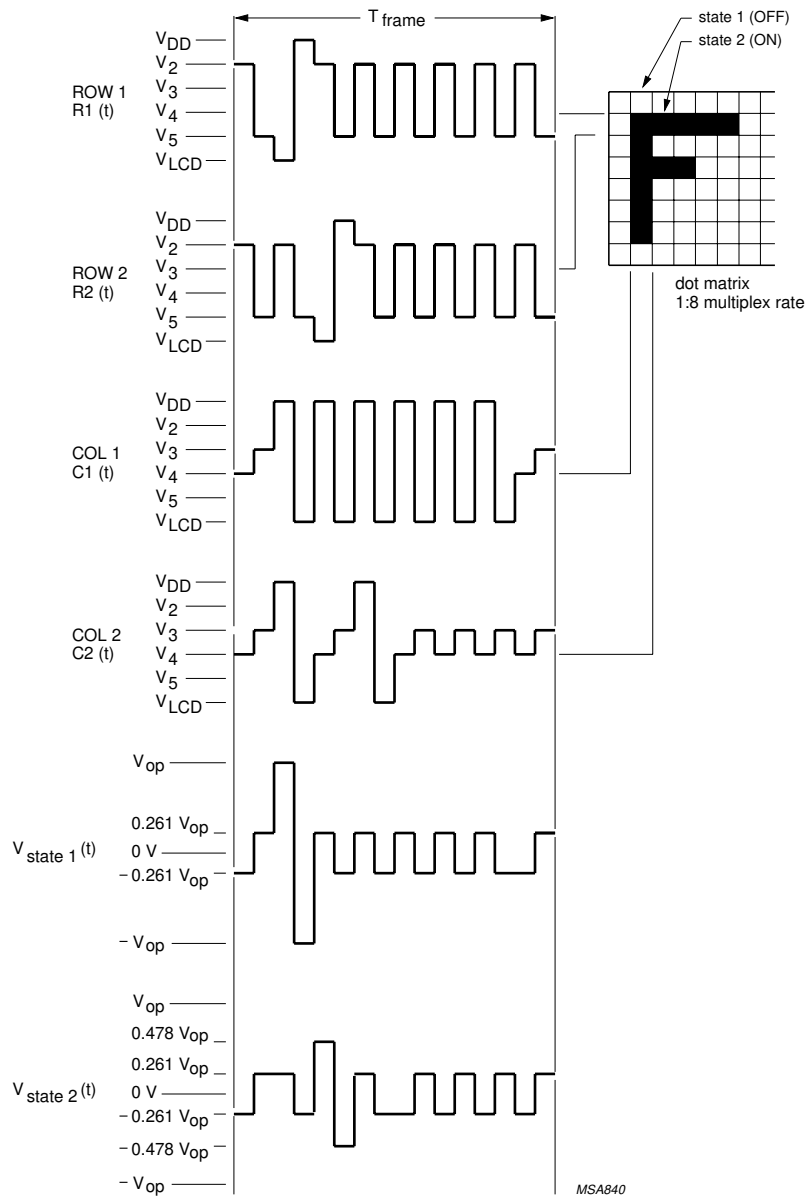
$V_{state\ 1}\ (t) = C1(t) - R1(t):$

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8\ (\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}\ (t) = C2(t) - R2(t):$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\ (\sqrt{8}-1)}{\sqrt{8}\ (\sqrt{8}+1)^2}} = 0.297$$
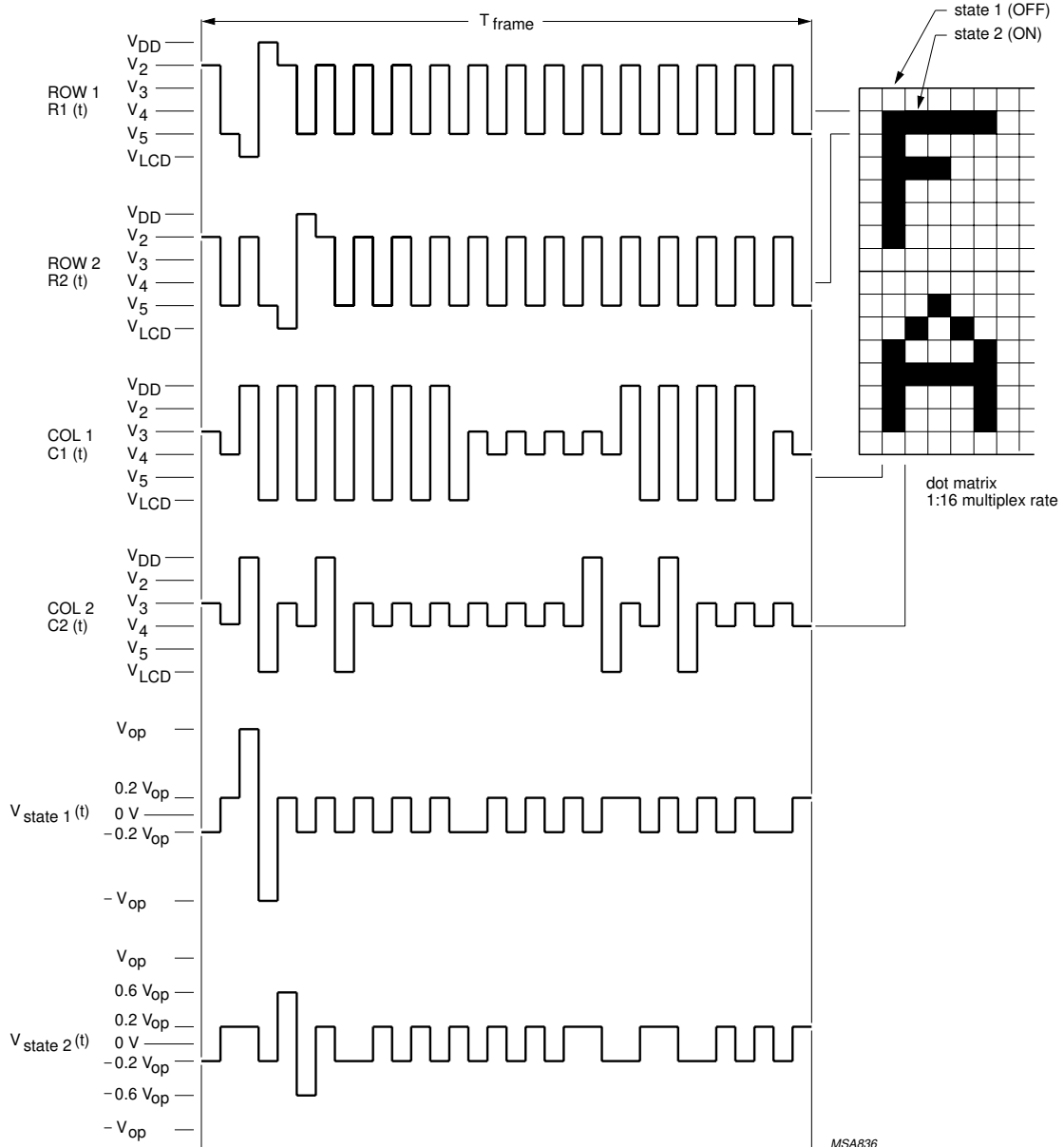
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n\ (\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\ (\sqrt{n}-1)}{\sqrt{n}\ (\sqrt{n}+1)^2}}$$

Fig.7 LCD drive mode waveforms for 1 : 8 multiplex rate.

$V_{state\,1}\,(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16\,(\sqrt{16}+1)}} = 0.316$$

$V_{state\,2}\,(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16}-1)}{\sqrt{16}\,(\sqrt{16}+1)^2}} = 0.254$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n\,(\sqrt{n}+1)}}$$

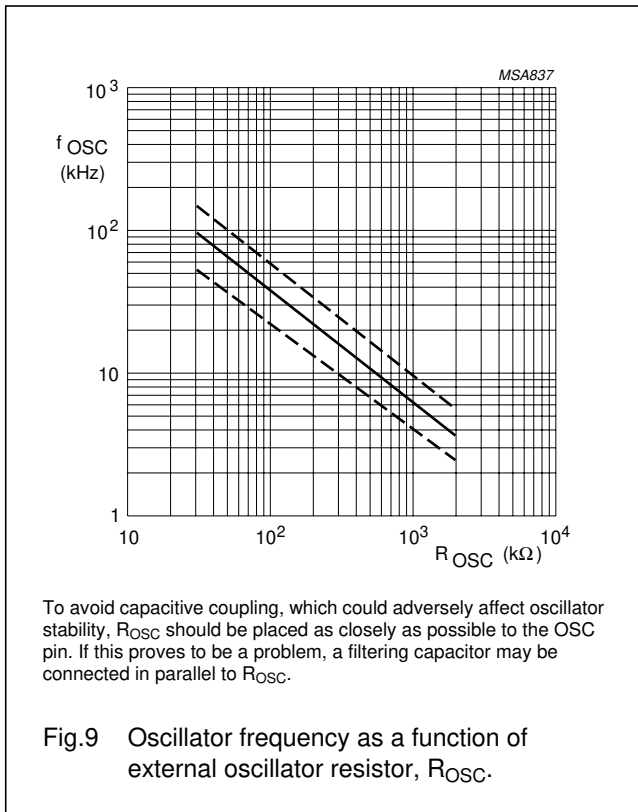$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n}-1)}{\sqrt{n}\,(\sqrt{n}+1)^2}}$$

Fig.8 LCD drive mode waveforms for 1 : 16 multiplex rate.

| LCD row/column driver for dot matrix graphic displays | PCF8578 |

7.5 Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.9. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency $\frac{1}{6}$ (multiplex rate 1 : 8, 1 : 16 and 1 : 32) or $\frac{1}{8}$ (multiplex rate 1 : 24) of the oscillator frequency.

To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

Fig.9 Oscillator frequency as a function of external oscillator resistor, R_{OSC}.

7.6 External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 4 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

7.7 Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

7.8 Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit.

Using a 1 : 16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations, i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1 : 8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit. In 1 : 8 R0 to R7 are rows; in 1 : 16 R0 to R15/C15 are rows; in 1 : 24 R0 to R23/C23 are rows; in 1 : 32 R0 to R31/C31 are rows.

Table 4 Signal frequencies required for nominal 64 Hz frame frequency; note 1.

OSCILLATOR FREQUENCY f_{OSC}[(2)] (Hz)	FRAME FREQUENCY $f_{\overline{SYNC}}$ (Hz)	MULTIPLEX RATE (n)	DIVISION RATIO	CLOCK FREQUENCY f_{CLK} (Hz)
12288	64	1 : 8, 1 : 16, 1 : 32	6	2048
12288	64	1 : 24	8	1536

Notes

1. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

2. R_{OSC} = 330 kΩ.

7.9 Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

7.10 Display RAM

The PCF8578 contains a 32×40-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes ($4 \times 8 \times 40$ bits). During RAM access, data is transferred to/from the RAM via the I^{2}C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579. There is a direct correspondence between X-address and column output number.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^{2}C-bus.

7.12 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

7.13 I^{2}C-bus controller

The I^{2}C-bus controller detects the I^{2}C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I^{2}C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

7.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.15 RAM access

RAM operations are only possible when the PCF8578 is in mixed mode.

In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 to G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.10).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.11):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM ACCESS mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

7.16 Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.12. This feature is useful when scrolling in alphanumeric applications.

7.17 TEST pin

The TEST pin must be connected to V$_{SS}$.
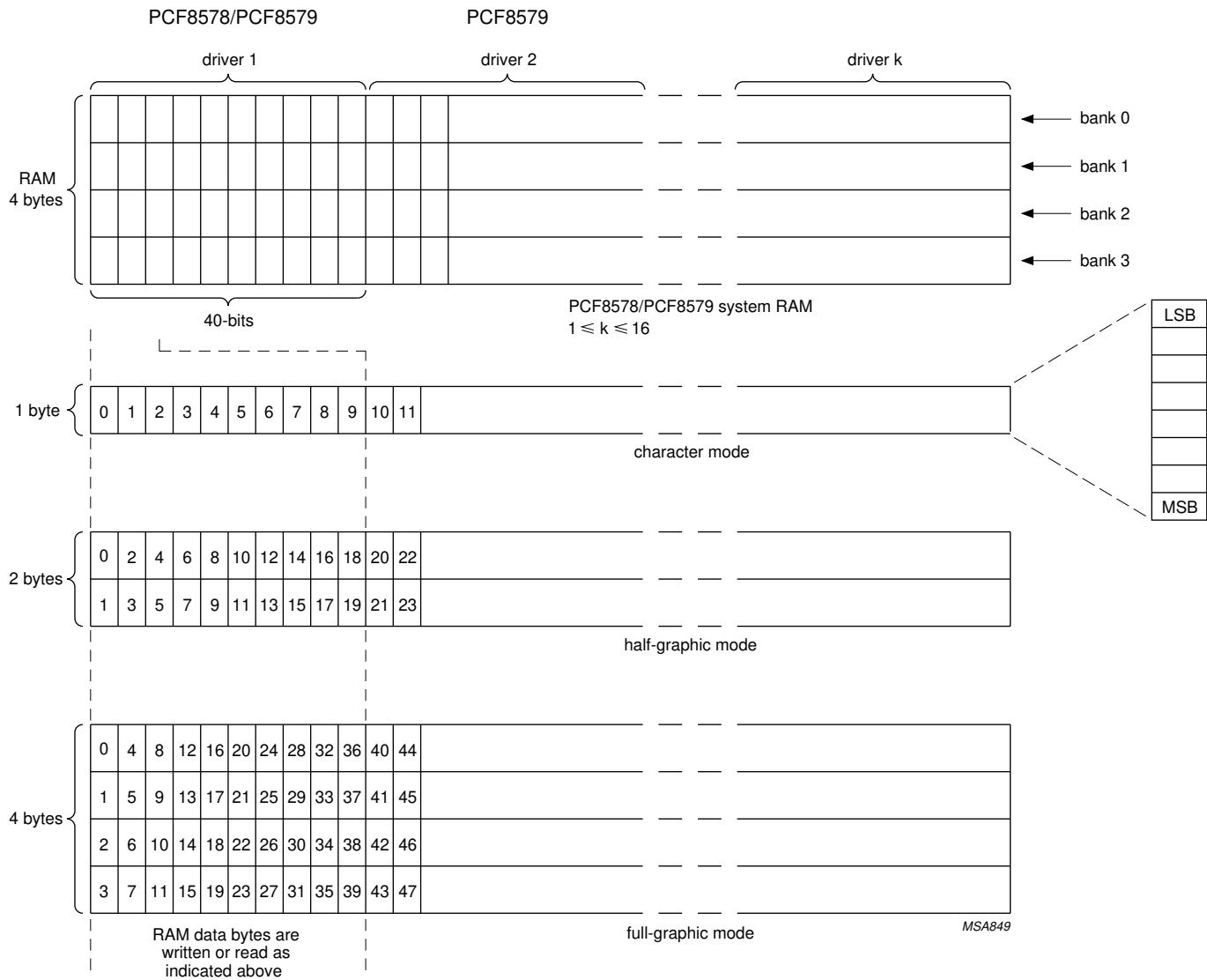
Fig.10 RAM ACCESS mode.
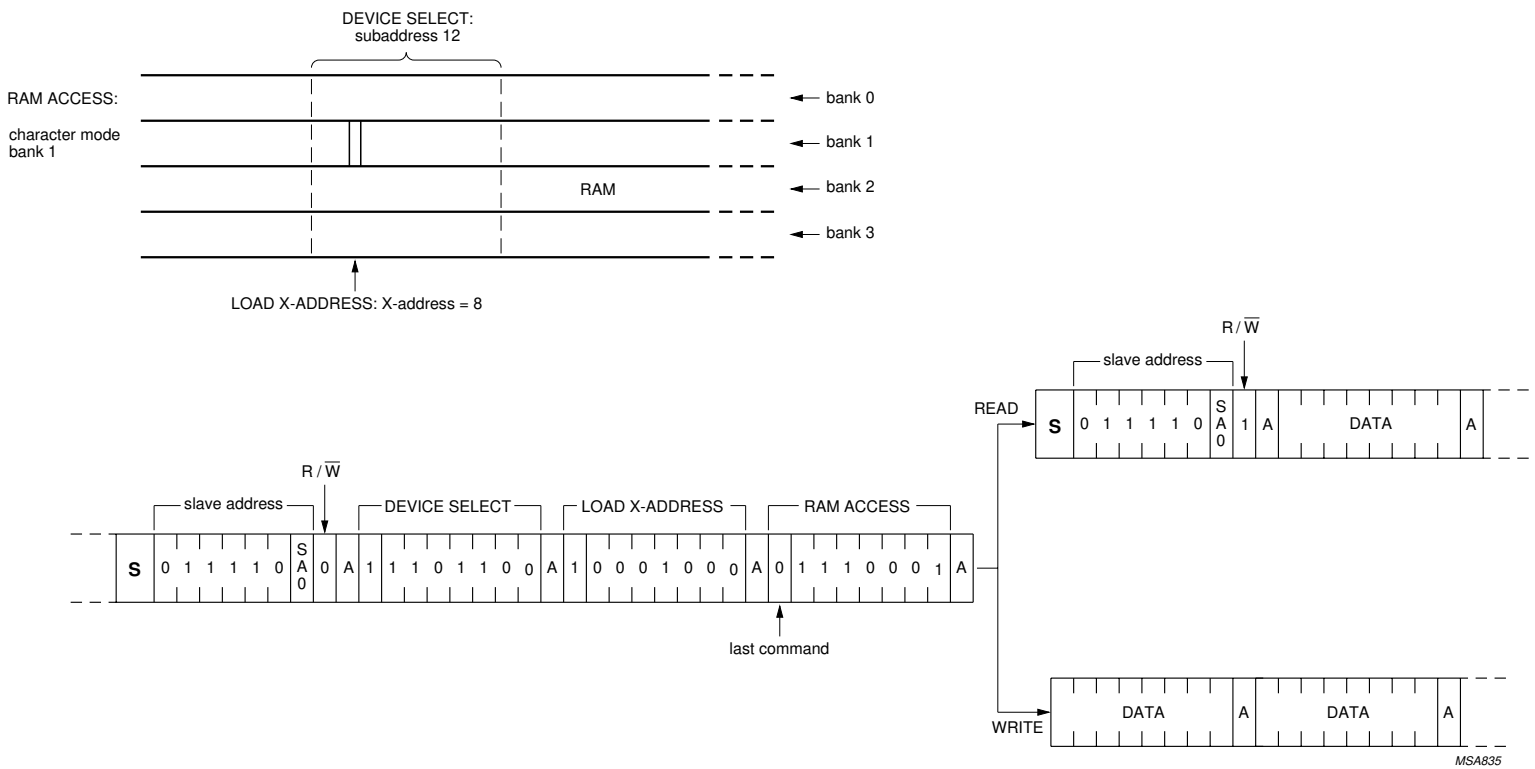
Fig.11 Example of commands specifying initial data byte RAM locations.
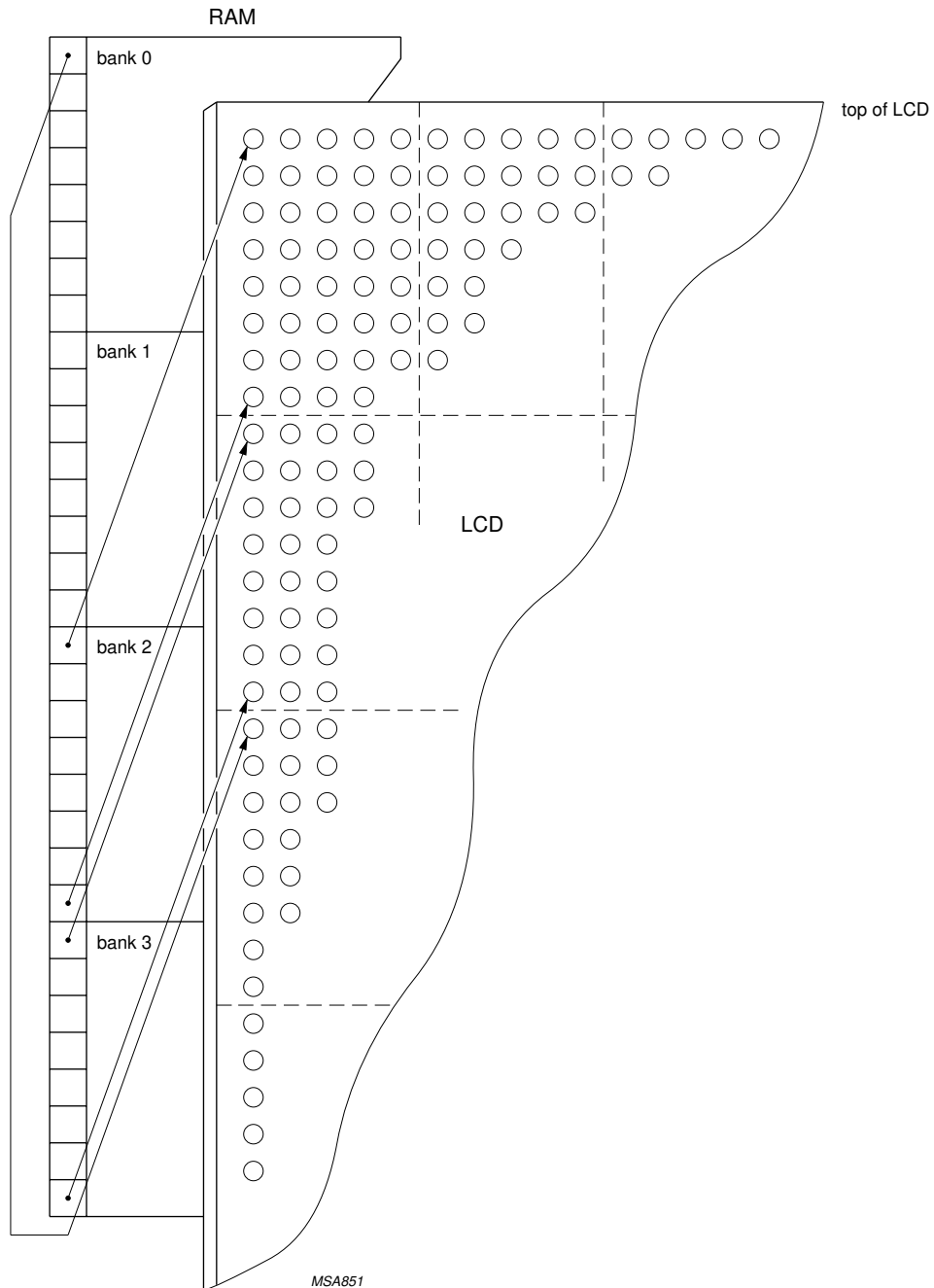
Fig.12 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

8   I2C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I2C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I2C-bus for very large applications

2. The use of two types of LCD multiplex schemes on the same I2C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I2C-bus protocol is shown in Fig.13.
All communications are initiated with a start condition (S) from the I2C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I2C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by not generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.
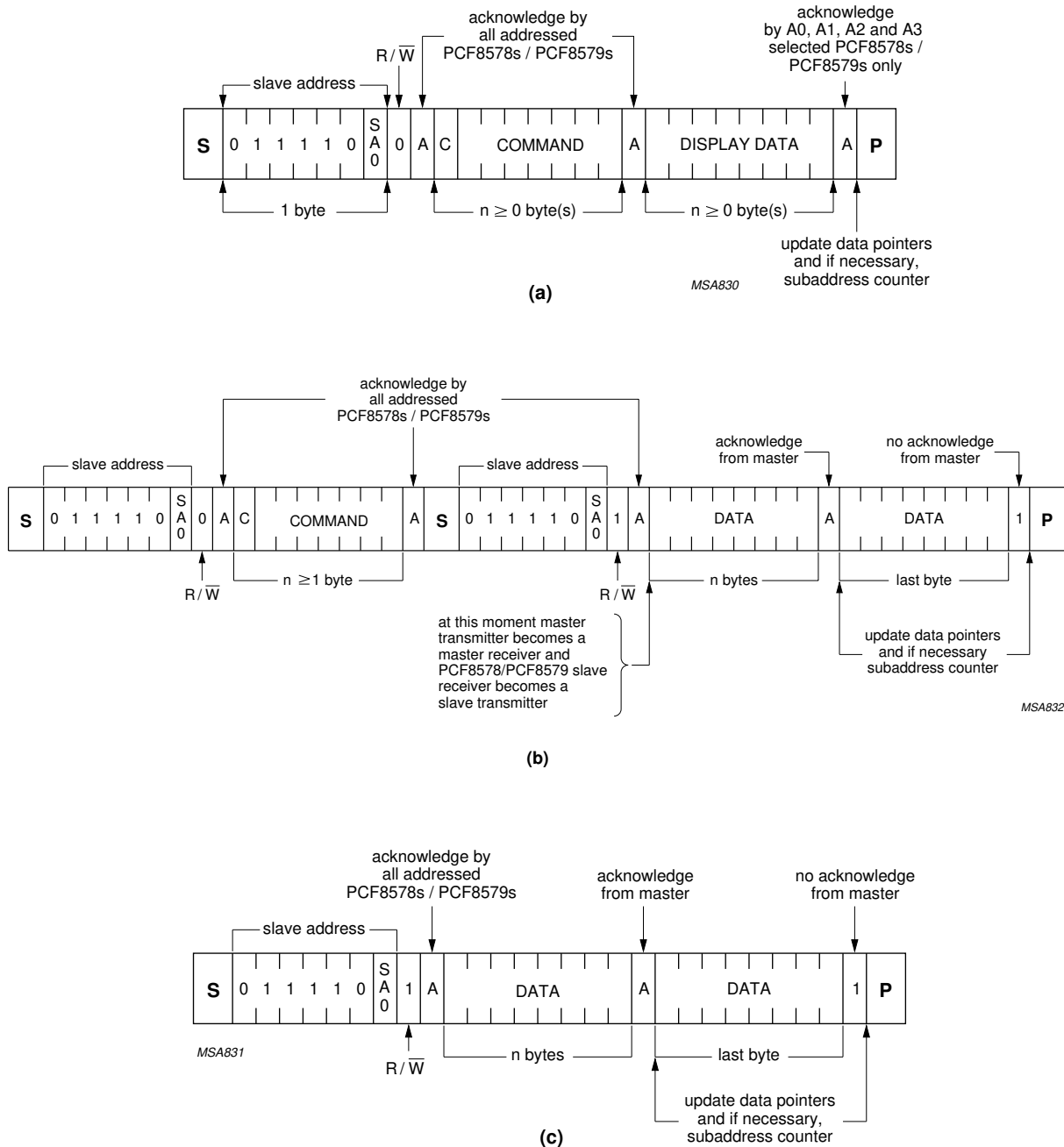
Fig.13 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string
(WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ
mode).

LCD row/column driver for
dot matrix graphic displays

PCF8578

8.1 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.14). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

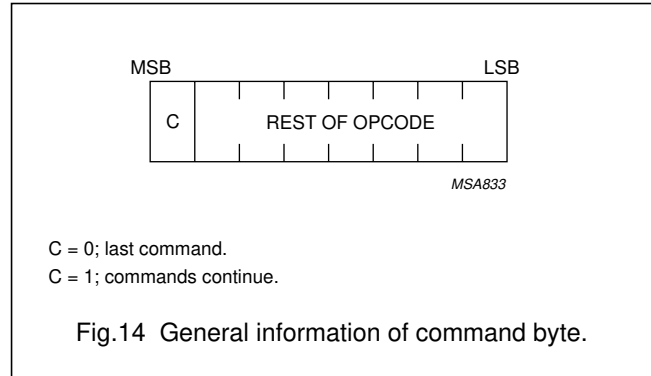The five commands available to the PCF8578 are defined in Tables 5 and 6.

C = 0; last command.
C = 1; commands continue.

Fig.14 General information of command byte.

Table 5 Summary of commands

COMMAND	OPCODE[1]							DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit. D = may be a logic 1 or 0.

LCD row/column driver for
dot matrix graphic displays

PCF8578

Table 6   Definition of PCF8578/PCF8579 commands

COMMAND			OPCODE						OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 7	defines LCD drive mode
									see Table 8	defines display status
									see Table 9	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 10	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 11	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 12	defines the auto-increment behaviour of the address for RAM access
									see Table 13	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 14	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 7 Set mode option 1

LCD DRIVE MODE		BITS	
		M1	**M0**
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 8 Set mode option 2

DISPLAY STATUS	BITS	
	E1	**E0**
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 9 Set mode option 3

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 10 Set start bank option 1

START BANK POINTER	BITS	
	B1	**B0**
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 11 Device select option 1

DESCRIPTION	BITS			
Decimal value 0 to 15	A3	A2	A1	A0

Table 12 RAM access option 1

RAM ACCESS MODE	BITS	
	G1	**G0**
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 6.

Table 13 Device select option 1

DESCRIPTION	BITS	
Decimal value 0 to 3	Y1	Y0

Table 14 Device select option 1

DESCRIPTION	BITS					
Decimal value 0 to 39	X5	X4	X3	X2	X1	X0

9 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

9.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition (P).

9.3 System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

9.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.
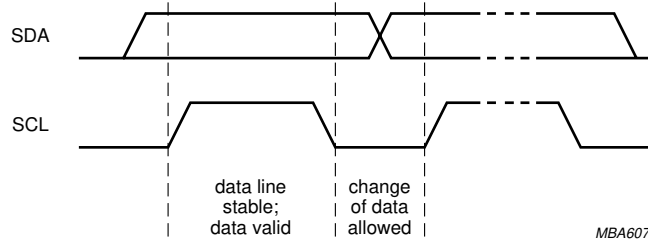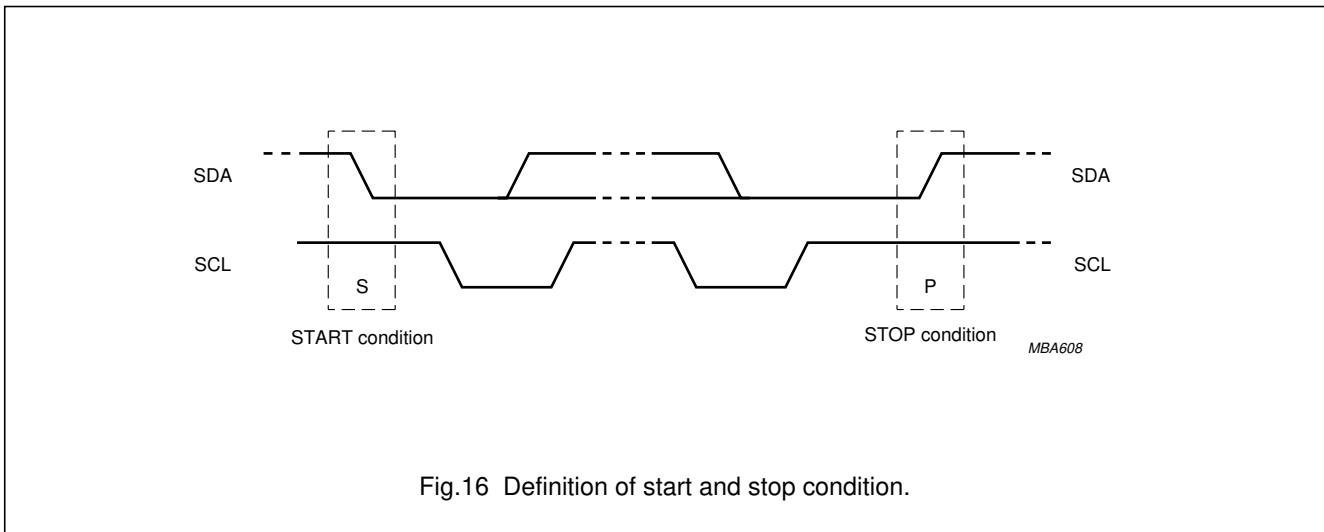

Fig.15 Bit transfer.

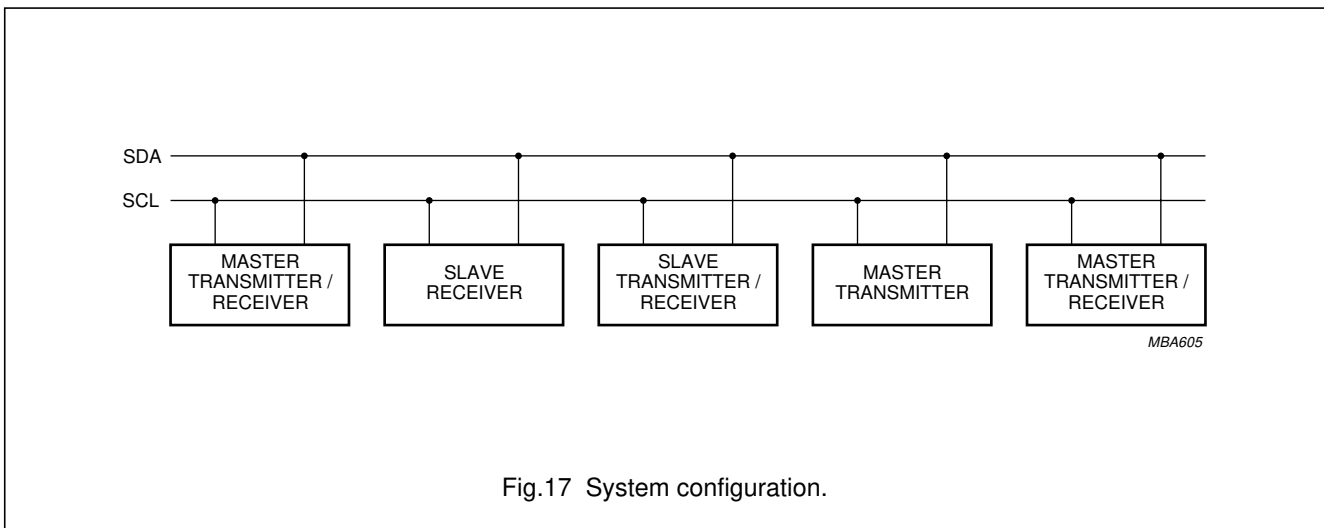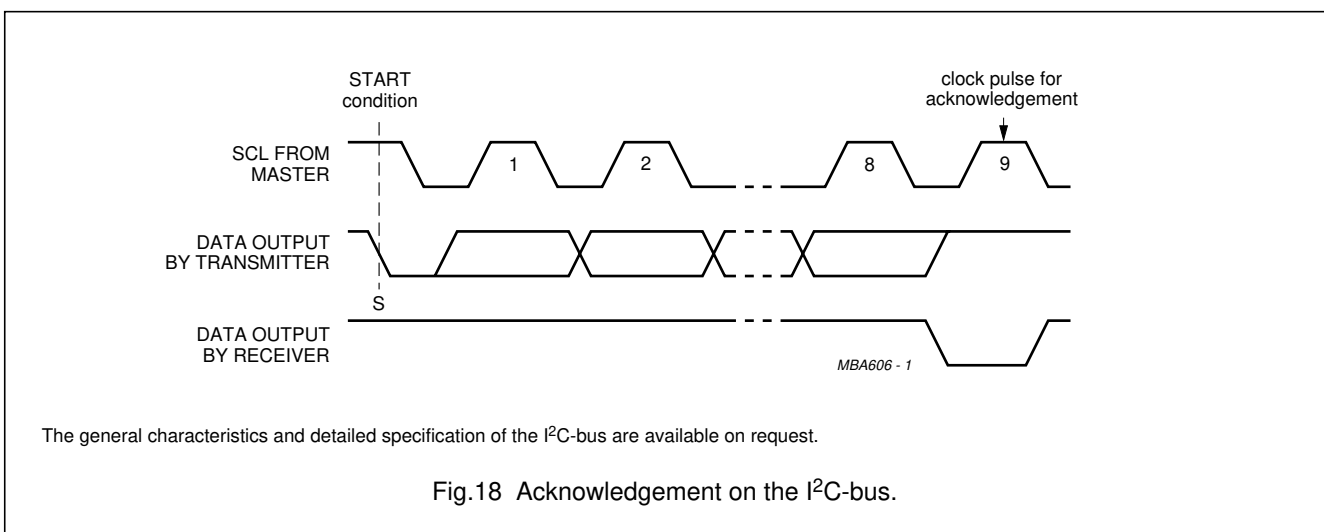Fig.16 Definition of start and stop condition.

Fig.17 System configuration.

The general characteristics and detailed specification of the I^{2}C-bus are available on request.

Fig.18 Acknowledgement on the I^{2}C-bus.