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**PCF8578**
LCD row/column driver for dot matrix graphic displays
Rev. 06 — 5 May 2009                                     Product data sheet

# 1. General description

The PCF8578 is a low power CMOS[1] LCD row and column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable and configurable for the following ratios of rows/columns: $\frac{32}{8}$, $\frac{24}{16}$, $\frac{16}{24}$ or $\frac{8}{32}$. The PCF8578 can function as a stand-alone LCD controller and driver for use in small systems. For larger systems it can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overhead is minimized by a display RAM with auto-incremented addressing and display bank switching.

# 2. Features

- Single chip LCD controller and driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable for several ratios of rows/columns: $\frac{32}{8}$, $\frac{24}{16}$, $\frac{16}{24}$ or $\frac{8}{32}$
- Selectable multiplex rates: 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-On Reset (POR) blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead small outline package and 64 pin quad flat pack

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 15.

## 3. Applications

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Industrial computer terminals
- Instrumentation

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | Version |
|---|---|---|---|---|
| | **Name** | **Description** | | |
| PCF8578T/1 | VSO56 | plastic very small outline package; 56 leads | | SOT190-1 |
| PCF8578H/1 | LQFP64 | plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm[1] | | SOT314-2 |
| PCF8578HT/1 | TQFP64 | plastic thin quad flat package; 64 leads; body $10 \times 10 \times 1.0$ mm | | SOT357-1 |

[1] Should not be used for new designs.

## 5. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| PCF8578T/1 | PCF8578T |
| PCF8578H/1 | PCF8578H |
| PCF8578HT/1 | PCF8578HT |

# 6. Block diagram



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.

**Fig 1.    Block diagram**
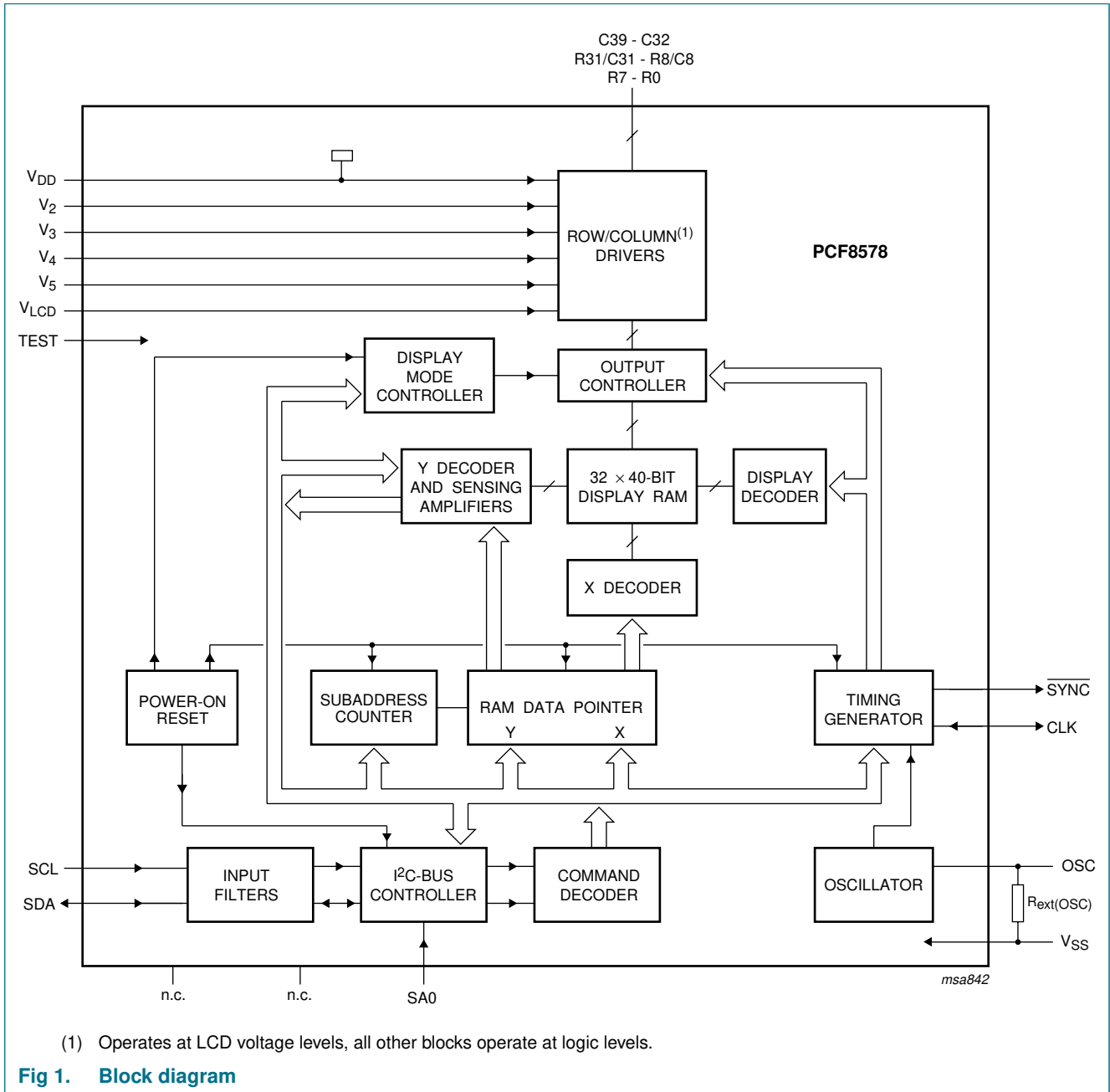
# 7. Pinning information

## 7.1 Pinning



Top view. For mechanical details, see Figure 29.

**Fig 2.** **Pinning diagram of PCF8578T/1 (VSO56)**

Top view. For mechanical details, see Figure 30.

**Fig 3.    Pinning diagram of PCF8578H/1 (LQFP64)**

Top view. For mechanical details, see Figure 31.

**Fig 4.    Pinning diagram of PCF8578HT/1 (TQFP64)**
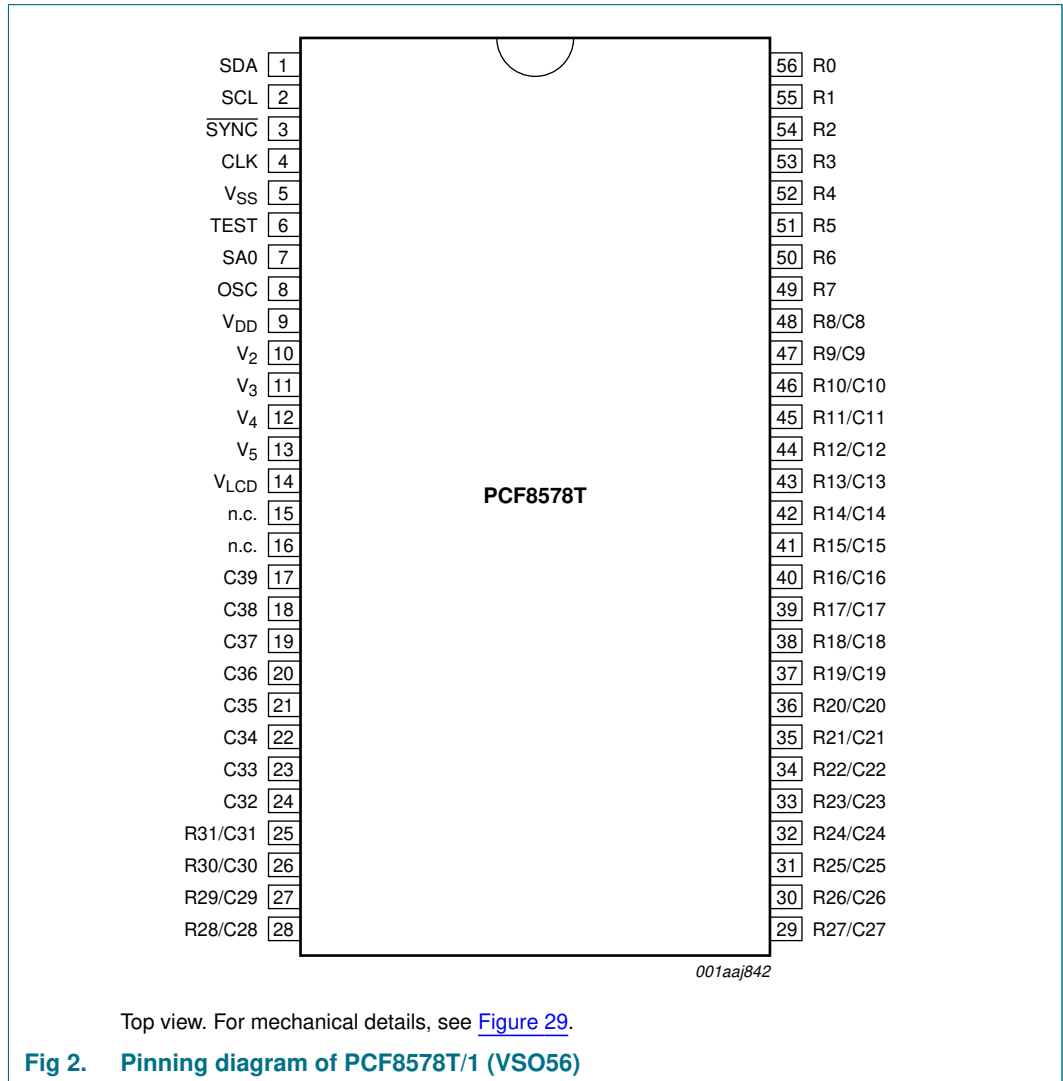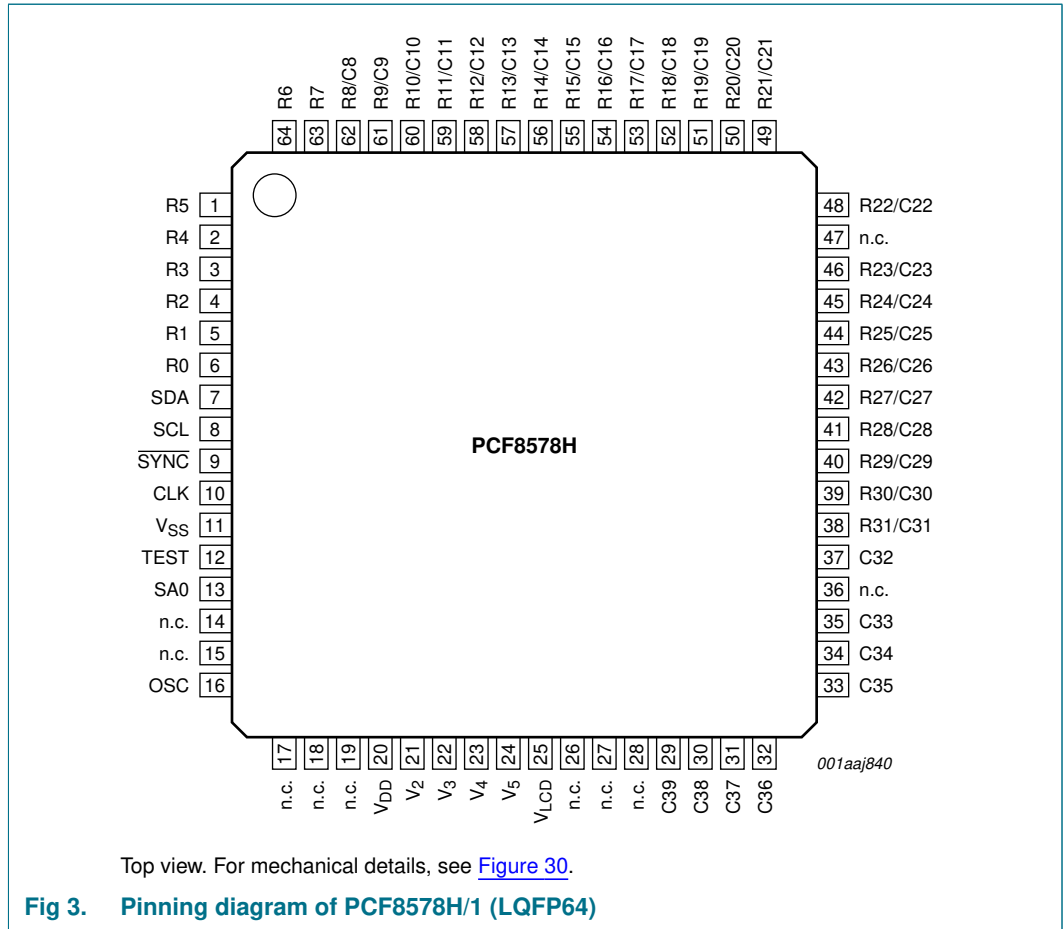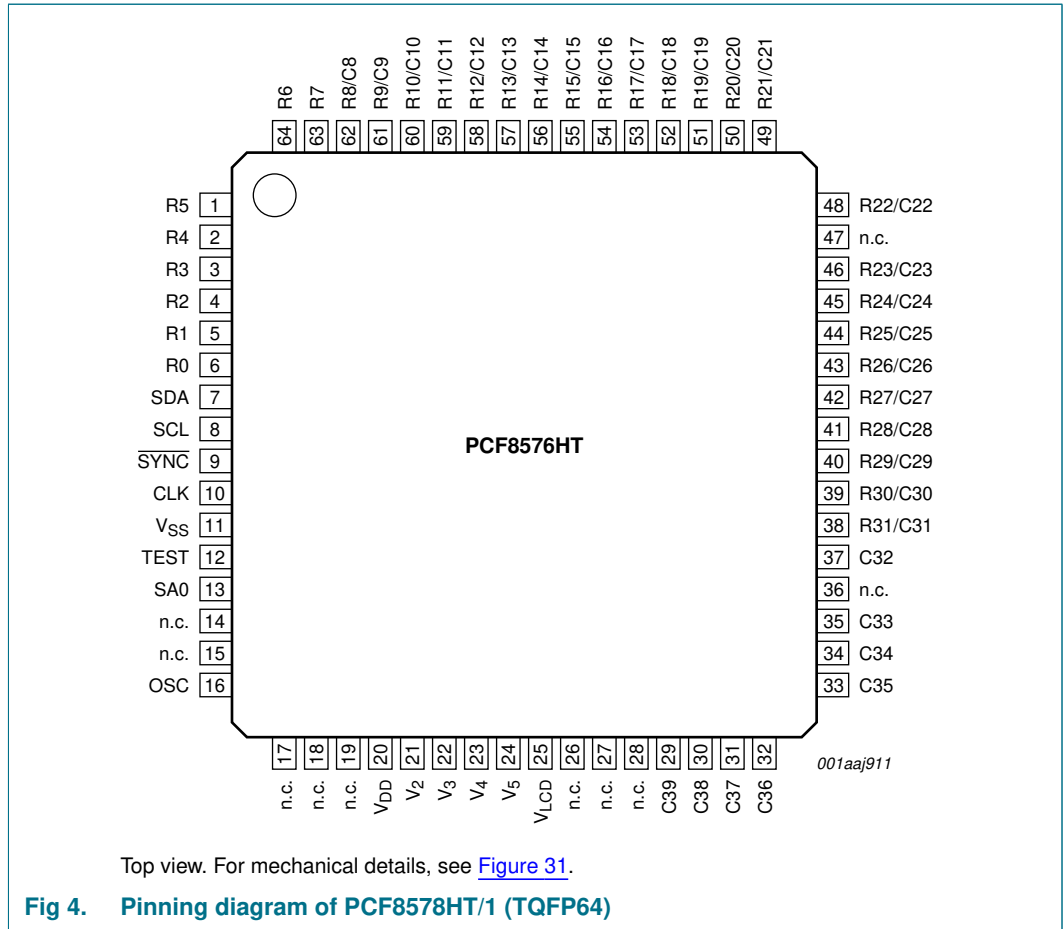
### 7.2 Pin description

**Table 3.     Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | **VSO56** | **LQFP64, TQFP64** | |
| SDA | 1 | 7 | $I^2C$-bus serial data input/output |
| SCL | 2 | 8 | $I^2C$-bus serial clock input |
| SYNC | 3 | 9 | cascade synchronization output |
| CLK | 4 | 10 | external clock input/output |
| $V_{SS}$ | 5 | 11 | ground |
| TEST[1] | 6 | 12 | test pin |
| SA0 | 7 | 13 | $I^2C$-bus slave address input (bit 0) |
| OSC | 8 | 16 | oscillator input |
| $V_{DD}$ | 9 | 20 | supply voltage |
| $V_2$ to $V_5$ | 10 to 13 | 21 to 24 | LCD bias voltage inputs |
| $V_{LCD}$ | 14 | 25 | LCD supply voltage |
| n.c. | 15, 16 | 14, 15, 17 to 19, 26 to 28, 36, 47 | not connected |
| C39 to C32 | 17 to 24 | 29 to 35, 37 | LCD column driver outputs |
| R31/C31 to R8/C8 | 25 to 48 | 38 to 46, 48 to 62 | LCD row and column driver outputs |
| R7 to R0 | 49 to 56 | 63, 64, 1 to 6 | LCD row driver outputs |

[1]     The TEST pin must be connected to $V_{SS}$.

# 8. Functional description

## 8.1 Display configurations

The PCF8578 row and column driver is designed for use in one of three ways:

- Stand-alone row and column driver for small displays (mixed mode)
- Row and column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (mixed mode and row mode)

**Table 4.    Possible display configurations**

| Application | Multiplex rate | Mixed mode | | Row mode | | Typical applications |
|---|---|---|---|---|---|---|
| | | Rows | Columns | Rows | Columns | |
| stand alone | 1:8 | 8 | 32 | - | - | small digital or alphanumeric displays |
| | 1:16 | 16 | 24 | - | - | |
| | 1:24 | 24 | 16 | - | - | |
| | 1:32 | 32 | 8 | - | - | |
| with PCF8579 | 1:8 | 8[1] | 632[1] | $8 \times 4$[2] | 640[2] | alphanumeric displays and dot matrix graphic displays |
| | 1:16 | 16[1] | 624[1] | $16 \times 2$[2] | 640[2] | |
| | 1:24 | 24[1] | 616[1] | 24[2] | 640[2] | |
| | 1:32 | 32[1] | 608[1] | 32[2] | 640[2] | |

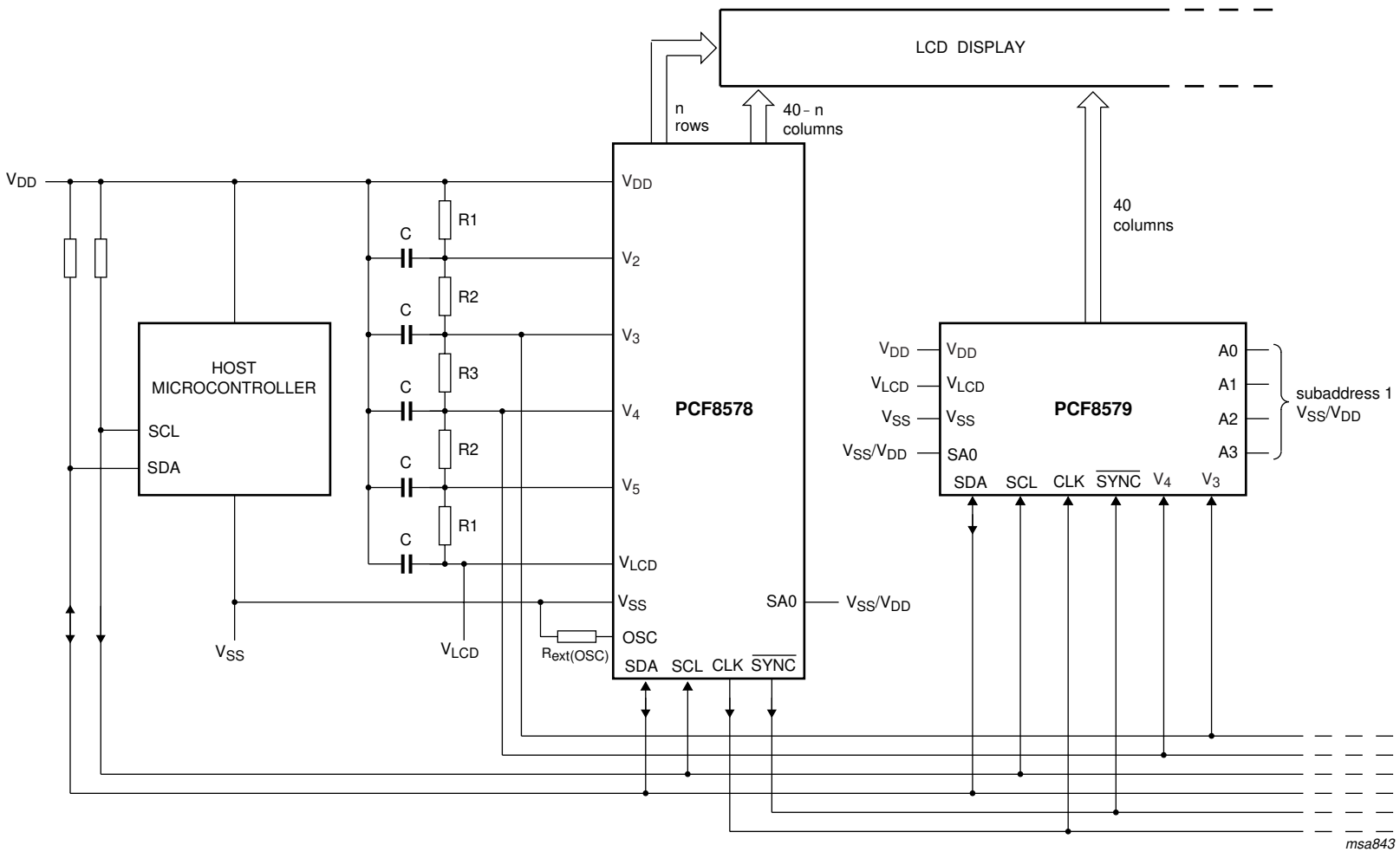[1]    Using 15 PCF8579s.

[2]    Using 16 PCF8579s.

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See Table 4 for common display configurations.

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between pin OSC and pin $V_{SS}$.

Five commands are available to configure and control the operation of the device. Communication is made via a two-line bidirectional I²C-bus. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 have different subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0111 100 (see Section 8.8.7 on page 19). The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Figure 5 (a stand-alone system would be identical but without the PCF8579).

LCD  DISPLAY

n rows

40 – n columns

40 columns

V_DD

R1

C

V_2

R2

C

V_3

R3

C

HOST MICROCONTROLLER

SCL

SDA

C

R2

V_4

C

R1

V_5

V_LCD

V_SS

OSC

R_ext(OSC)

SDA  SCL  CLK  SYNC

V_DD

V_2

V_3

V_4

V_5

V_LCD

V_SS

SA0

PCF8578

SA0 — V_SS/V_DD

V_LCD

V_SS

V_DD

V_LCD

V_SS

V_SS/V_DD

SDA  SCL  CLK  SYNC  V_4  V_3

A0

A1

A2

A3

PCF8579

subaddress 1 V_SS/V_DD

msa843

**Fig 5.    Typical mixed mode configuration**

Table 5 shows the relative values of the resistors required in the configuration of Figure 5 to produce the standard multiplex rates.

**Table 5.** **Multiplex rates and resistor values for Figure 5**

| Resistors | Multiplex rate (1:n) | |
| --- | --- | --- |
| | n = 8 | n = 16, 24, 32 |
| R1 | R | R |
| R2 | $(\sqrt{n} - 2)R$ | R |
| R3 | $(3 - \sqrt{n})R$ | $(\sqrt{n} - 3)R$ |

## 8.2 Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1:32 multiplex rate, row mode
3. Start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I2C-bus interface is initialized

**Remark:** Do not transfer data on the I2C-bus for at least 1 ms after power-on to allow the reset action to complete.

## 8.3 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage ($V_{th}$). $V_{th}$ is typically defined as the RMS voltage at which the LCD exhibits 10 % contrast. Table 6 shows the optimum voltage bias levels and Table 7 the discrimination ratios (D) for the different multiplex rates as functions of $V_{oper}$.

$$V_{oper} = V_{DD} - V_{LCD} \tag{1}$$

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with the equation

$$V_{on(RMS)} = V_{oper} \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n(\sqrt{n} + 1)}} \tag{2}$$

and the RMS off-state voltage ($V_{off(RMS)}$) with the equation

$$V_{off(RMS)} = V_{oper} \sqrt{\frac{2(\sqrt{n} - 1)}{\sqrt{n}(\sqrt{n} + 1)^2}} \tag{3}$$

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where the values for n are determined by the multiplex rate (1:n). Valid values for n are:

n = 8 for 1:8 multiplex

n = 16 for 1:16 multiplex

n = 24 for 1:24 multiplex

n = 32 for 1:32 multiplex

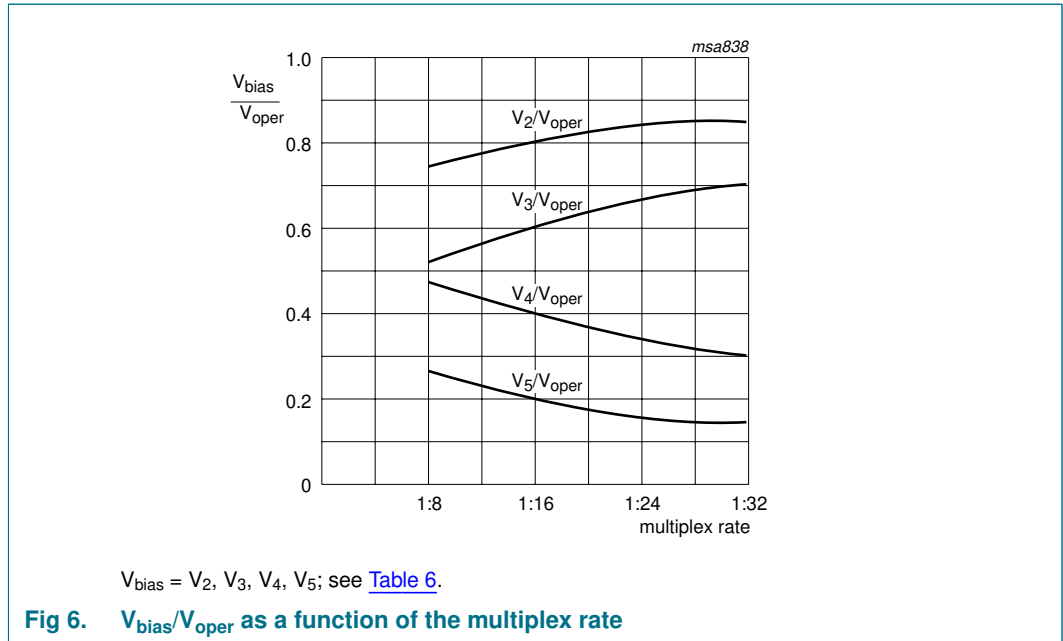**Table 6.    Optimum LCD voltages**

| Bias ratios | Multiplex rate | | | |
|---|---|---|---|---|
| | 1:8 | 1:16 | 1:24 | 1:32 |
| $\dfrac{V_2}{V_{oper}}$ | 0.739 | 0.800 | 0.830 | 0.850 |
| $\dfrac{V_3}{V_{oper}}$ | 0.522 | 0.600 | 0.661 | 0.700 |
| $\dfrac{V_4}{V_{oper}}$ | 0.478 | 0.400 | 0.339 | 0.300 |
| $\dfrac{V_5}{V_{oper}}$ | 0.261 | 0.200 | 0.170 | 0.150 |

**Table 7.    Discrimination ratios**

| Discrimination ratios | Multiplex rate | | | |
|---|---|---|---|---|
| | 1:8 | 1:16 | 1:24 | 1:32 |
| $\dfrac{V_{off(RMS)}}{V_{oper}}$ | 0.297 | 0.245 | 0.214 | 0.193 |
| $\dfrac{V_{on(RMS)}}{V_{oper}}$ | 0.430 | 0.316 | 0.263 | 0.230 |
| $D = \dfrac{V_{on(RMS)}}{V_{off(RMS)}}$ | 1.447 | 1.291 | 1.230 | 1.196 |
| $\dfrac{V_{oper}}{V_{th}}$ | 3.370 | 4.080 | 4.680 | 5.190 |

Figure 6 shows the values of Table 6 as graphs.

$V_{bias} = V_2, V_3, V_4, V_5$; see Table 6.

**Fig 6.** $V_{bias}/V_{oper}$ **as a function of the multiplex rate**

## 8.4 LCD drive mode waveforms
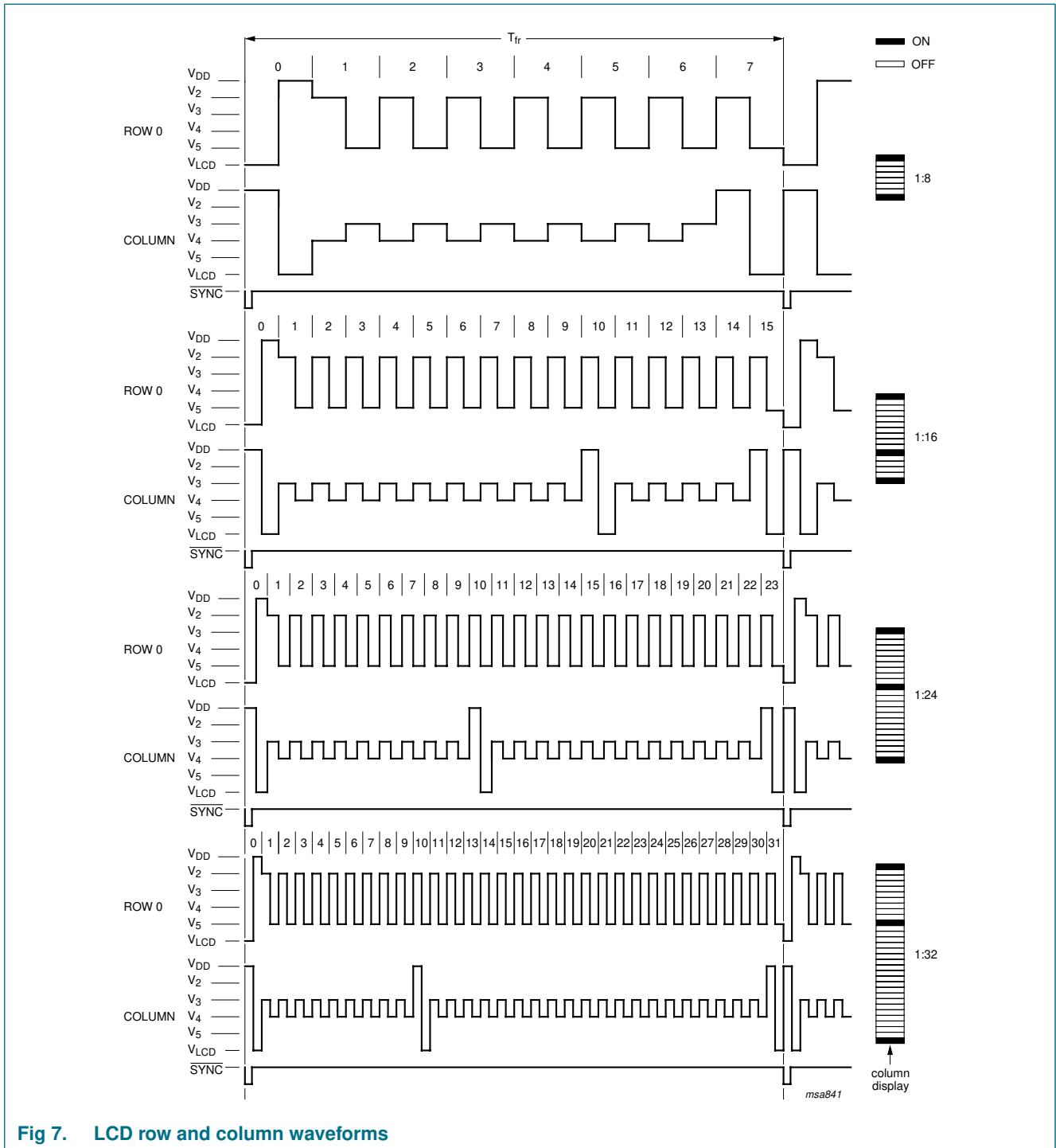


**Fig 7.** **LCD row and column waveforms**

$V_{state1}(t) = C1(t) - R1(t).$

$$\frac{V_{on(RMS)}}{V_{oper}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state2}(t) = C2(t) - R2(t).$

$$\frac{V_{off(RMS)}}{V_{oper}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

**Fig 8.    LCD drive mode waveforms for 1:8 multiplex rate**

state 1 (OFF)
state 2 (ON)

$V_{state1}(t) = C1(t) - R1(t).$

$$\frac{V_{on(RMS)}}{V_{oper}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state2}(t) = C2(t) - R2(t).$

$$\frac{V_{off(RMS)}}{V_{oper}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

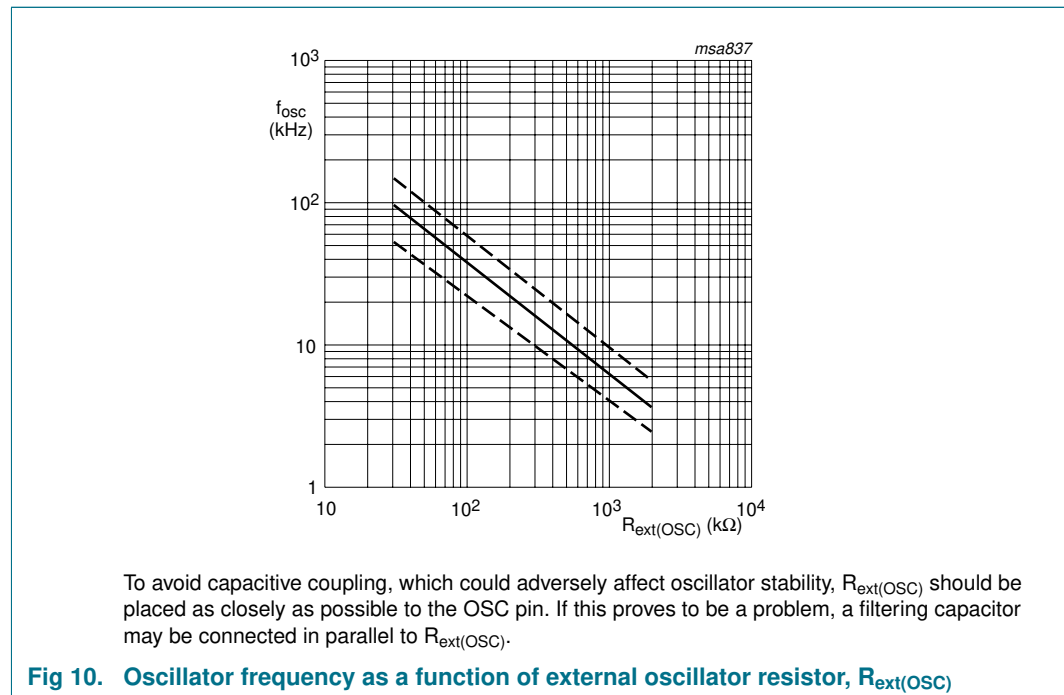**Fig 9.   LCD drive mode waveform for 1:16 multiplex rate**
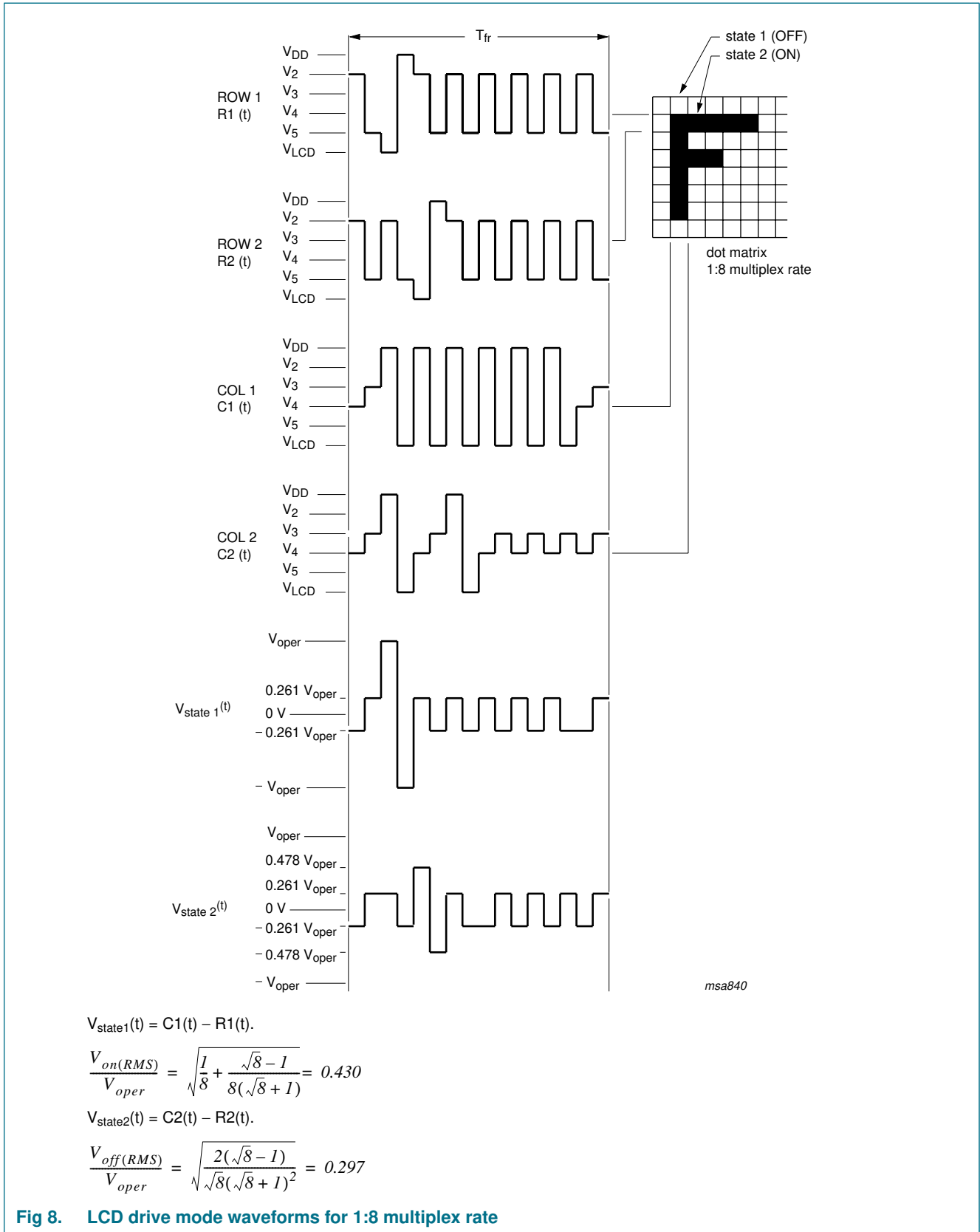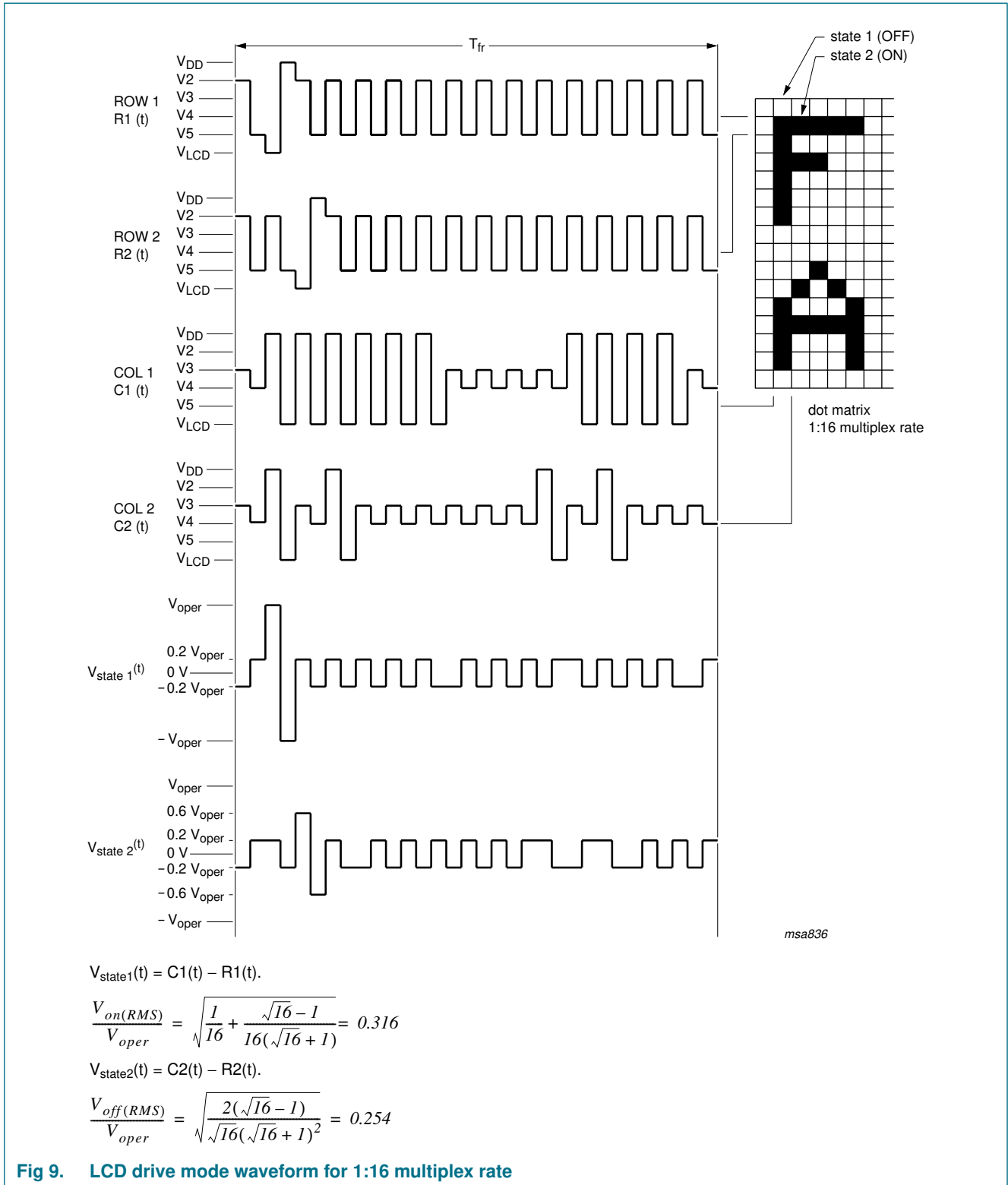
## 8.5 Oscillator

### 8.5.1 Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor $R_{ext(OSC)}$, see Figure 10. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency of $\frac{1}{6}$ (multiplex rate 1:8, 1:16 and 1:32) or $\frac{1}{8}$ (multiplex rate 1:24) of the oscillator frequency.



To avoid capacitive coupling, which could adversely affect oscillator stability, $R_{ext(OSC)}$ should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to $R_{ext(OSC)}$.

**Fig 10. Oscillator frequency as a function of external oscillator resistor, $R_{ext(OSC)}$**

### 8.5.2 External clock

If an external clock is used, OSC must be connected to $V_{DD}$ and the external clock signal to CLK. Table 8 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

**Table 8. Signal frequencies required for nominal 64 Hz frame frequency[1]**

| Oscillator frequency, $f_{osc}$ (Hz)[2] | Frame frequency, $f_{fr}$ (Hz) | Multiplex rate, (1:n) | Division ratio | Clock frequency, $f_{clk}$ (Hz) |
|---|---|---|---|---|
| 12288 | 64 | 1:8, 1:16, 1:32 | 6 | 2048 |
| 12288 | 64 | 1:24 | 8 | 1536 |

[1] A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

[2] $R_{ext(OSC)}$ = 330 kΩ.

## 8.6 Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

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### 8.7 Row and column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 4). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit.

Using a 1:16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations, i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1:8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open circuit.

Depending on the multiplex rate the following outputs are rows:

- In MUX 1:8 R0 to R7
- In MUX 1:16 R0 to R15/C15
- In MUX 1:24 R0 to R23/C23
- In MUX 1:32 R0 to R31/C31

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

### 8.8 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

#### 8.8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

#### 8.8.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition (P).

#### 8.8.3 System configuration

A device transmitting a message is a transmitter, a device receiving a message is the receiver. The device that controls the message flow is the master and the devices which are controlled by the master are the slaves.

### 8.8.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.
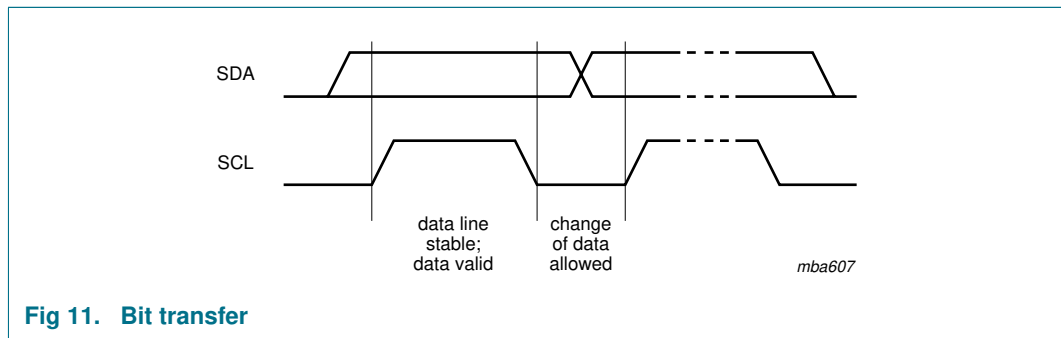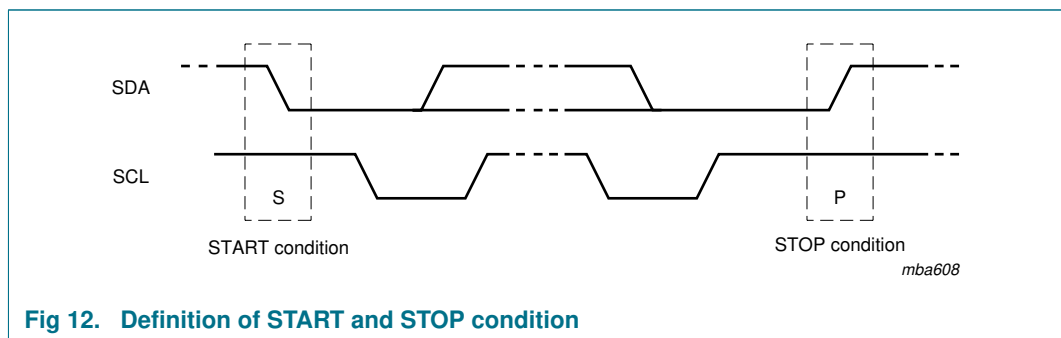


**Fig 11. Bit transfer**
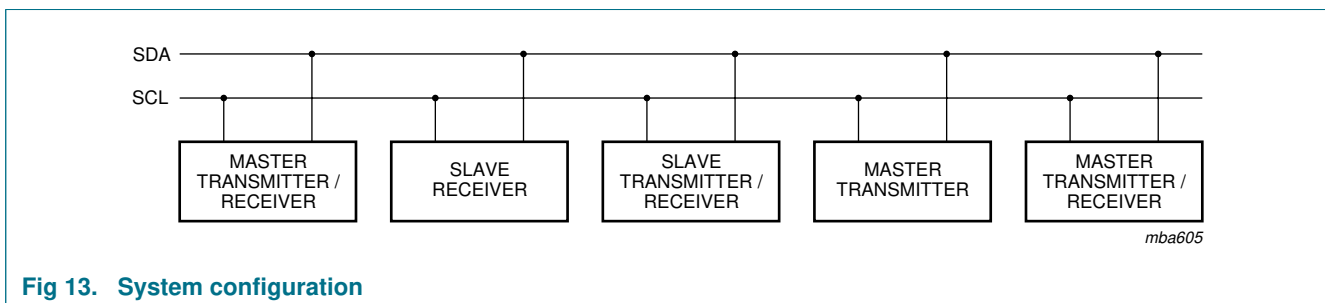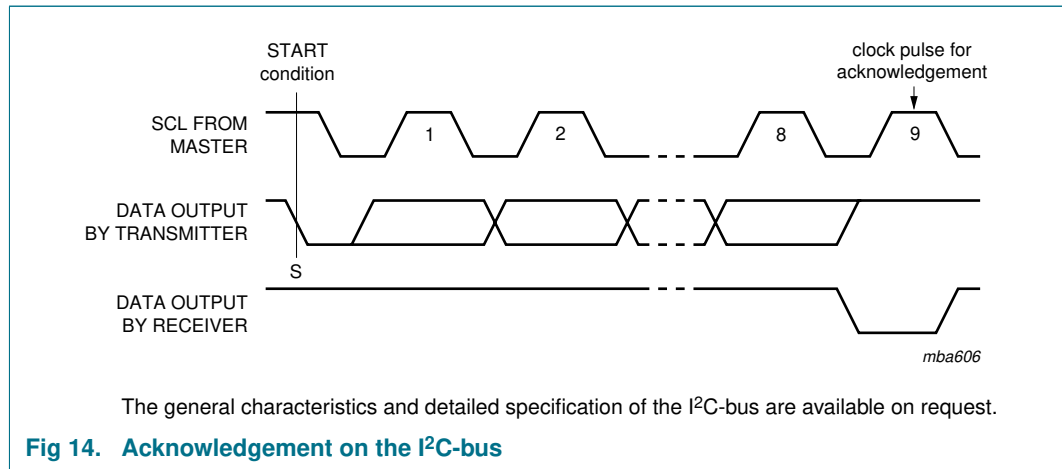


**Fig 12. Definition of START and STOP condition**



**Fig 13. System configuration**

The general characteristics and detailed specification of the I2C-bus are available on request.

**Fig 14. Acknowledgement on the I2C-bus**

### 8.8.5 I2C-bus controller

The I2C-bus controller detects the I2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I2C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

### 8.8.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.
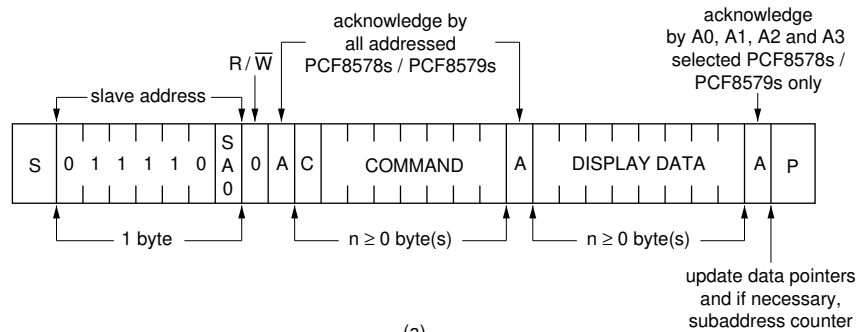
### 8.8.7 I2C-bus protocol

Two 7-bit slave addresses (0111 100 and 0111 101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either logic 0 ($V_{SS}$) or logic 1 ($V_{DD}$). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I2C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I2C-bus for very large applications.
2. The use of two types of LCD multiplex schemes on the same I2C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I2C-bus protocol is shown in Figure 15. All communications are initiated with a START condition (S) from the I2C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I2C-bus master issues a STOP condition (P).

(a)

*msa830*

a. Master transmits to slave receiver (WRITE mode)
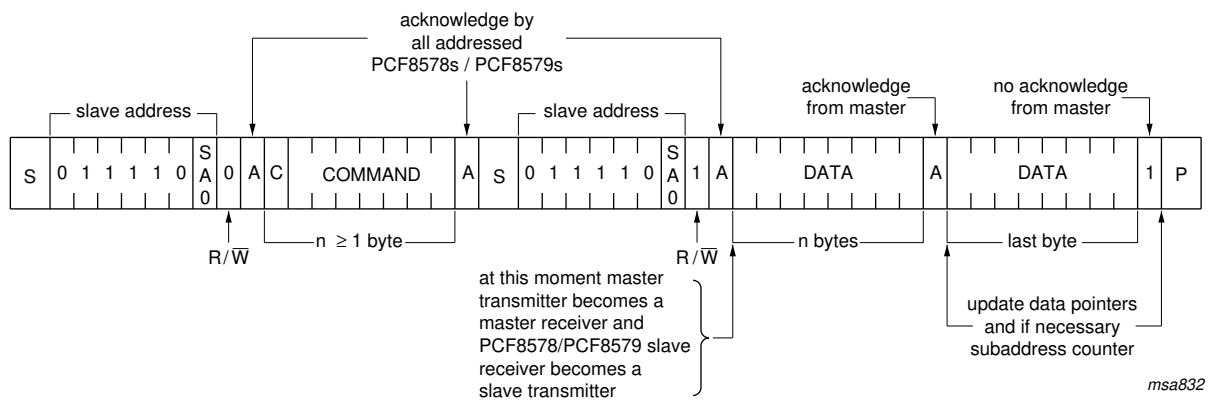


(b)

*msa832*

b. Master reads after sending command string (write commands; read data)
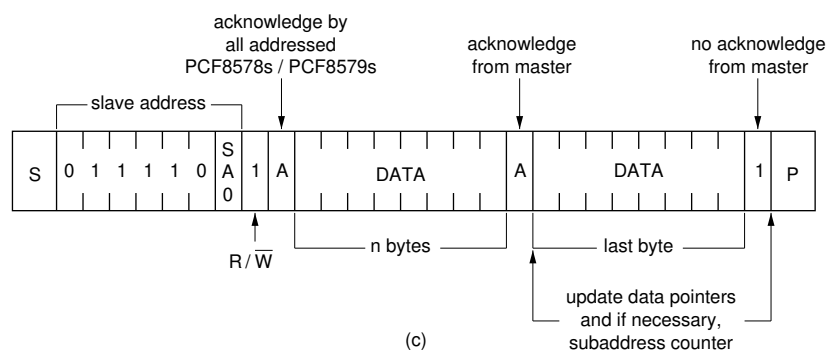


(c)

*msa831*

c. Master reads slave immediately after sending slave address (READ mode)

**Fig 15.  I²C-bus protocol**

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The

master receiver must signal an end of data to the slave transmitter, by not generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a STOP condition (P).

Display bytes are written into, or read from the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to $V_{SS}$ or $V_{DD}$ to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated to a unique hardware subaddress.

## 8.9 Display RAM

The PCF8578 contains a $32 \times 40$-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes ($4 \times 8 \times 40$ bits). During RAM access, data is transferred to and from the RAM via the I²C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579. There is a direct correspondence between X-address and column output number.

### 8.9.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I²C-bus.

### 8.9.2 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter match with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

## 8.10 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus.

The five commands available to the PCF8578 are defined in Table 9.

**Table 9.    Definition of PCF8578 commands**

| Command | Operation code | | | | | | | | Reference |
|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| set-mode | C | 1 | 0 | T | E[1:0] | | M[1:0] | | Table 11 |
| set-start-bank | C | 1 | 1 | 1 | 1 | 1 | B[1:0] | | Table 12 |
| device-select | C | 1 | 1 | 0 | A[3:0] | | | | Table 13 |
| RAM-access | C | 1 | 1 | 1 | G[1:0] | | Y[1:0] | | Table 14 |
| load-X-address | C | 0 | X[5:0] | | | | | | Table 15 |

The most-significant bit of a command is the continuation bit  C (see Table 10 and Figure 16). Commands are transferred in WRITE mode only.

**Table 10. C bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | | continue bit |
| | | 0 | last control byte in the transfer; next byte will be regarded as display data |
| | | 1 | control bytes continue; next byte will be a command too |



C = 0; last command.

C = 1; commands continue.

**Fig 16. General information of command byte**
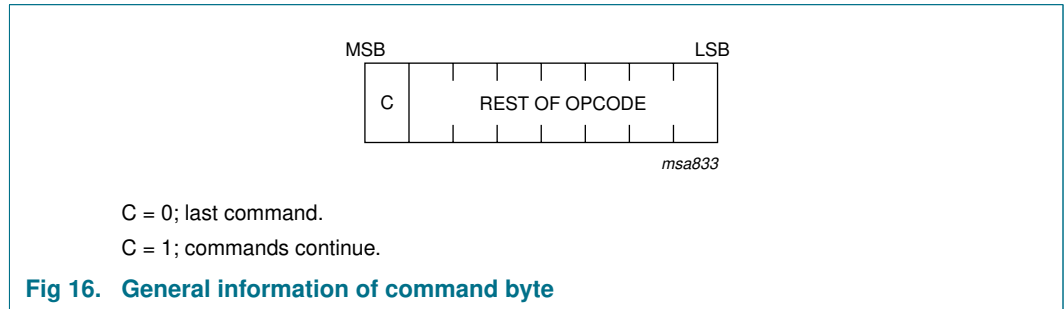
**Table 11. Set-mode - command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | 0, 1 | see Table 10 |
| 6, 5 | - | 10 | fixed value |
| 4 | T | | display mode |
| | | 0 | row mode |
| | | 1 | mixed mode |
| 3, 2 | E[1:0] | | display status |
| | | 00 | blank |
| | | 01 | normal |
| | | 10 | all segments on |
| | | 11 | inverse video |
| 1, 0 | M[1:0] | | LCD drive mode |
| | | 01 | 1:8 MUX (8 rows) |
| | | 10 | 1:16 MUX (16 rows) |
| | | 11 | 1:24 MUX (24 rows) |
| | | 00 | 1:32 MUX (32 rows) |

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**Table 12.   Set-start-bank - command bit description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 | C | 0, 1 | see Table 10 |
| 6 to 2 | - | 11111 | fixed value |
| 1, 0 | B[1:0] | | start bank pointer (see Figure 20)[1] |
| | | 00 | bank 0 |
| | | 01 | bank 1 |
| | | 10 | bank 2 |
| | | 11 | bank 3 |

[1]   Useful for scrolling, pseudo-motion and background preparation of new display content.

**Table 13.   Device-select - command bit description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 | C | 0, 1 | see Table 10 |
| 6 to 4 | - | 110 | fixed value |
| 3 to 0 | A[3:0] | 0 to 15[1] | hardware subaddress; |
| | | | 4 bit binary value; transferred to the subaddress counter to define one of sixteen hardware subaddresses |

[1]   Values shown in decimal.

**Table 14.   RAM-access - command bit description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 | C | 0, 1 | see Table 10 |
| 6 to 4 | - | 111 | fixed value |
| 3, 2 | G[1:0] | | RAM access mode; |
| | | | defines the auto-increment behavior of the address for RAM access (see Figure 18) |
| | | 00 | character |
| | | 01 | half-graphic |
| | | 10 | full-graphic |
| | | 11 | not allowed[1] |
| 1, 0 | Y[1:0] | 0 to 3[2] | RAM row address; |
| | | | two bits of immediate data, transferred to the Y-address pointer to define one of four display RAM rows (see Figure 17) |

[1]   See operation code for set-start-bank in Table 12.

[2]   Values shown in decimal.

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**Table 15.   Load-X-address - command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | 0, 1 | see Table 10 |
| 6 | - | 0 | fixed value |
| 5 to 0 | X[5:0] | 0 to 39[1] | RAM column address; |
|  |  |  | six bits of immediate data, transferred to the X-address pointer to define one of forty display RAM columns (see Figure 17) |

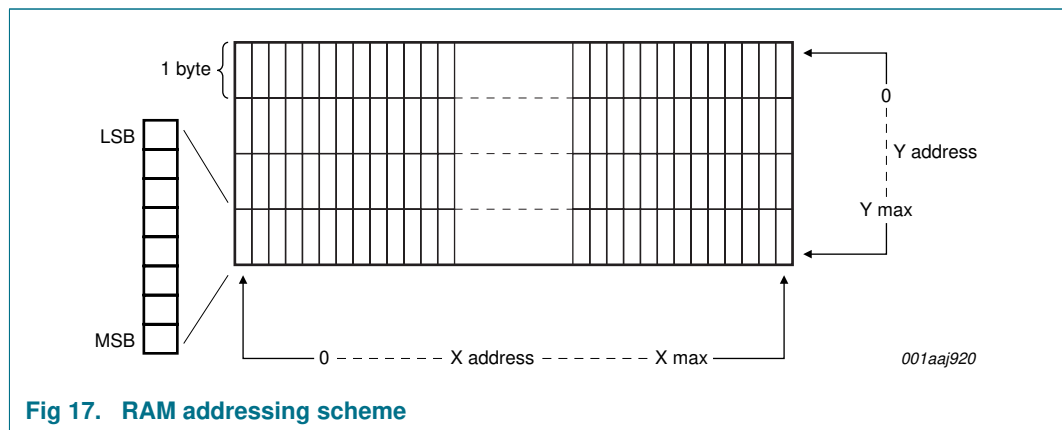[1]   Values shown in decimal.

## 8.11  RAM access



**Fig 17.   RAM addressing scheme**

RAM operations are only possible when the PCF8578 is in mixed mode. In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM-access modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by the bits G[1:0] of the RAM-access command. The RAM-access command controls the order in which data is written to or read from the RAM (see Figure 18).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Figure 19):

- Device subaddress (specified by the device-select command)
- RAM X-address (specified by the bits X[5:0] of the load-X-address command)
- RAM bank (specified by the bits Y[1:0] of the RAM-access command)

Subsequent data bytes will be written or read according to the chosen RAM-access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.
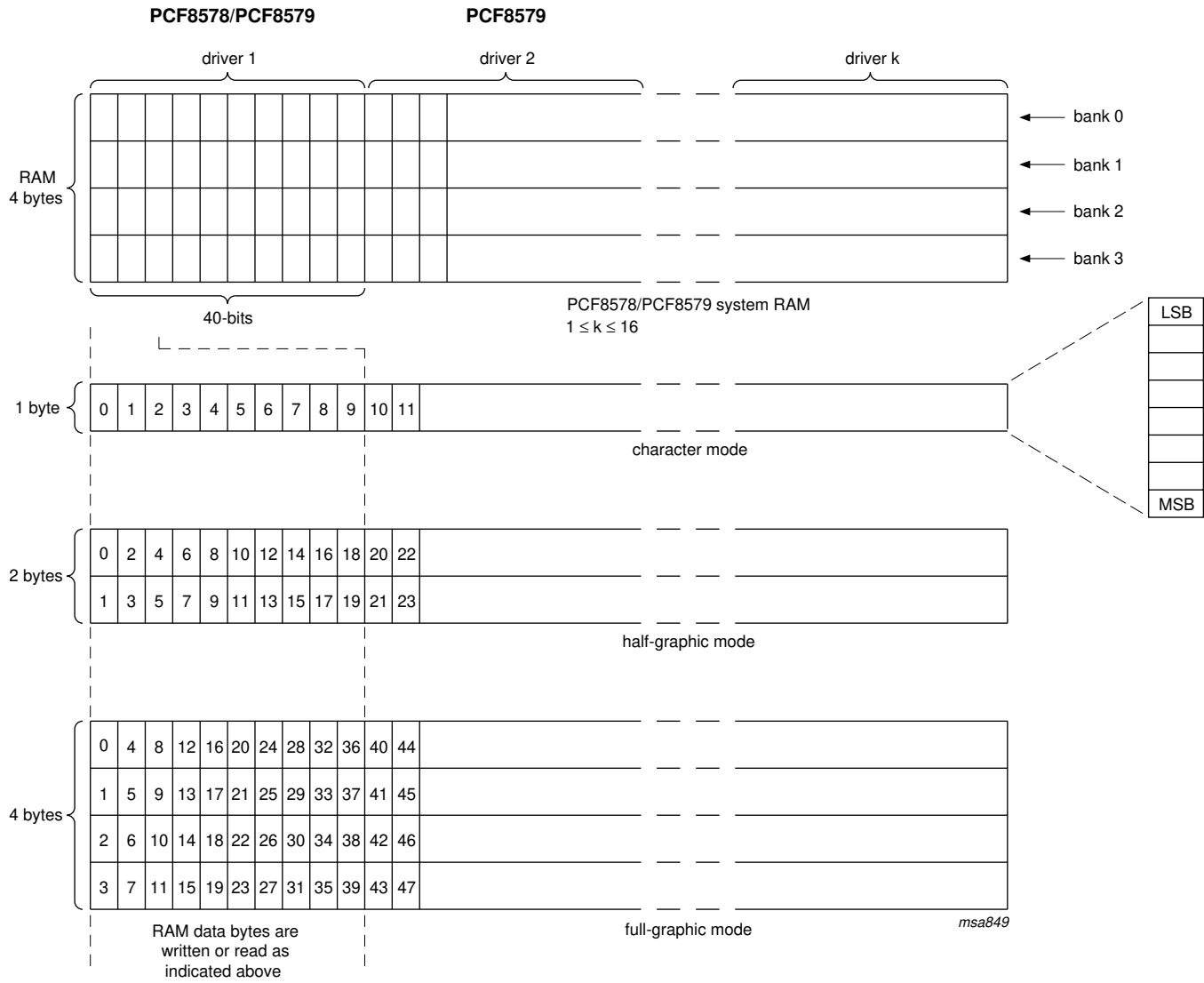
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**PCF8578/PCF8579**  driver 1

**PCF8579**  driver 2

driver k

bank 0
bank 1
bank 2
bank 3

RAM
4 bytes

40-bits

PCF8578/PCF8579 system RAM
$1 \leq k \leq 16$

1 byte | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

LSB

MSB

character mode

2 bytes
| 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 |
| 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 |

half-graphic mode

4 bytes
| 0 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | 36 | 40 | 44 |
| 1 | 5 | 9 | 13 | 17 | 21 | 25 | 29 | 33 | 37 | 41 | 45 |
| 2 | 6 | 10 | 14 | 18 | 22 | 26 | 30 | 34 | 38 | 42 | 46 |
| 3 | 7 | 11 | 15 | 19 | 23 | 27 | 31 | 35 | 39 | 43 | 47 |

RAM data bytes are
written or read as
indicated above

full-graphic mode

msa849

**Fig 18.   RAM access mode**