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PCI Express 1.1 Root Complex Lite x1, x4 IP Core User's Guide

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Chapter 1:

Introduction

PCI Express is a high performance, fully scalable, well defined standard for a wide variety of computing and communications platforms. It has been defined to provide software compatibility with existing PCI drivers and operating systems. Being a packet based serial technology, PCI Express greatly reduces the number of required pins and simplifies board routing and manufacturing. PCI Express is a point-to-point technology, as opposed to the multidrop bus in PCI. Each PCI Express device has the advantage of full duplex communication with its neighbor to greatly increase overall system bandwidth. The basic data rate for a single lane is double that of the 32 bit/33 MHz PCI bus. A four lane link has eight times the data rate in each direction of a conventional bus.

Lattice's PCI Express Root Complex (RC) Lite core provides an x1 or x4 root complex solution from the electrical SERDES interface, physical layer, data link layer and a minimum transaction layer in PCI express protocol stack. This IP is a lighter version of the root complex intended to be used in simple local bus bridging applications. This solution supports the LatticeECP3™ and LatticeECP2M™ FPGA device families and is an extremely economical, high value FPGA platform.

This user's guide covers two versions of the Lattice PCI Express RC-Lite core:

- The **PCI Express x4 RC-Lite Core** targets the LatticeECP3 and LatticeECP2M families of devices.
- The **PCI Express x1 RC-Lite Core** targets the LatticeECP3 and LatticeECP2M families. This is a reduced LUT count x1 core with a 16-bit datapath.

Refer to Lattice's PCIe Solutions web site at:

http://www.latticesemi.com/solutions/technologysolutions/pciexpresssolutions.cfm?source=topnav

Quick Facts

Table 1-1 gives quick facts about the PCI Express RC-Lite IP core.

Table 1-1. PCI Express RC-Lite IP Core Quick Facts

		PCI Express RC-Lite IP Configuration			
		x4 RC		**Native x1 RC**	
Core Requirements	FPGA Families Supported	LatticeECP3 and LatticeECP2M			
	Minimal Device Needed [1]	LFE3-17E-7FN484C	LFE2M-20E-6F484C	LFE3-17E-7FN484C	LFE2M-20E-6F484C
Typical Resource Utilization	Targeted Device	LFE3-70E-7FN672C	LFE2M-50E-6F672C	LFE3-70E-7FN672C	LFE2M-50E-6F672C
	Data Path Width	64	64	16	16
	LUTs	10650	10900	4700	4800
	sysMEM EBRs	9	9	5	5
	Registers	8500	8500	3100	3150
Design Tool Support	Lattice Implementation	Diamond® 1.1 or ispLEVER® 8.1			
	Synthesis	Synopsys® Synplify® Pro for Lattice D-2009.12L-1			
		Mentor Graphics® Precision® RTL			
	Simulation	Aldec Active-HDL® 8.2 (Windows only, Verilog and VHDL)			
		Mentor Graphics ModelSim® SE 6.5F (Verilog Only)			
		Cadence® NC-Verilog® (Linux only)			

1. The packages specified in the Minimal Device Needed row relate to the many user interface signals implemented as I/Os in the evaluation design. Depending on the application, it might be possible to implement a design in a package with fewer I/O pins since the majority of the user interface signals are terminated inside the FPGA.

Features

The Lattice PCI Express RC-Lite IP core supports the following features.

PHY Layer

- 2.5 Gbps CML electrical interface
- PCI Express 1.1 electrical compliance
- Many options for signal integrity including differential output voltage, transmit pre-emphasis and receiver equalization
- Serialization and de-serialization
- 8b10b symbol encoding/decoding
- Link state machine for symbol alignment
- Clock tolerance compensation supports +/- 300 ppm
- Framing and application of symbols to lanes
- Data scrambling and de-scrambling
- Lane-to-lane de-skew
- Link Training and Status State Machine (LTSSM)
  - Electrical idle generation
  - Receiver detection
  - TS1/TS2 generation/detection
  - Lane polarity inversion
  - Link width negotiation
  - Higher layer control to jump to defined states

Data Link Layer

- Data link control and management state machine
- Flow control initialization
- Ack/Nak DLLP generation/termination
- LCRC generation/checking
- Sequence number appending/checking/removing
- Retry buffer and management
- Receiver buffer

Transaction Layer

- Transmit and Receive Flow control
- Malformed and poisoned TLP detection
- Optional ECRC generation/checking
- INTx message TLP decoding and interrupt signaling to user
- Error message TLP decoding and signaling to user.
- 128, 256, 512, 1k, 2k or 4k bytes maximum payload size

Top Level IP Support

- 125 MHz user interface
  - x4 supports a 64-bit data path
  - x1 supports a 16-bit data path
- In transmit, user creates TLPs without ECRC, LCRC, or sequence number
- In receive, user receives valid TLPs without ECRC, LCRC, or sequence number
- Credit interface for transmit and receive for PH, PD, NPH, NPD, CPLH, CPLD credit types
- Higher layer control of LTSSM via ports

Functional Description

This chapter provides a functional description of the Lattice PCI Express RC-Lite IP core.

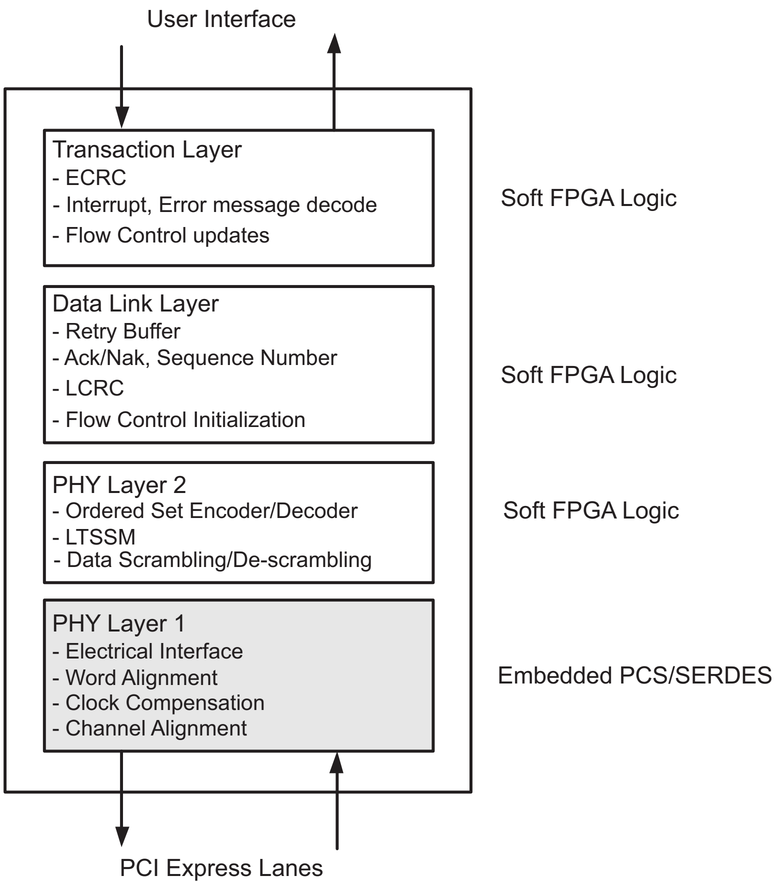
Overview

The PCI Express RC-Lite IP core is implemented in several different FPGA technologies. These technologies include soft FPGA fabric elements such as LUTs, registers, embedded block RAMs (EBRs) and embedded hard elements with the PCS/SERDES.

The IPexpress™ tool is used to customize and create a complete IP module for the user to instantiate in a design. Inside the module created by the IPexpress tool are several blocks implemented in heterogeneous technologies. All of the connectivity is provided, allowing the user to interact at the top level of the IP core.

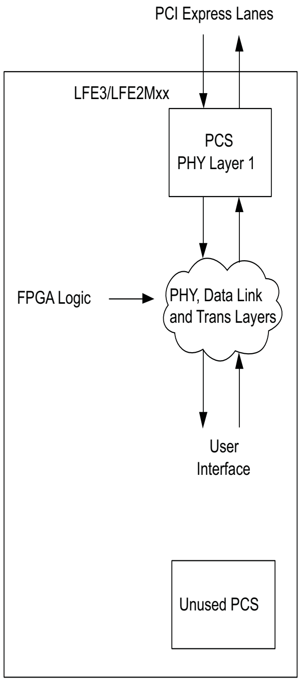
Figure 2-1 provides a high-level block diagram to illustrate the main functional blocks and the technology used to implement PCI Express RC-Lite IP core functions.

Figure 2-1. .PCI Express RC-Lite IP Core Technology and Functions



As the PCI Express RC-Lite IP core proceeds through the Diamond or ispLEVER software design flow specific technologies are targeted to their specific locations on the device. Figure 2-2 provides implementation representations of the LFE3/LFE2M devices with a PCI Express RC-Lite IP core.

Figure 2-2. PCI Express RC-Lite IP Core Implementation in LatticeECP3 and LatticeECP2M Devices



As shown, the data flow moves in and out of the heterogeneous FPGA technology. The user is responsible for selecting the location of the hard SERDES/PCS blocks as described in "Overview" on page 7. The FPGA logic placement and routing is the job of the Diamond or ispLEVER design tools to select regions nearby the hard SERDES/PCS blocks to achieve the timing goals.

Figure 2-3 provides a high-level interface representation.

Figure 2-3. PCI Express RC-Lite IP Core Interfaces

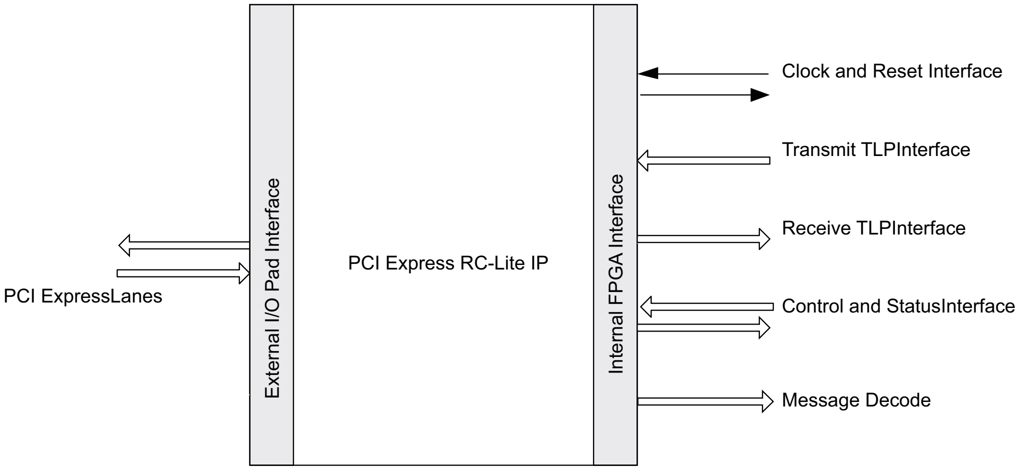


Table 2-1 provides the list of ports and descriptions for the PCI Express RC-Lite IP core.

Table 2-1. PCI Express RC-Lite IP Core Port List

Port Name	Direction	Clock	Description
Clock and Reset Interface			
refclk[p,n]	Input		100 MHz PCI Express differential reference clock used to generate the 2.5 Gbps data.
sys_clk_125	Output		125 MHz clock derived from refclk to be used in the user application.
rst_n	Input		Active-low asynchronous data path and state machine reset. This port will be connected to the GSR for the entire device. This reset is pulsed after bit stream download and will not need to be asserted by the user.
hdin[p,n]_[0,1,2,3]	Input		PCI Express 2.5 Gbps CML inputs for lanes 0,1,2, and 3. The port “flip_lanes” is used to define the connection of PCS/SERDES channel to PCI Express lane. flip_lanes=0 hdin[p,n]_0 - PCI Express Lane 0 hdin[p,n]_1 - PCI Express Lane 1 hdin[p,n]_2 - PCI Express Lane 2 hdin[p,n]_3 - PCI Express Lane 3 flip_lanes=1 hdin[p,n]_0 - PCI Express Lane 3 hdin[p,n]_1 - PCI Express Lane 2 hdin[p,n]_2 - PCI Express Lane 1 hdin[p,n]_3 - PCI Express Lane 0

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
hdout[p,n]_[0,1,2,3]	Output		PCI Express 2.5 Gbps CML outputs for lanes 0,1,2, and 3. The port "flip_lanes" is used to define the connection of PCS/SERDES channel to PCI Express lane. flip_lanes=0 hdout[p,n]_0 - PCI Express Lane 0 hdout[p,n]_1 - PCI Express Lane 1 hdout[p,n]_2 - PCI Express Lane 2 hdout[p,n]_3 - PCI Express Lane 3 flip_lanes=1 hdout[p,n]_0 - PCI Express Lane 3 hdout[p,n]_1 - PCI Express Lane 2 hdout[p,n]_2 - PCI Express Lane 1 hdout[p,n]_3 - PCI Express Lane 0
Transmit TLP Interface			
tx_data_vc0[n:0]	Input	sys_clk_125	x4 Transmit data bus [63:56] Byte N [55:48] Byte N+1 [47:40] Byte N+2 [39:32] Byte N+3 [31:24] Byte N+4 [23:16] Byte N+5 [15: 8] Byte N+6 [7: 0] Byte N+7 x1 Transmit data bus [15:8] Byte N [7:0] Byte N+1
tx_req_vc0	Input	sys_clk_125	Active High transmit request. This port is asserted when the user wants to send a TLP. If several TLPs will be provided in a burst, this port can remain High until all TLPs have been sent.
tx_rdy_vc0	Output	sys_clk_125	Active High transmit ready indicator. Tx_st should be provided next clock cycle after tx_rdy is High.This port will go Low between TLPs.
tx_st_vc0	Input	sys_clk_125	Active High transmit start of TLP indicator.
tx_end_vc0	Input	sys_clk_125	Active High transmit end of TLP indicator. This signal must go Low at the end of the TLP.
tx_nlfy_vc0	Input	sys_clk_125	Active High transmit nullify TLP. Can occur anywhere during the TLP. If tx_nlfy_vc0 is asserted to nullify a TLP the tx_end_vc0 port should not be asserted. The tx_nlfy_vc0 terminates the TLP.
tx_dwen_vc0	Input	sys_clk_125	Active High transmit 32-bit word indicator. Used if only bits [63:32] provide valid data. This port is available only on the x4 core.
tx_val	Output	sys_clk_125	Active High transmit clock enable. When a x4 is downgraded to a x1, this signal is used as the clock enable to downshift the transmit bandwidth. This port is available only on the x4 core.

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
tx_ca_[ph,nph,cplh]_vc0[8:0]	Output	sys_clk_125	Transmit Interface credit available bus. This port will decrement as TLPs are sent and increment as UpdateFCs are received. Ph - Posted header Nph - Non-posted header Cplh - Completion header This credit interface is only updated when an UpdateFC DLLP is received from the PCI Express line. [8] - This bit indicates the receiver has infinite credits. If this bit is High then bits. [7:0] should be ignored. [7:0] - The amount of credits available at the receiver.
tx_ca_[pd,npd,cpld]_vc0[12:0]	Output	sys_clk_125	Transmit Interface credit available bus. This port will decrement as TLPs are sent and increment as UpdateFCs are received. pd - posted data npd - non-posted data cpld - completion data [12] - This bit indicates the receiver has infinite credits. If this bit is High, then bits [11:0] should be ignored. [11:0] - The amount of credits available at the receiver.

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
Receive TLP Interface			
rx_data_vc0[n:0]	Output	sys_clk_125	x4 Receive data bus [63:56] Byte N [55:48] Byte N+1 [47:40] Byte N+2 [39:32] Byte N+3 [31:24] Byte N+4 [23:16] Byte N+5 [15: 8] Byte N+6 [7: 0] Byte N+7 x1 Receive data bus [15:8] Byte N [7:0] Byte N+1
rx_st_vc0	Output	sys_clk_125	Active High receive start of TLP indicator.
rx_end_vc0	Output	sys_clk_125	Active High receive end of TLP indicator.
rx_dwen_vc0	Output	sys_clk_125	Active High 32-bit word indicator. Used if only bits [63:32] contain valid data. This port is available only on the x4 core.
rx_ecrc_err_vc0	Output	sys_clk_125	Active High ECRC error indicator. Indicates a ECRC error in the current TLP. This port is available only if ECRC feature is selected while generating the IP core.
rx_pois_tlp_vc0	Output	sys_clk_125	Active High poisoned TLP indicator. Asserted if “poisoned (EP) “ bits is set in any TLP with data.
rx_malf_tlp_vc0	Output	sys_clk_125	Active High malformed TLP indicator. Indicates a problem with the current TLPs length or format.
[ph,pd, nph,npd,cplh,cpld] _buf_status_vc0	Input	sys_clk_125	Active High user buffer full status indicator. When asserted, an UpdateFC will be sent for the type specified as soon as possible without waiting for the UpdateFC timer to expire.
[ph,nph,cplh]_processed_vc0	Input	sys_clk_125	Active High indicator to inform the IP core of how many credits have been processed. Each clock cycle High counts as one credit processed. The core will generate the required UpdateFC DLLP when either the UpdateFC timer expires or enough credits have been processed.
[pd,npd,cpld]_processed_vc0	Input	sys_clk_125	Active High enable for [pd, npd,cpld]_num_vc0 port. The user should place the number of data credits processed on the [pd, npd,cpld]_num_vc0 port and then assert [pd, npd]_processed_vc0 for one clock cycle. The core will generate the required UpdateFC DLLP when either the UpdateFC timer expires or enough credits have been processed.
[pd,npd]_num_vc0[7:0]	Input	sys_clk_125	This port provides the number of PD or NPD or CPLD credits processed. It is enabled by the [pd, npd,cpld]_processed_vc0 port.
Control and Status			
			PHYSICAL LAYER
flip_lanes	Input	Async	Reverses the lane connections to the SERDES. This function is used to provide flexibility for the PCB layout. The “Locating” section later in this document describes how this function can be used. 0-Lane 0 connects to SERDES Channel 0, etc. 1-Lane 0 connects to SERDES Channel 3, etc.

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
phy_ltssm_state[3:0]	Output	sys_clk_125	PHY Layer LTSSM current state 0000 - Detect 0001 - Polling 0010 - Config 0011 - L0 0100 - L0s 0101 - L1 0110 - L2 0111 - Recovery 1000 - Loopback 1001 - Hot Reset 1010 - Disabled

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
phy_ltssm_substate[2:0]	Output	sys_clk_125	PHY Layer LTSSM current sub state. Each major LTSSM state has a series of sub states. When phy_ltssm_state=DETECT 000 - DET_WAIT 001 - DET_QUIET 010 - DET_GODET1 011 - DET_ACTIVE1 100 - DET_WAIT12MS 101 - DET_GODET2 110 - DET_ACTIVE2 111 - DET_EXIT When phy_ltssm_state=POLLING 000 - POL_WAIT 001 - POL_ACTIVE 010 - POL_COMPLIANCE 011 - POL_CONFIG 100 - POL_EXIT When phy_ltssm_state=CONFIG 000 - CFG_WAIT 001 - CFG_LINK_WIDTH_ST 010 - CFG_LINK_WIDTH_ACC 011 - CFG_LANE_NUM_WAIT 100 - CFG_LANE_NUM_ACC 101 - CFG_COMPLETE 110 - CFG_IDLE 111 - CFG_EXIT When phy_ltssm_state=L0 000 - L0_WAIT 001 - L0_L0 010 - L0_L0RX 011 - L0_L0TX 100 - L0_EIDLE_0 101 - L0_EIDLE_1 110 - L0_EXIT When phy_ltssm_state=L0s 000 - L0s_RX_WAIT 001 - L0s_RX_ENTRY 010 - L0s_RX_IDLE 011 - L0s_RX_FTS 100 - L0s_RX_EXIT When phy_ltssm_state=L1 000 - L1_WAIT 001 - L1_ENTRY 010 - L1_IDLE 011 - L1_EXIT When phy_ltssm_state=L2 000 - L2_WAIT 001 - L2_IDLE
phy_cfgln_sum[2:0]	Output	sys_clk_125	Link Width 000 - No link defined 001 - Link width = 1 100 - Link width = 4

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
phy_pol_compliance	Output	sys_clk_125	Active High indicator that the LTSSM is in the Polling.Compliance state.
phy_force_cntl[3:0]	Input	sys_clk_125	These signals to be used only for debug purpose. [0] - force_lsm_active - Forces the Link State Machine for all of the channels to the linked state. [1] - force_rec_ei - Forces the detection of a received electrical idle. [2] - force_phy_status - Forces the detection of a receiver during the LTSSM Detect state on all of the channels. [3] - force_disable_scr - Disables scrambler and de-scrambler.
phy_ltssm_cntl[15:0]	Input	sys_clk_125	[0] – no_pcie_train - Active High signal disables LTSSM training and forces the LTSSM to L0 as a x4 configuration. This is intended to be used in simulation only to force the LTSSM into the L0 state. [1] - retrain - Active High request to re-train the link when LTSSM is in L0. [2] – hl_disable_scr - Active High to set the disable scrambling bit in the TS1/TS2 sequence [3] – hl_gto_dis – Active High request to go to Disable state when LTSSM is in Config or Recovery. [4] – hl_gto_det – Active High request to go to Detect state when LTSSM is in L2 or Disable. [5] – hl_gto_hrst - Active High request to go to Hot Reset when LTSSM is in Recovery. [6] – hl_gto_l0stx - Active High request to go to L0s when LTSSM is in L0. [7] – hl_gto_l0stxfts - Active High request to go to L0s and transmit FTS when LTSSM is in L0s. [8] – hl_gto_l1 - Active High request to go to L1 when LTSSM is in L0. [9] – hl_gto_l2 - Active High request to go to L2 when LTSSM is in L0. [13:10] – hl_gto_lbk - Active High request to go to Loopback when LTSSM is in Config or Recovery [14] – hl_gto_rcvry - Active High request to go to Recovery when LTSSM is in L0, L0s or L1. [15] – hl_gto_cfg - Active High request to go to Config when LTSSM is in Recovery.
tx_lbk_rdy	Output	sys_clk_125	This output port is used to enable the transmit master loopback data. This port is only available if the Master Loopback feature is enabled in the IPexpress tool.
tx_lbk_kcntl[3:0]	Input	sys_clk_125	This input port is used to indicate a K control word is being sent on tx_lbk_data port. This port is only available if the Master Loopback feature is enabled in the IPexpress tool. **x4 port** [7] - K control on tx_lbk_data[63:56] [6] - K control on tx_lbk_data[55:48] [5] - K control on tx_lbk_data[47:40] [4] - K control on tx_lbk_data[39:32] [3] - K control on tx_lbk_data[31:24] [2] - K control on tx_lbk_data[23:16] [1] - K control on tx_lbk_data[15:8] [0] - K control on tx_lbk_data[7:0] **x1 port** [1] - K control on tx_lbk_data[15:8] [0] - K control on tx_lbk_data[7:0]

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
tx_lbk_data[31:0]	Input	sys_clk_125	This input port is used to send 32-bit data for the master loopback. This port is only available if the Master Loopback feature is enabled in the IPexpress tool. **x4 port** [63:56] - Lane 7 data [55:48] - Lane 6 data [47:40] - Lane 5 data [39:32] - Lane 4 data [31:24] - Lane 3 data [23:16] - Lane 2 data [15:8] - Lane 1 data [7:0] - Lane 0 data **x1 port** [15:8] - Lane 1 data [7:0] - Lane 0 data
rx_lbk_kcntl[3:0]	Output	sys_clk_125	This output port is used to indicate a K control word is being received on rx_lbk_data port. This port is only available if the Master Loopback feature is enabled in the IPexpress tool. **x4 port** [7] - K control on rx_lbk_data[63:56] [6] - K control on rx_lbk_data[55:48] [5] - K control on rx_lbk_data[47:40] [4] - K control on rx_lbk_data[39:32] [3] - K control on rx_lbk_data[31:24] [2] - K control on rx_lbk_data[23:16] [1] - K control on rx_lbk_data[15:8] [0] - K control on rx_lbk_data[7:0] **x1 port** [1] - K control on rx_lbk_data[15:8] [0] - K control on rx_lbk_data[7:0]
rx_lbk_data[31:0]	Output	sys_clk_125	This output port is used to receive 32-bit data for the master loopback. This port is only available if the Master Loopback feature is enabled in the IPexpress tool. **x4 port** [63:56] - Lane 7 data [55:48] - Lane 6 data [47:40] - Lane 5 data [39:32] - Lane 4 data [31:24] - Lane 3 data [23:16] - Lane 2 data [15:8] - Lane 1 data [7:0] - Lane 0 data **x1 port** [15:8] - Lane 1 data [7:0] - Lane 0 data
DATA LINK LAYER			

Table 2-1. PCI Express RC-Lite IP Core Port List (Continued)

Port Name	Direction	Clock	Description
dll_status[7:0]	Output	sys_clk_125	[0] – dl_up - Data Link Layer is in the up and ready to send/receive TLPs from/to Transaction Layer. [1] - dl_init - Data Link Layer is in the DL_Init state. [2] – dl_inactive - Data Link Layer is the DL_Inactive state. [3] – bad_dllp – Data link Layer received a bad DLLP. [4] – dlerr – Data Link Layer Protocol error. [5] – bad_tlp - Data link Layer received a bad TLP. [6] – rply_tout – Indicates a replay timeout [7] – rnum_rlor – Indicates replay number roll over which initiates Link re-training.
tx_dllp_val	Input	sys_clk_125	Active High power message send command. 00 - Nothing to send 01 - Send DLLP using tx_pmtype DLLP 10 - Send DLLP using tx_vsd_data Vendor Defined DLLP 11 - Not used
tx_pmtype[2:0]	Input	sys_clk_125	Transmit power message type 000 - PM Enter L1 001 - PM Enter L2 011 - PM Active State Request L1 100 - PM Request Ack
tx_vsd_data[23:0]	Input	sys_clk_125	Vendor-defined data to send in DLLP.
tx_dllp_sent	Output	sys_clk_125	Requested DLLP was sent.
rxdp_pmd_type[2:0]	Output	sys_clk_125	Receive power message type 000 - PM Enter L1 001 - PM Enter L2 011 - PM Active State Request L1 100 - PM Request Ack
rxdp_vsd_data[23:0]	Output	sys_clk_125	Received vendor-defined DLLP data.
rxdp_dllp_val	Output	sys_clk_125	Active High DLLP received
TRANSACTION LAYER			
ecrc_gen_enb	Input	Async	Active High enable for ECRC generation. When asserted, IP generates and inserts ECRC to transmitting TLPs. When asserted, the TD bit in the transmit TLP header must be set. This port is available only if ECRC feature is selected while generating the IP core.
ecrc_chk_enb	Input	Async	Active High enable for ECRC checking. When asserted, IP checks ECRC in received TLPs. This port is available only if ECRC feature is selected while generating the IP core.
MESSAGE DECODES			
int[a,b,c,d]_n	Output	sys_clk_125	Active Low interrupt wires. 0 – Received Assert INTx message TLP. 1 – Received De-Assert INTx message TLP.
nftl_err_msg	Output	sys_clk_125	Active High signal indicates receiving a NON-FATAL ERROR message TLP.
ftl_err_msg	Output	sys_clk_125	Active High signal indicates receiving a FATAL ERROR message TLP.
corr_err_msg	Output	sys_clk_125	Active High signal indicates receiving a CORRECTABLE ERROR message TLP.

Interface Description

This section describes the datapath user interfaces of the IP core. Both the transmit and receive interfaces use the TLP as the data structure.

Transmit TLP Interface

In the transmit direction, the user must first check the credits available on the far end before sending the TLP. This information is found on the tx_ca_[ph,pd,nph,npd,cplh,cpld]_vc0 bus. There must be enough credits available for the entire TLP to be sent.

The user must then check that the core is ready to send the TLP. This is done by asserting the tx_req_vc0 port and waiting for the assertion of tx_rdy_vc0. If there is enough credit, the user can proceed with sending the data based on tx_rdy_vc0. If the credit becomes insufficient, tx_req_vc0 must be de-asserted on the next clock until enough credit is available. When tx_rdy_vc0 is asserted, the next clock cycle will provide the first 64-bit word of the TLP and will assert tx_st_vc0.

The tx_rdy_vc0 signal will remain High until one clock cycle before the last clock cycle of TLP data (based on the length field of the TLP). This allows the tx_rdy_vc0 to be used as the read enable of a non-pipelined FIFO.

Transmit TLP Interface Waveforms for x4 Core

Figure 2-4 through Figure 2-10 provide timing diagrams for the tx interface signals with a 64-bit datapath.

Figure 2-4. Transmit Interface x4, 3DW Header, 1 DW Data

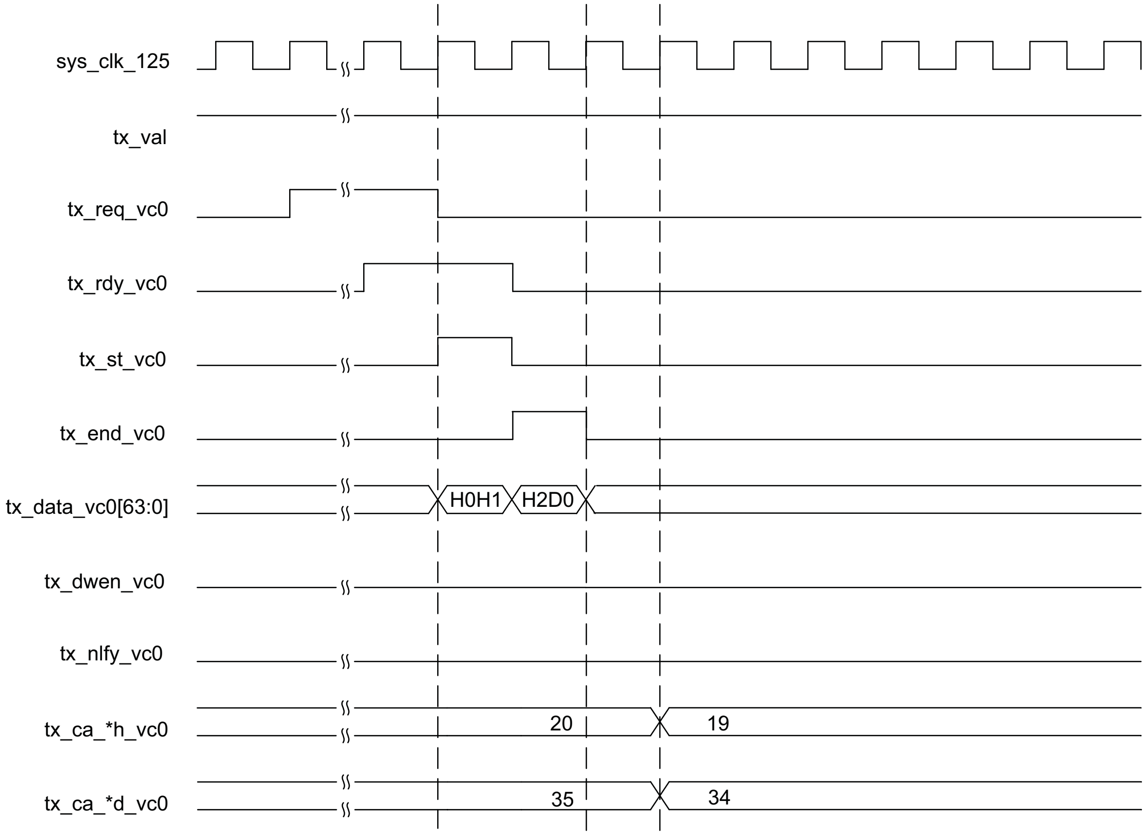


Figure 2-5. Transmit Interface x4, 3DW Header, 2 DW Data

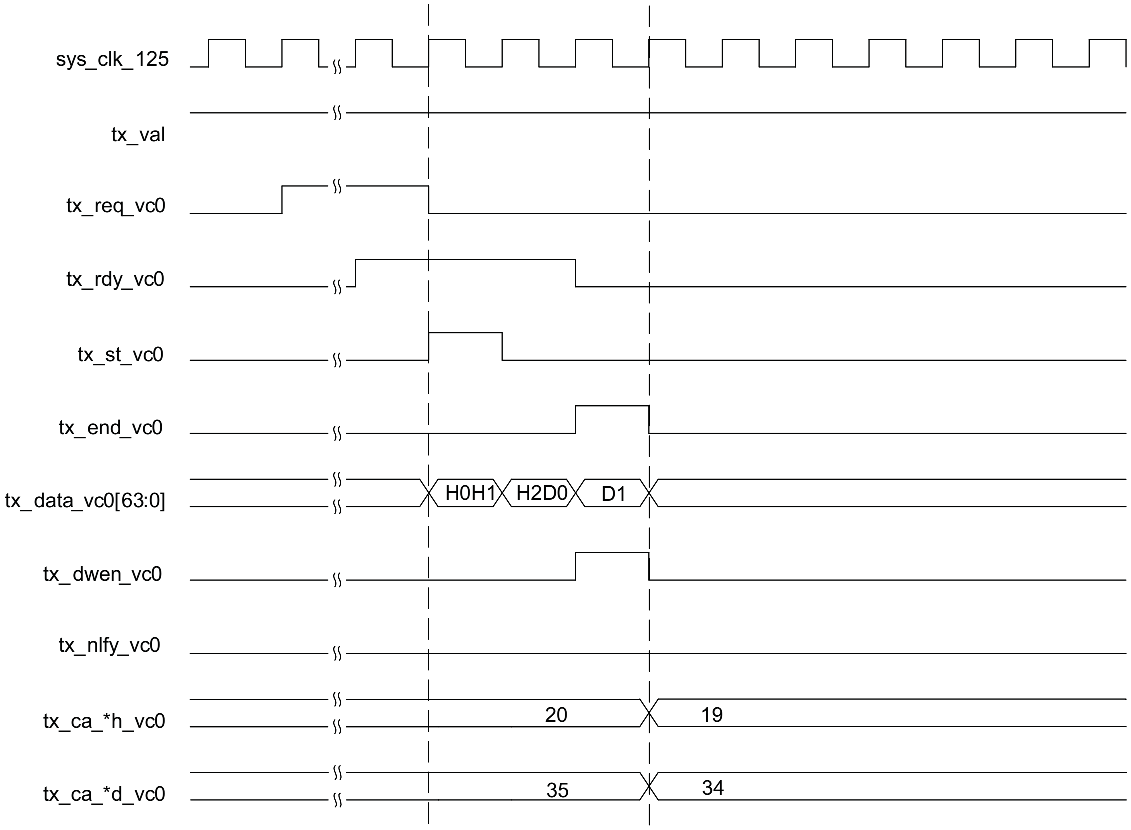


Figure 2-6. Transmit Interface x4, 4DW Header, 0 DW

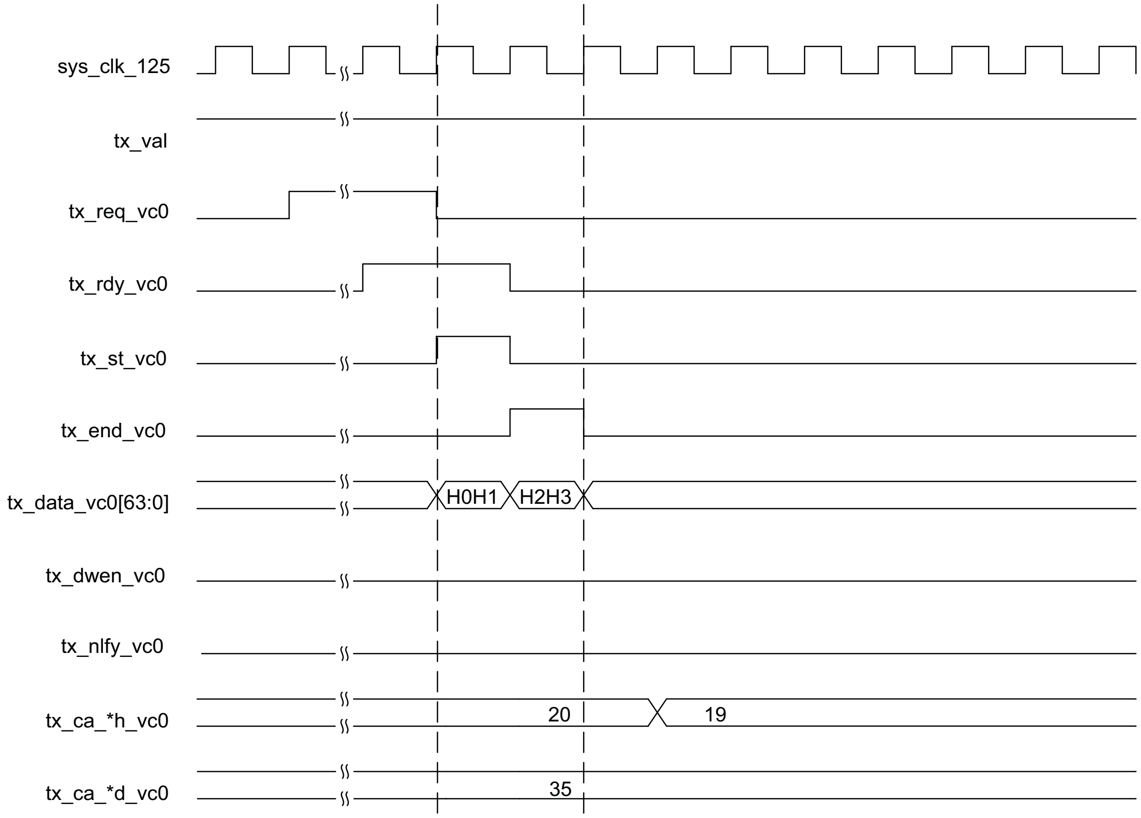


Figure 2-7. Transmit Interface x4, 4DW Header, Odd Number of DWs

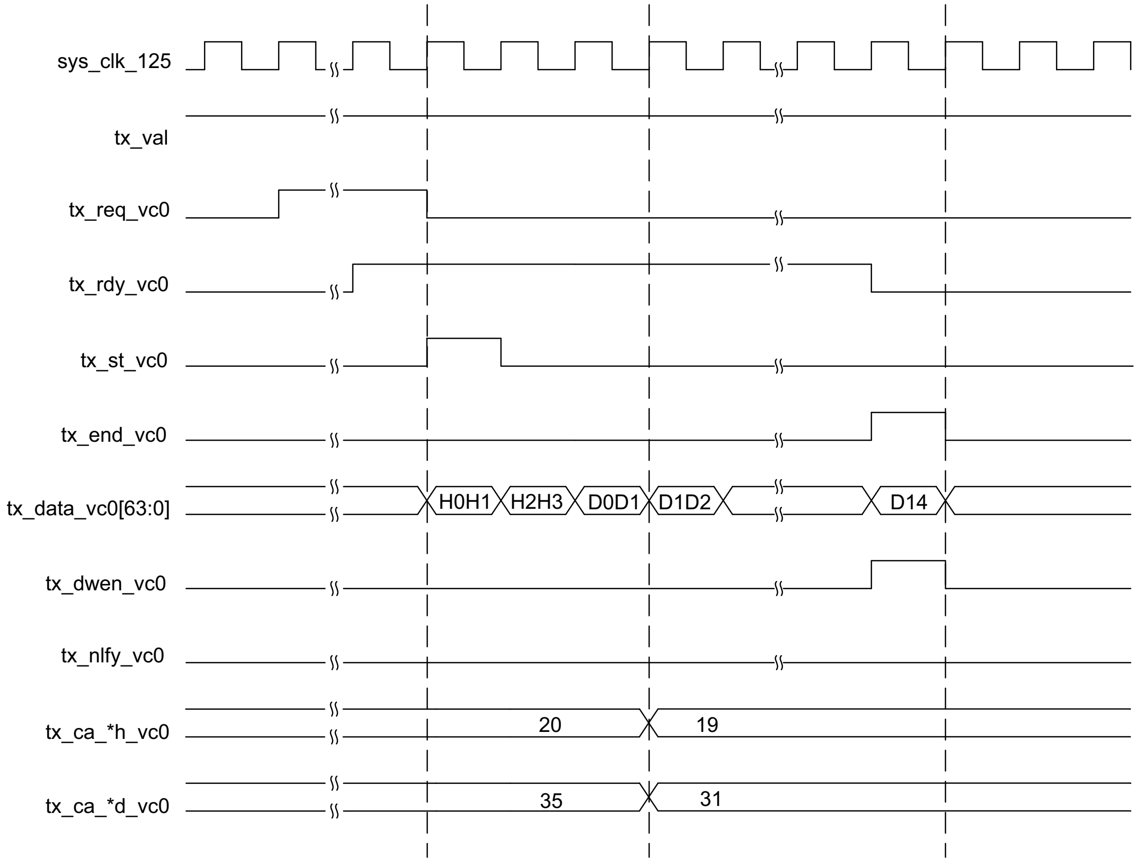


Figure 2-8. Transmit Interface x4, Burst of Two TLPs

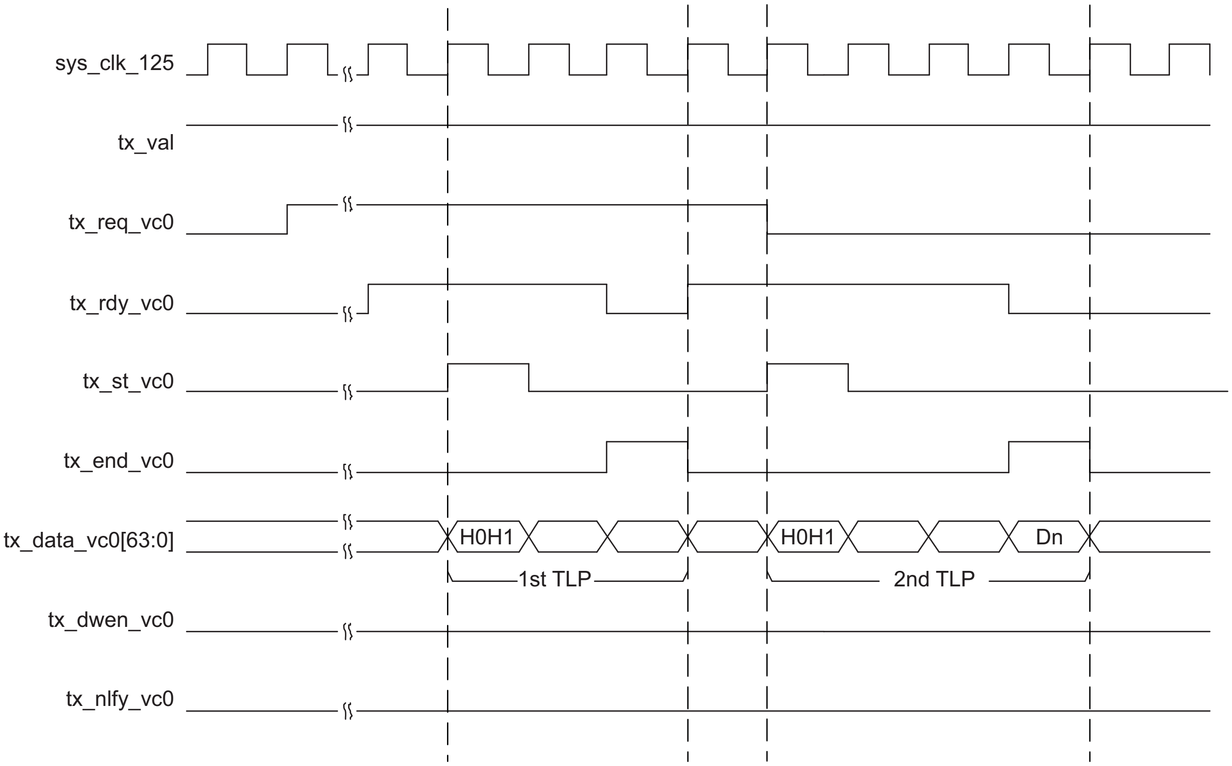


Figure 2-9. Transmit Interface x4, Nullified TLP

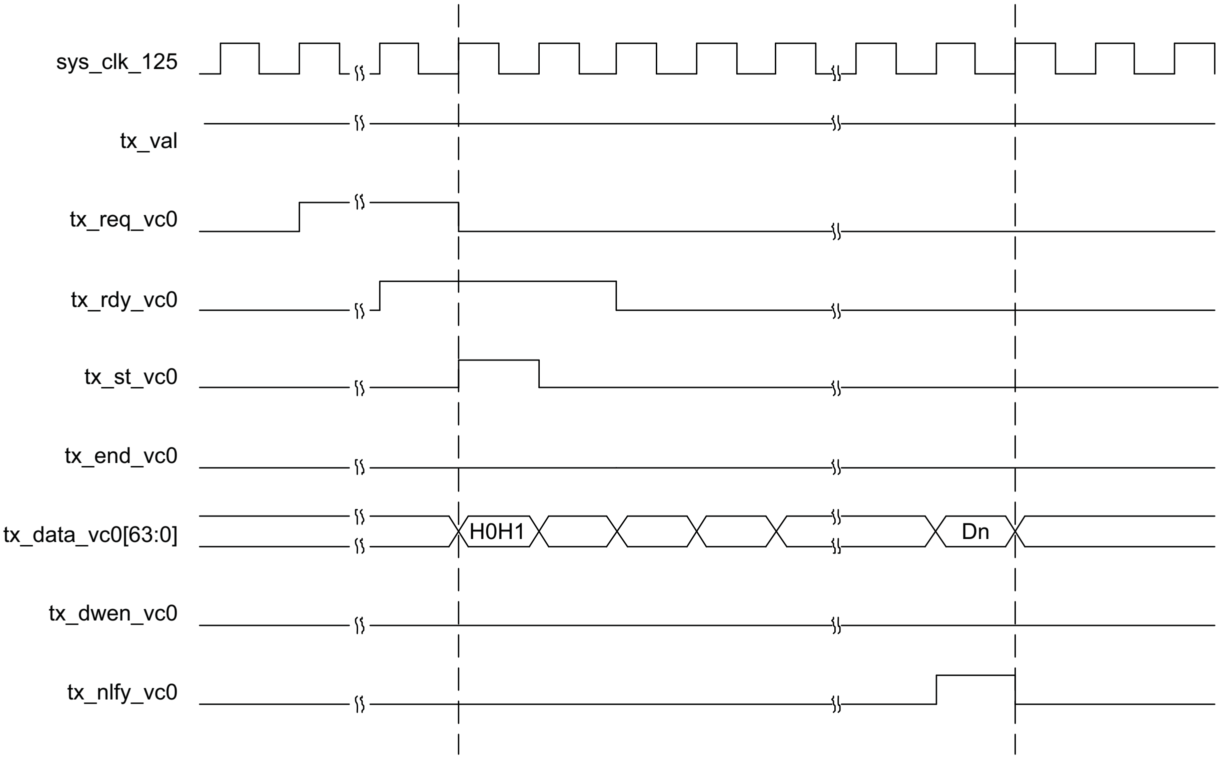
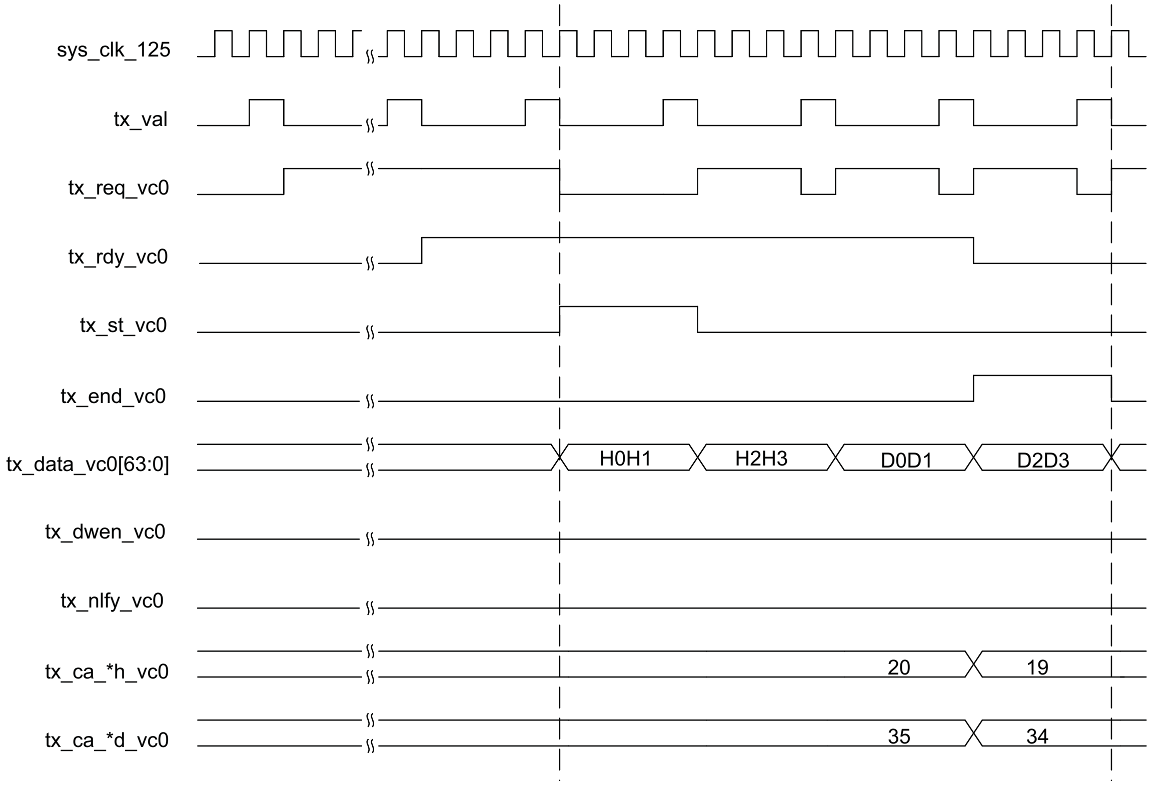


Figure 2-10. Transmit Interface x4 Downgraded to x1 Using tx_val



Transmit TLP Interface Waveforms for x1

Figure 2-11 through Figure 2-13 provide timing diagrams for the transmit interface signals with a 16-bit datapath.

Figure 2-11. Transmit Interface x1, 3DW Header, 1 DW Data

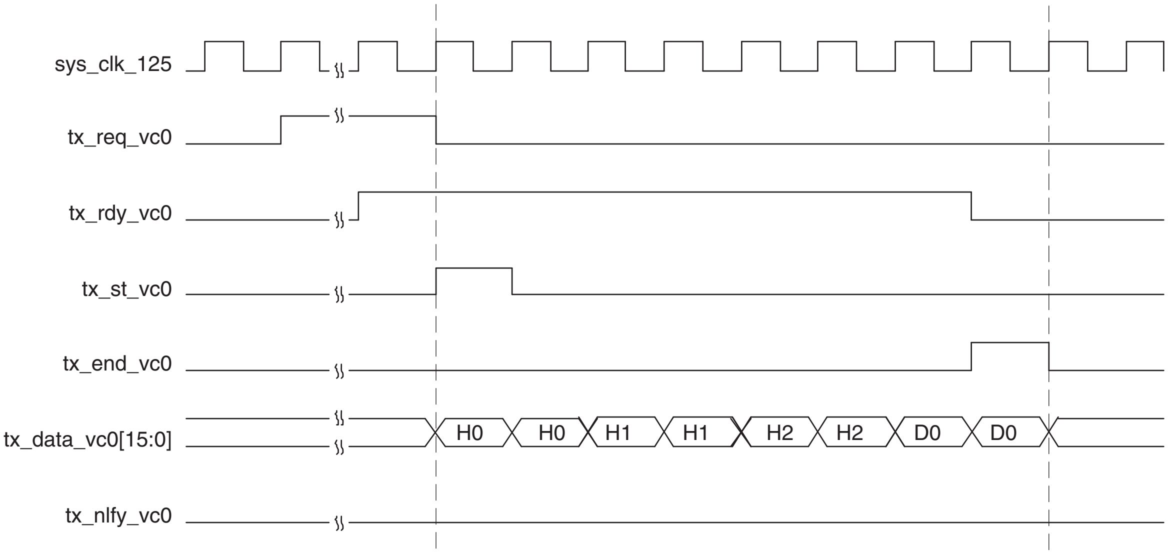


Figure 2-12. Transmit Interface x1, Burst of Two TLPs

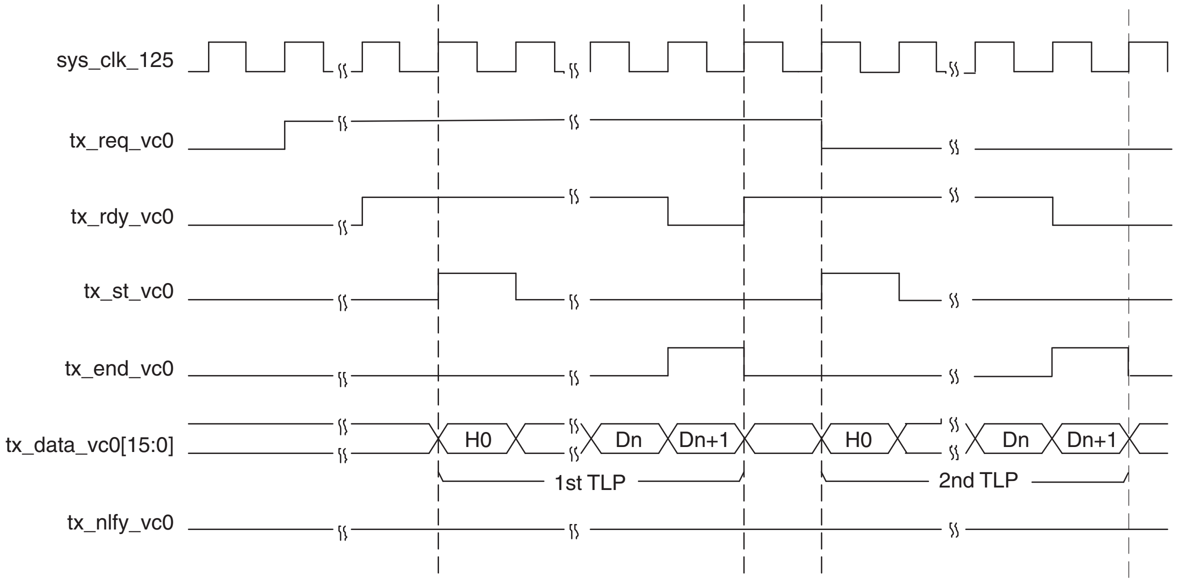
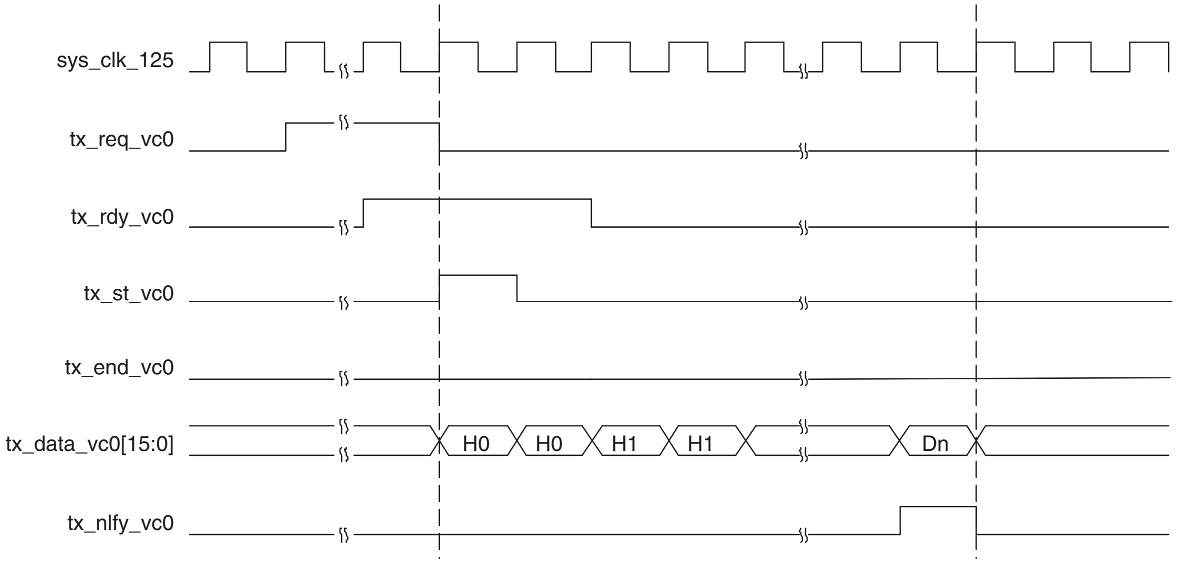


Figure 2-13. Transmit Interface x1, Nullified TLP



Receive TLP Interface

In the receive direction, TLPs will come from the core as they are received on the PCI Express lanes. Interrupt messages and Error Message TLPs are processed by the IP core and corresponding signals are provided through ports. Interrupt message TLPs are decoded to ports inta_n, intb_n, intc_n and Intd_n. Error message TLPs are decoded to ports ftl_err_msg, nftl_err_msg and cor_err_msg. Figure 2-14 through Figure 2-16 provide timing diagrams of the these ports.

When a TLP is sent to the user the rx_st_vc0 signal will be asserted with the first word of the TLP. The remaining TLP data will be provided on consecutive clock cycles until the last word with rx_end_vc0 asserted. If the TLP contains a ECRC error the rx_ecrc_err_vc0 signal will be asserted at the end of the TLP. If the TLP has a length problem the rx_malf_tlp_vc0 will be asserted at any time during the TLP. Figure 2-14 through Figure 2-16 provide timing diagrams of the receive interface.

TLPs come from the receive interface only as fast as they come from the PCI Express lanes. There will always be at least one clock cycle between rx_end_vc0 and the next rx_st_vc0.

Figure 2-14. Receive Interface, Clean TLP

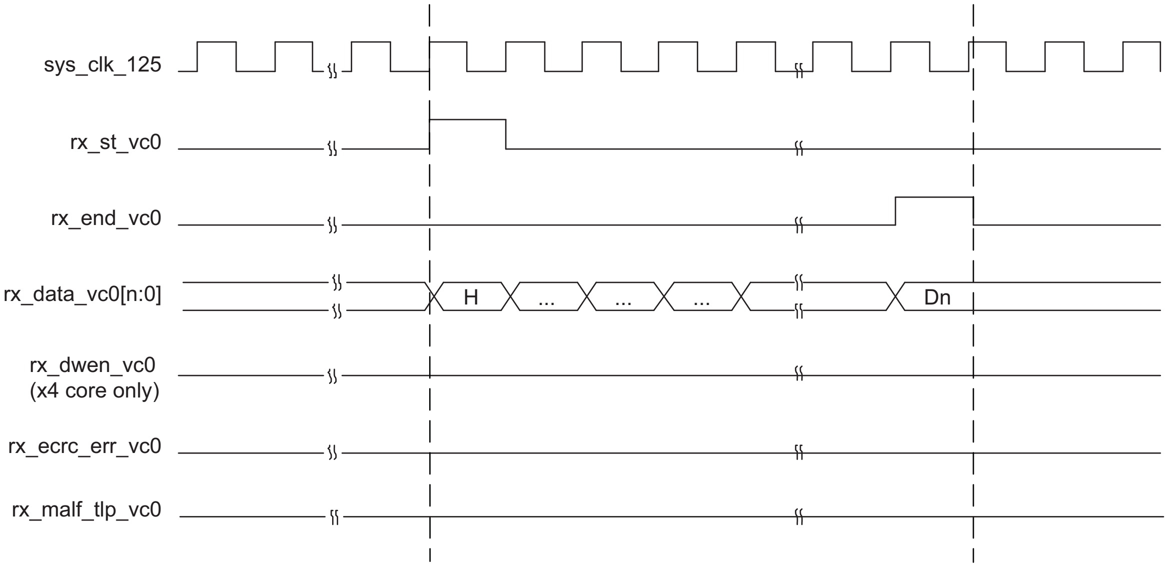
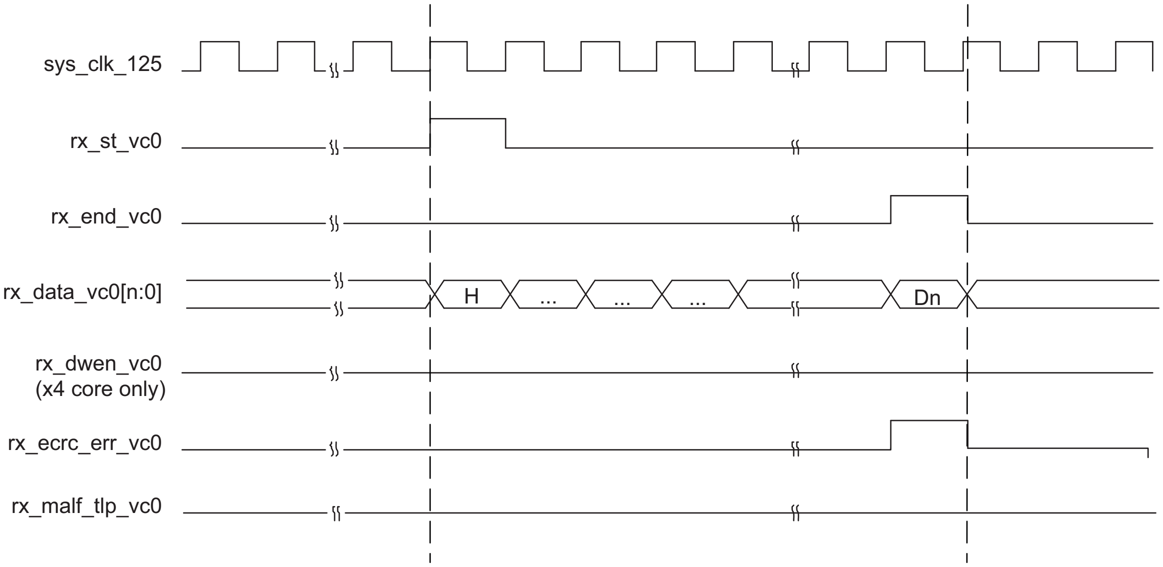


Figure 2-15. Receive Interface, ECRC Errored TLP


sys_clk_125
rx_st_vc0
rx_end_vc0
rx_data_vc0[n:0]
H
...
...
...
Dn
rx_dwen_vc0
(x4 core only)
rx_ecrc_err_vc0
rx_malf_tlp_vc0