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PCI Express x1/x2/x4 Endpoint IP Core

User Guide

FPGA-IPUG-02009 Version 1.8

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1. Introduction

PCI Express is a high performance, fully scalable, well defined standard for a wide variety of computing and communications platforms. It has been defined to provide software compatibility with existing PCI drivers and operating systems. Being a packet based serial technology, PCI Express greatly reduces the number of required pins and simplifies board routing and manufacturing. PCI Express is a point-to-point technology, as opposed to the multidrop bus in PCI. Each PCI Express device has the advantage of full duplex communication with its link partner to greatly increase overall system bandwidth. The basic data rate for a single lane is double that of the 32 bit/33 MHz PCI bus. A four lane link has eight times the data rate in each direction of a conventional bus.

Lattice's PCI Express core provides a x1, x2 or x4 endpoint solution from the electrical SERDES interface to the transaction layer. This solution supports the LatticeECP3™, ECP5™ and ECP5-5G™device families. When used with the LatticeECP3, ECP5 and ECP5-5G family of devices, the PCI Express core is implemented using an extremely economical and high value FPGA platform.

This user guide covers the following versions of the Lattice PCI Express Endpoint IP core:

PCI Express (2.5G) IP Core

- The Native x4 Core targets the LatticeECP3 and ECP5 family of devices.
- The x4 Downgraded x1 Core also targets the LatticeECP3 and ECP5 family. The x4 Downgraded x1 core is a x4 core that uses one channel of SERDES/PCS and a 64-bit data path for x1 link width.
- The x4 Downgraded x2 Core also targets the LatticeECP3 and ECP5 family. The x4 Downgraded x2 core is a x4 core that uses two channels of SERDES/PCS and a 64-bit data path for x2 link width.
- The Native x1 Core targets the LatticeECP3 and ECP5 family of devices. This is a reduced LUT count x1 core with a 16-bit data path.

PCI Express 5G IP Core

- The Native x2 Core targets the Lattice ECP5-5G device. The x2 core uses 2 channels of SERDES/PCS and a 64-bit data path for x2 link width.
- The x2 Downgraded x1 Core targets the Lattice ECP5-5G device. The x2 Downgraded x1 core is a x2 core that uses 1 channel of SERDES/PCS and a 64-bit data path for x1 link width.

1.1. Quick Facts

Table 1.1 provides quick facts about the Lattice PCI Express (2.5G) x1/x2/x4 IP Core.

Table 1.1. PCI Express (2.5G) IP Core Quick Facts

		PCI Express IP Configuration					
		Native x4		Native x1		Downgraded x2	
IP Requirements	FPGA Families Supported	LatticeECP3 and ECP5					
	Minimal Device Needed	LFE317E-7FN484C	LFE5UM-45F-7BG756CES	LFE3-17E-7FN484C	LFE5UM-25F-7BG381C	LFE317E-7FN484C	LFE5UM-45F-7BG756CES
Resource Utilization	Targeted Device	LFE395E-7FPBGA1156C	LFE5UM-85F-7BG756CES	LFE3-95E-7FPBGA1156C	LFE5UM-85F-7BG756CES	LFE395E-7FPBGA1156C	LFE5UM-85F-7BG756CES
	Data Path Width	64	64	16	16	64	64
	LUTs	12200	13900	6040	6207	12900	12200
	sysMEM™ EBRs	11	11	4	4	11	11
	Registers	9746	9763	4027	4188	8899	9746
Design Tool Support	Lattice Implementation	Lattice Diamond® 3.8					
	Synthesis	Synopsys® Synplify Pro® for Lattice I-2013.09L-SP1					
	Simulation	Aldec® Active-HDLTM 9.3 (Windows only, Verilog and VHDL)					
		Mentor Graphics® ModelSim® SE 10.2C (Verilog Only)					

Table 1.2 provides quick facts about the Lattice PCI Express 5G x1/x2 IP Core.

Table 1.2. PCI Express 5G IP Core Quick Facts

		PCI Express 5G IP Configuration	
		Native x2	**Downgraded x1**
IP Requirements	FPGA Families Supported	**Lattice ECP5-5G**	
	Minimal Device Needed	LFE5UM5G-25F-8MG285C	LFE5UM5G-25F-8MG285C
Resource Utilization	Targeted Device	LFE5UM5G-85F-8BG756C	LFE5UM5G-85F-8BG756C
	Data Path Width	64	64
	LUTs	15673	13893
	sysMEM™ EBRs	7	7
	Registers	11249	9660
Design Tool Support	Lattice Implementation	Lattice Diamond® 3.9	
	Synthesis	Synopsys® Synplify Pro® for Lattice L-2016.09L-1	
	Simulation	Aldec® Active-HDL 10.3 (Windows only, Verilog and VHDL)	
		Mentor Graphics® ModelSim® SE 10.2C (Verilog Only)	

1.2. Features

The Lattice PCI Express IP core supports the following features.

1.2.1. PHY Layer

- 2.5 Gb/s or 5.0 Gb/s CML electrical interface
- PCI Express 2.0 electrical compliance
- Serialization and de-serialization
- 8b10b symbol encoding/decoding
- Data scrambling and de-scrambling
- Link state machine for symbol alignment
- Clock tolerance compensation supports +/- 300 ppm
- Framing and application of symbols to lanes
- Lane-to-lane de-skew
- Link Training and Status State Machine (LTSSM)
  - Electrical idle generation
  - Receiver detection
  - TS1/TS2 generation/detection
  - Lane polarity inversion
  - Link width negotiation
  - Higher layer control to jump to defined states

1.2.2. Data Link Layer

- Data link control and management state machine
- Flow control initialization
- Ack/Nak DLLP generation/termination
- Power management DLLP generation/termination through simple user interface
- LCRC generation/checking
- Sequence number generation/checking
- Retry buffer and management

1.2.3. Transaction Layer

- Supports all types of TLPs (memory, I/O, configuration and message)
- Power management user interface to easily send and receive power messages
- Optional ECRC generation/checking
- 128, 256, 512, 1 k, 2 k, or 4 Kbyte maximum payload size

1.2.4. Configuration Space Support

- PCI-compatible Type 0 Configuration Space Registers contained inside the core (0x0-0x3C)
- PCI Express Capability Structure Registers contained inside the core
- Power Management Capability Structure Registers contained inside the core
- MSI Capability Structure Registers contained inside the core
- Device Serial Number Capability Structure contained inside the core
- Advanced Error Reporting Capability Structure contained inside the core

1.2.5. Top Level IP Support

- 125 MHz user interface
  For 2.5G IP core:
  - Native x4 and Downgraded x1/x2 support a 64-bit datapath
  - Native x1 supports a 16-bit datapath

  For 5G IP core:
  - Native x2 and Downgraded x1 support a 64-bit datapath
- In transmit, user creates TLPs without ECRC, LCRC, or sequence number
- In receive, user receives valid TLPs without ECRC, LCRC, or sequence number
- Credit interface for transmit and receive for PH, PD, NPH, NPD, CPLH, CPLD credit types
- Upstream/downstream, single function endpoint topology
- Higher layer control of LTSSM via ports
- Access to select configuration space information via ports

2. Functional Descriptions

This chapter provides a functional description of the Lattice PCI Express Endpoint IP core.

2.1. Overview

The PCI Express core is implemented in several different FPGA technologies. These technologies include soft FPGA fabric elements such as LUTs, registers, embedded block RAMs (EBRs), embedded hard elements with the PCS/SERDES.

The Clarity Designer design tool is used to customize and create a complete IP module for the user to instantiate in a design. Inside the module created by the Clarity Designer tool are several blocks implemented in heterogeneous technologies. All of the connectivity is provided, allowing the user to interact at the top level of the IP core.

Figure 2.1 provides a high-level block diagram to illustrate the main functional blocks and the technology used to implement PCI Express functions.

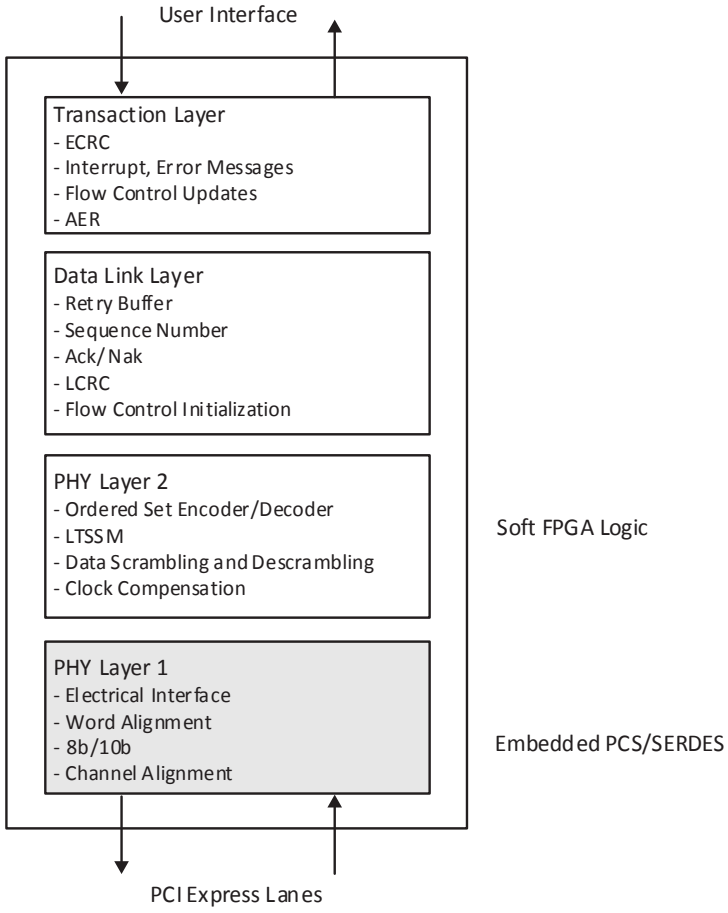

Figure 2.1. PCI Express IP Core Technology and Functions

As the PCI Express core proceeds through the Diamond software design flow specific technologies are targeted to their specific locations on the device. Figure 2.2 provides implementation representations of the LFE5UM devices with a PCI Express core.

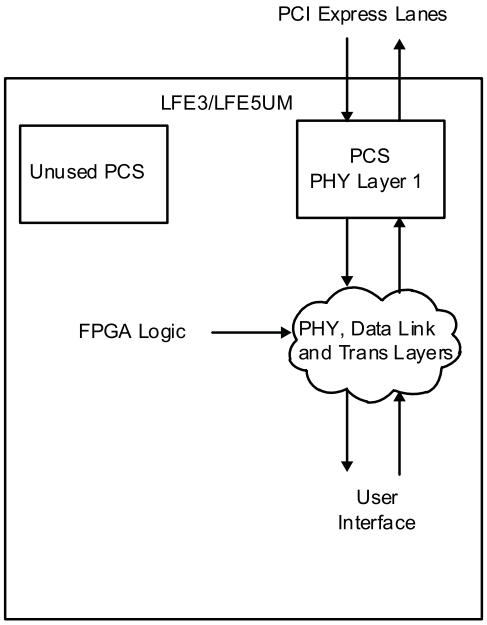

Figure 2.2. PCI Express Core Implementation in LatticeECP3, ECP5 and EPC5-5G

As shown, the data flow moves in and out of the heterogeneous FPGA technology. The user is responsible for selecting the location of the hard blocks (this topic will be discussed later in this document). The FPGA logic placement and routing is the job of the Diamond design tools to select regions nearby the hard blocks to achieve the timing goals.

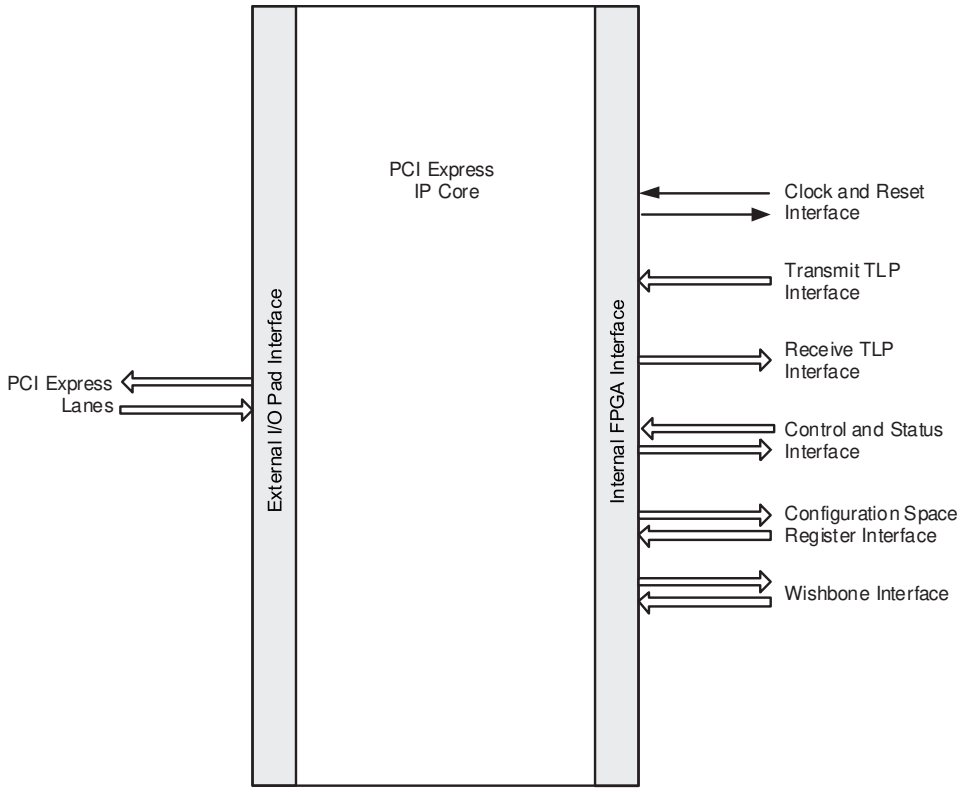

Figure 2.3. PCI Express Interfaces

Table 2.1 provides the list of ports and descriptions for the PCI Express IP core.

Table 2.1. PCI Express IP Core Port List

Port Name	Direction	Clock	Function Description
Clock and Reset Interface			
refclk[p,n]	Input	—	For 2.5G IP core: 100 MHz PCI Express differential reference clock used to generate the 2.5 Gb/s data. For 5G IP core: 200 MHz PCI Express differential reference clock used to generate 5.0 Gb/s data.
sys_clk_125	Output	—	125 MHz clock derived from refclk to be used in the user application.
rst_n	Input	—	Active-low asynchronous data path and state machine reset.
PCI Express Lanes			
hdin[p,n]_[0,1,2,3]	Input	—	PCI Express 2.5 or 5.0 Gb/s CML inputs for lanes 0, 1, 2, and 3. For 5G IP core, up to lanes 0 and 1 only. hdin[p,n]_0 - PCI Express Lane 0 hdin[p,n]_1 - PCI Express Lane 1 hdin[p,n]_2 - PCI Express Lane 2 hdin[p,n]_3 - PCI Express Lane 3
hdout[p,n]_[0,1,2,3]	Output	—	PCI Express 2.5 or 5.0 Gb/s CML inputs for lanes 0, 1, 2, and 3. For 5G IP core, up to lanes 0 and 1 only. hdout[p,n]_0 - PCI Express Lane 0 hdout[p,n]_1 - PCI Express Lane 1 hdout[p,n]_2 - PCI Express Lane 2 hdout[p,n]_3 - PCI Express Lane 3
Transmit TLP Interface			
tx_data_vc0[n:0]	Input	sys_clk_125	Transmit data bus. For 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core: [63:56] Byte N [55:48] Byte N+1 [47:40] Byte N+2 [39:32] Byte N+3 [31:24] Byte N+4 [23:16] Byte N+5 [15: 8] Byte N+6 [7: 0] Byte N+7 For 2.5G IP core Native x1: [15:8] Byte N [7:0] Byte N+1
tx_req_vc0	Input	sys_clk_125	Active high transmit request. This port is asserted when the user wants to send a TLP. If several TLPs will be provided in a burst, this port can remain high until all TLPs have been sent.
tx_rdy_vc0	Output	sys_clk_125	Active high transmit ready indicator. Tx_st should be provided next clock cycle after tx_rdy is high. This port will go low between TLPs.

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
tx_st_vc0	Input	sys_clk_125	Active high transmit start of TLP indicator.
tx_end_vc0	Input	sys_clk_125	Active high transmit end of TLP indicator. This signal must go low at the end of the TLP.
tx_nlfy_vc0	Input	sys_clk_125	Active high transmit nullify TLP. Can occur anywhere during the TLP. If tx_nlfy_vc0 is asserted to nullify a TLP the tx_end_vc0 port should not be asserted. The tx_nlfy_vc0 terminates the TLP.
tx_dwen_vc0	Input	sys_clk_125	Active high transmit 32-bit word indicator. Used if only bits [63:32] provide valid data. This port is only available for 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core.
tx_val	Output	sys_clk_125	Active high transmit clock enable. When a Native x4 or x2 is downgraded, this signal is used as the clock enable to downshift the transmit bandwidth. This port is only available for 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core.
tx_ca_[ph,nph,cplh]_vc0[8:0]	Output	sys_clk_125	Transmit Interface header credit available bus. This port will decrement as TLPs are sent and increment as UpdateFCs are received. Ph - Posted header Nph - Non-posted header Cplh - Completion header This credit interface is only updated when an UpdateFC DLLP is received from the PCI Express line. [8] - This bit indicates the receiver has infinite credits. If this bit is high then bits [7:0] should be ignored. [7:0] – The amount of credits available at the receiver.
tx_ca_[pd,npd,cpld]_vc0[12:0]	Output	sys_clk_125	Transmit Interface data credit available bus. This port will decrement as TLPs are sent and increment as UpdateFCs are received. pd - posted data npd - non-posted data cpld - completion data [12] - This bit indicates the receiver has infinite credits. If this bit is high, then bits [11:0] should be ignored. [11:0] - The amount of credits available at the receiver.
tx_ca_p_recheck_vc0	Output	sys_clk_125	Active high signal that indicates the core sent a Posted TLP which changed the tx_ca_p[h,d]_vc0 port. This might require a recheck of the credits available if the user has asserted tx_req_vc0 and is waiting for tx_rdy_vc0 to send a Posted TLP.
tx_ca_cpl_recheck_vc0	Output	sys_clk_125	Active high signal that indicates the core sent a Completion TLP which changed the tx_ca_cpl[h,d]_vc0 port. This might require a recheck of the credits available if the user has asserted tx_req_vc0 and is waiting for tx_rdy_vc0 to send a Completion TLP.

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
Receive TLP Interface			
rx_data_vc0[n:0]	Output	sys_clk_125	Receive data bus. For 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core: [63:56] Byte N [55:48] Byte N+1 [47:40] Byte N+2 [39:32] Byte N+3 [31:24] Byte N+4 [23:16] Byte N+5 [15: 8] Byte N+6 [7: 0] Byte N+7 For 2.5G IP core Native x1: [15:8] Byte N [7:0] Byte N+1
rx_st_vc0	Output	sys_clk_125	Active high receive start of TLP indicator.
rx_end_vc0	Output	sys_clk_125	Active high receive end of TLP indicator.
rx_dwen_vc0	Output	sys_clk_125	Active high 32-bit word indicator. Used if only bits [63:32] contain valid data. This port is only available for 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core.
rx_ecrc_err_vc0	Output	sys_clk_125	Active high ECRC error indicator. Indicates an ECRC error in the current TLP. Only available if ECRC is enabled in the IP configuration GUI.
rx_us_req_vc0	Output	sys_clk_125	Active high unsupported request indicator. Asserted if any of the following TLP types are received: — Memory Read Request-Locked — The TLP is still passed to the user where the user will need to terminate the TLP with an Unsupported Request Completion.
rx_malf_tlp_vc0	Output	sys_clk_125	Active high malformed TLP indicator. Indicates a problem with the current TLPs length or format.
rx_bar_hit[6:0]	Output	sys_clk_125	Active high BAR indicator for the current TLP. If this bit is high, the current TLP on the receive interface is in the address range of the defined BAR. [6] - Expansion ROM [5] - BAR5 [4] - BAR4 [3] - BAR3 [2] - BAR2 [1] - BAR1 [0] - BAR0 For 64-bit BARs, a BAR hit will be indicated on the lower BAR number. The rx_bar_hit changes along with the rx_st_vc0 signal.
ur_np_ext	Input	sys_clk_125	Active high indicator for unsupported non-posted request reception.
ur_p_ext	Input	sys_clk_125	Active high indicator for unsupported posted request reception.

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
[ph,pd, nph,npd] _buf_status_vc0	Input	sys_clk_125	Active high user buffer full status indicator. When asserted, an UpdateFC will be sent for the type specified as soon as possible without waiting for the UpdateFC timer to expire.
[ph,nph]_processed_vc0	Input	sys_clk_125	Active high indicator to inform the IP core of how many credits have been processed. Each clock cycle high counts as one credit processed. The core will generate the required UpdateFC DLLP when either the UpdateFC timer expires or enough credits have been processed.
[pd,npd]_processed_vc0	Input	sys_clk_125	Active high enable for [pd, npd]_num_vc0 port. The user should place the number of data credits processed on the [pd, npd]_num_vc0 port and then assert [pd, npd]_processed_vc0 for one clock cycle. The core will generate the required UpdateFC DLLP when either the UpdateFC timer expires or enough credits have been processed.
[pd,npd]_num_vc0[7:0]	Input	sys_clk_125	This port provides the number of PD or NPD credits processed. It is enabled by the [pd, npd]_processed_vc0 port.
Control and Status			
PHYSICAL LAYER			
no_pcie_train	Input	Async	Active high signal disables LTSSM training and forces the LTSSM to L0. This is intended to be used in simulation only to force the LTSSM into the L0 state.
force_lsm_active	Input	Async	Forces the Link State Machine for all of the channels to the linked state.
force_rec_ei	Input	Async	Forces the detection of a received electrical idle.
force_phy_status	Input	Async	Forces the detection of a receiver during the LTSSM Detect state on all of the channels.
force_disable_scr	Input	Async	Disables the PCI Express TLP scrambler.
hl_snd_beacon	Input	sys_clk_125	Active high request to send a beacon.
hl_disable_scr	Input	Async	Active high to set the disable scrambling bit in the TS1/TS2 sequence.
hl_gto_dis	Input	Async	Active high request to go to Disable state when LTSSM is in Config or Recovery.
hl_gto_det	Input	sys_clk_125	Active high request to go to Detect state when LTSSM is in L2 or Disable.
hl_gto_hrst	Input	sync	Active high request to go to Hot Reset when LTSSM is in Recovery.
hl_gto_l0stx	Input	sys_clk_125	Active high request to go to L0s when LTSSM is in L0.
hl_gto_l0stxfts	Input	sys_clk_125	Active high request to go to L0s and transmit FTS when LTSSM is in L0s.
hl_gto_l1	Input	sys_clk_125	Active high request to go to L1 when LTSSM is in L0.
hl_gto_l2	Input	sys_clk_125	Active high request to go to L2 when LTSSM is in L0.
hl_gto_lbk[3:0]	Input	sys_clk_125	Active high request to go to Loopback when LTSSM is in Config or Recovery.
hl_gto_rcvry	Input	sys_clk_125	Active high request to go to Recovery when LTSSM is in L0, L0s or L1.
hl_gto_cfg	Input	sys_clk_125	Active high request to go to Config when LTSSM is in Recovery.

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
phy_ltssm_state[3:0]	Output	sys_clk_125	PHY Layer LTSSM current state 0000 - Detect 0001 - Polling 0010 - Config 0011 - L0 0100 - L0s 0101 - L1 0110 - L2 0111 - Recovery 1000 - Loopback 1001 - Hot Reset 1010 - Disabled
phy_cfgln[n:0]	Output	sys_clk_125	Active high LTSSM Config state link status. An active bit indicates the channel is included in the configuration link width negotiation. [3:0] - 2.5G IP core Native x4, Downgraded x1/x2 [1:0] - 5G IP core Native x2, Downgraded x1 [0] - PCI Express Lane 3 [1] - PCI Express Lane 2 [2] - PCI Express Lane 1 [3] - PCI Express Lane 0
phy_cfgln_sum[2:0]	Output	sys_clk_125	Link Width. This port is only available for 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core. 000 - No link defined 001 - Link width = 1 010 - Link width = 2 100 - Link width = 4
phy_pol_compliance	Output	sys_clk_125	Active high indicator that the LTSSM is in the Polling. Compliance state.
tx_lbk_rdy	Output	sys_clk_250	This output port is used to enable the transmit master loop-back data. This port is only available if the Master Loop-back feature is enabled in the IP configuration GUI.
tx_lbk_kcntl[7/1:0]	Input	sys_clk_250	This input port is used to indicate a K control word is being sent on tx_lbk_data port. This port is only available if the Master Loopback feature is enabled in the IP configuration GUI. For 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core: [7:6]- K control on tx_lbk_data[63:48] [5:4] - K control on tx_lbk_data[47:32] [3:2] - K control on tx_lbk_data[31:16] [1:0] - K control on tx_lbk_data[15:0] For 2.5G IP core Native x1: [1:0] - K control on rx_lbk_data[15:0]

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
tx_lbk_data[63/15:0]	Input	sys_clk_250	This input port is used to send 64-bit data for the master loopback. This port is only available if the Master Loopback feature is enabled in the IP configuration GUI. For 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core: [63:48] - Lane 3 data [47:32] - Lane 2 data [31:16] - Lane 1 data [15:0] - Lane 0 data For 2.5G IP core Native x1: [15:0] - Lane 0 data
rx_lbk_kcntl[7/1:0]	Output	sys_clk_250	This output port is used to indicate a K control word is being received on rx_lbk_data port. This port is only avail- able if the Master Loopback feature is enabled in the IP configuration GUI. For 2.5G IP core Native x4, Downgraded x1/x2 or 5G IP core: [7:6] - K control on rx_lbk_data[63:48] [5:4] - K control on rx_lbk_data[47:32] [3:2] - K control on rx_lbk_data[31:16] [1:0] - K control on rx_lbk_data[15:0] For 2.5G IP core Native x1: [1:0] - K control on rx_lbk_data[15:0]
rx_lbk_data[63:0]	Output	sys_clk_250	This output port is used to receive 64/16-bit data for the master loopback. This port is only available if the Master Loopback feature is enabled in the IP configuration GUI. For 2.5G IP core Native x4, Downgraded x1/x2 and 5G IP core: [63:48] - Lane 3 data [47:32] - Lane 2 data [31:16] - Lane 1 data [15:0] - Lane 0 data For 2.5G IP core Native x1: [15:0]- Lane 0 data
DATA LINK LAYER			
dl_inactive	Output	sys_clk_125	Data Link Layer is the DL_Inactive state.
dl_init	Output	sys_clk_125	Data Link Layer is in the DL_Init state.
dl_active	Output	sys_clk_125	Data Link Layer is in the DL_Active state.
dl_up	Output	sys_clk_125	Data Link Layer is in the DL_Active state and is now providing TLPs to the Transaction Layer.
tx_dllp_val	Input	sys_clk_125	Active high power message send command 00 - Nothing to send 01 - Send DLLP using tx_pmtype DLLP 10 - Send DLLP using tx_vsd_data Vendor Defined DLLP 11 - Not used

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
tx_pmtype[2:0]	Input	sys_clk_125	Transmit power message type 000 - PM Enter L1 001 - PM Enter L2 011 - PM Active State Request L1 100 - PM Request Ack
tx_vsd_data[23:0]	Input	sys_clk_125	Vendor-defined data to send in DLLP
tx_dllp_sent	Output	sys_clk_125	Requested DLLP was sent.
rxdp_pmd_type[2:0]	Output	sys_clk_125	Receive power message type 000 - PM Enter L1 001 - PM Enter L2 011 - PM Active State Request L1 100 - PM Request Ack
rxdp_vsd_data[23:0]	Output	sys_clk_125	Vendor-defined DLLP data received
rxdp_dllp_val	Output	sys_clk_125	Active high power message received
tx_rbuf_empty	Output	sys_clk_125	Transmit retry buffer is empty. (Used for ASPM implementation outside the core.)
tx_dllp_pend	Output	sys_clk_125	A DLLP is pending to be transmitted. (Used for ASPM implementation outside the core.)
rx_tlp_rcvd	Output	sys_clk_125	A TLP was received. (Used for ASPM implementation outside the core.)
TRANSACTION LAYER			
ecrc_gen_enb	Output	sys_clk_125	If AER and ECRC are enabled then this port is an output and indicates when ECRC generation is enabled by the PCI Express IP core. If ECRC generation is turned on then the TD bit in the transmit TLP header must be set to provide room in the TLP for the insertion of the ECRC.
ecrc_chk_enb	Output	sys_clk_125	If AER and ECRC are enabled then this port is an output and indicates when ECRC checking is enabled by the PCI Express IP core.
cmpln_tout	Input	sys_clk_125	Completion Timeout Indicator for posted request. Used to force non-fatal error message generation and also set appropriate bit in AER.
cmpltr_abort_np	Input	sys_clk_125	Complete or Abort Indicator for non-posed request. Used to force non-fatal error message generation and also set appropriate bit in AER.
cmpltr_abort_p	Input	sys_clk_125	Complete or Abort Indicator. Used to force non-fatal error message generation and also set appropriate bit in AER.
unexp_cmpln	Input	sys_clk_125	Unexpected Completion Indicator. Used to force non-fatal error message generation and also set appropriate bit in AER.
np_req_pend	Input	sys_clk_125	Sets device Status[5] indicating that a Non-Posted transaction is pending.
err_tlp_header[127:0]	Input	sys_clk_125	Advanced Error Reporting errored TLP header. This port is used to provide the TLP header for the TLP associated with an unexp_cmpln or cmpltr_abort_np/cmpltr_abort_p. The header data should be provided on the same clock cycle as the unexp_cmpln or cmpltr_abort_np/cmpltr_abort_p.

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
CONFIGURATION REGISTERS			
bus_num[7:0]	Output	sys_clk_125	Bus Number supplied with configuration write.
dev_num[4:0]	Output	sys_clk_125	Device Number supplied with configuration write.
func_num[2:0]	Output	sys_clk_125	Function Number supplied with configuration write.
cmd_reg_out[5:0]	Output	sys_clk_125	PCI Type0 Command Register bits [5] - Interrupt Disable [4] - SERR# Enable [3] - Parity Error Response [2] - Bus Master [1] - Memory Space [0] - IO Space
dev_cntl_out[14:0]	Output	sys_clk_125	PCI Express Capabilities Device Control Register bits [14:0].
lnk_cntl_out[7:0]	Output	sys_clk_125	PCI Express Capabilities Link Control Register bits [7:0].
inta_n	Input	sys_clk_125	Legacy INTx interrupt request. Falling edge will produce an ASSERT_INTx message and set the Interrupt Status bit to a 1. Rising edge will produce a DEASSERT_INTx message and clear the Interrupt Status bit. The Interrupt Disable bit will disable the message to be sent, but the status bit will operate as normal. The inta_n port has a requirement for how close an assert or de-assert event can be to the previous assert or de-assert event. For the 2.5G IP core native x4 and x2/x1 downgraded cores, this is two sys_clk_125 clock cycles. For the native x1 core this is eight sys_clk_125 clock cycles. If the inta_n port is low indicating an ASSERT_INTx and the Interrupt Disable bit is driven low by the system, then the inta_n port needs to be pulled high to send a DEASSERT_INTx message. This can be automatically performed by using a logic OR between the inta_n and cmd_reg_out[5] port.
msi[7:0]	Input	sys_clk_125	MSI interrupt request. Rising edge on a bit will produce a MemWr TLP for a MSI interrupt for the provided address and data by the root complex. [7] - MSI 8 [6] - MSI 7 [5] - MSI 6 [4] - MSI 5 [3] - MSI 4 [2] - MSI 3 [1] - MSI 2 [0] - MSI 1
flr_rdy_in	Input	sys_clk_125	Ready from user logic to perform Functional Level Reset
initiate_flr	Output	sys_clk_125	Initiate Functional Level Reset for user logic
dev_cntl_2_out	Output	sys_clk_125	PCI Express Capabilities Device Control 2 Register Bits [4:0]
mm_enable[2:0]	Output	sys_clk_125	Multiple MSI interrupts are supported by the root complex. This indicates how many messages the root complex will accept.

Table 2.1. PCI Express IP Core Port List *(continued)*

Port Name	Direction	Clock	Function Description
msi_enable	Output	sys_clk_125	MSI interrupts are enabled by the root complex. When this port is high MSI interrupts are to be used. The inta_n port is disabled.
pme_status	Input	sys_clk_125	Active high input to the Power Management Capability Structure PME_Status bit. Indicates that a Power Management Event has occurred on the endpoint.
pme_en	Output	sys_clk_125	PME_En bit in the Power Management Capability Structure. Active high signal to allow the endpoint to send PME messages.
pm_power_state[1:0]	Output	sys_clk_125	Power State in the Power Management Capability Structure. Software sets this state to place the endpoint in a particular state. 00 - D0 01 - D1 10 - D2 11 - D3
load_id	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. When this port is low, the core will send Configuration Request Retry Status for all Configuration Requests. When this port is high, the core will send normal Successful Completions for Configuration Requests. On the rising edge of load_id the vectors on vendor_id[15:0], device_id[15:0], rev_id[7:0], class_code[23:0], subsys_ven_id[15:0], and subsys_id[15:0] will be loaded into the proper configuration registers.
vendor_id[15:0]	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. This port will load the vendor ID for the core on the rising edge of load_id.
device_id[15:0]	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. This port will load the device ID for the core on the rising edge of load_id.
rev_id[7:0]	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. This port will load the revision ID for the core on the rising edge of load_id.
class_code[23:0]	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. This port will load the class code for the core on the rising edge of load_id.
subsys_ven_id[15:0]	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. This port will load the subsystem vendor ID for the core on the rising edge of load_id.
subsys_id[15:0]	Input	sys_clk_125	This port is only present when the “Load IDs from Ports” checkbox is enabled in the IP configuration GUI. This port will load the subsystem device ID for the core on the rising edge of load_id.

Table 2.1. PCI Express IP Core Port List *(continued)*

Wishbone Interface*			
CLK_I	Input	—	Wishbone interface clock.
RST_I	Input	CLK_I	Asynchronous reset.
SEL_I [3:0]	Input	CLK_I	Data valid indicator [3] - DAT_I[31:24] [2] - DAT_I[23:16] [1] - DAT_I[15:8] [0] - DAT_i[7:0]
WE_I	Input	CLK_I	Write enable 1 - write 0 - read
STB_I	Input	CLK_I	Strobe input.
CYC_I	Input	CLK_I	Cycle input.
DAT_I[31:0]	Input	CLK_I	Data input.
ADR_I[12:0]	Input	CLK_I	Address input.
CHAIN_RDAT_in[31:0]	Input	CLK_I	Daisy chain read data. If using a read chain for the wishbone interface, this would be the read data from the previous slave. If not using a chain, then this port should be tied low.
CHAIN_ACK_in	Input	CLK_I	Daisy chain ack. If using a read chain for the wishbone interface, this would be the ack from the previous slave. If not using a chain, then this port should be tied low.
ACK_O	Output	CLK_I	Ack output.
IRQ_O	Output	CLK_I	Interrupt output. This port is not used (always 0).
DAT_O[31:0]	Output	CLK_I	Data output.

***Note**: Complete information on the Wishbone interface specification can be found at www.opencores.org in the WISHBONE System-on-Chip (SOC) Interconnection Architecture for Portable IP Cores specification.

2.2. Interface Description

This section describes the datapath user interfaces of the IP core. The transmit and receive interfaces both use the TLP as the data structure. The lower layers attach the start, end, sequence number and crc.

2.2.1. Transmit TLP Interface

In the transmit direction, the user must first check the credits available on the far end before sending the TLP. This information is found on the tx_ca_[ph,pd,nph,npd]_vc0 bus. There must be enough credits available for the entire TLP to be sent.

The user must then check that the core is ready to send the TLP. This is done by asserting the tx_req_vc0 port and waiting for the assertion of tx_rdy_vc0. While waiting for tx_rdy_vc0, if tx_ca_p/cpl_recheck is asserted, then the user must check available credit again. If there is enough credit, the user can proceed with the sending data based on tx_rdy_vc0. If the credit becomes insufficient, tx_req_vc0 must be deasserted on the next clock until enough credit is available. When tx_rdy_vc0 is asserted the next clock cycle will provide the first 64-bit word of the TLP and assert tx_st_vc0.

Tx_rdy_vc0 will remain high until one clock cycle before the last clock cycle of TLP data (based on the length field of the TLP). This allows the tx_rdy_vc0 to be used as the read enable of a non-pipelined FIFO.

2.2.1.1. Transmit TLP Interface Waveforms for 2.5G IP Core Native x4, Downgraded x1/x2 and 5G IP Core Native x2, Downgraded x1

Figure 2.4 through Figure 2.12 provide timing diagrams for the tx interface signals with a 64-bit datapath.

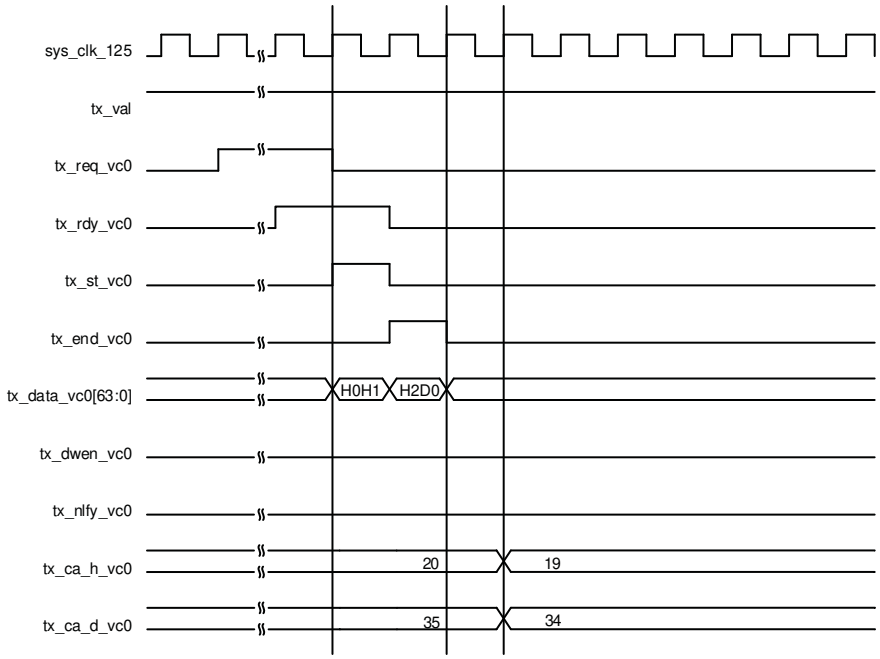

Figure 2.4. Transmit Interface of 2.5G IP core Native x4 or 5G IP core Native x2, 3DW Header, 1 DW Data

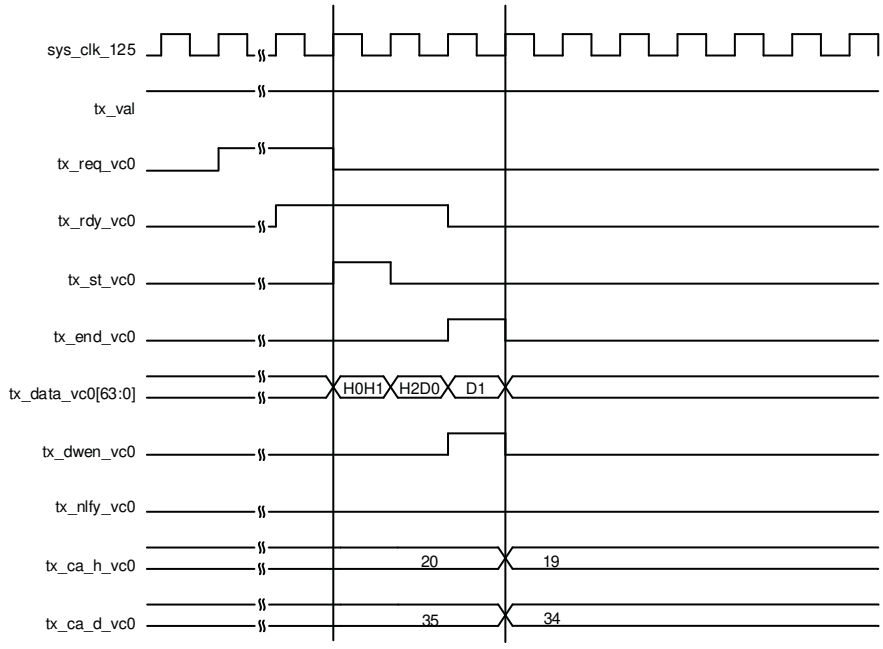

Figure 2.5. Transmit Interface 2.5G IP core Native x4 or 5G IP core Native x2, 3DW Header, 2 DW Data

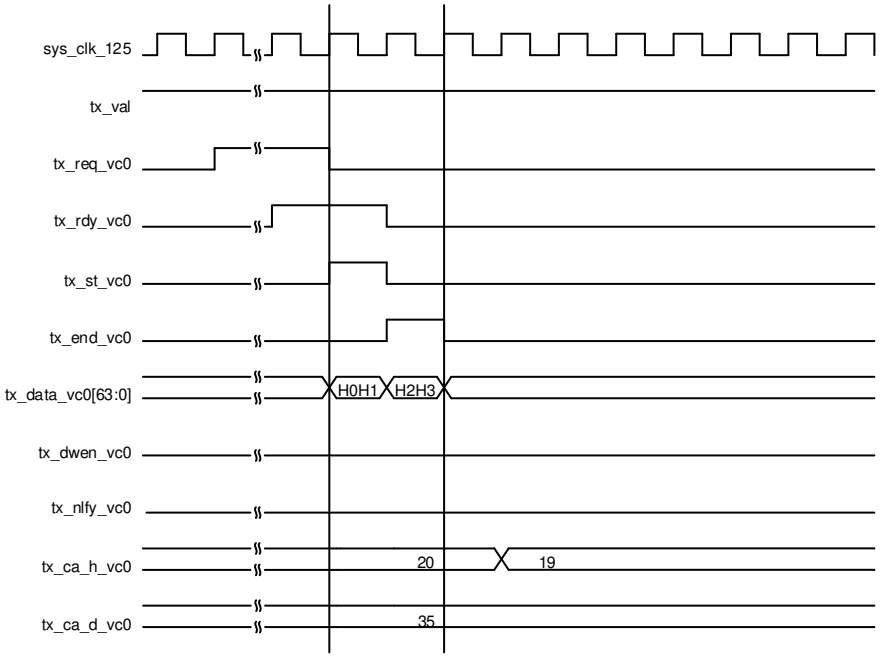

Figure 2.6. Transmit Interface 2.5G IP core Native x4 or 5G IP core Native x2, 4DW Header, 0 DW

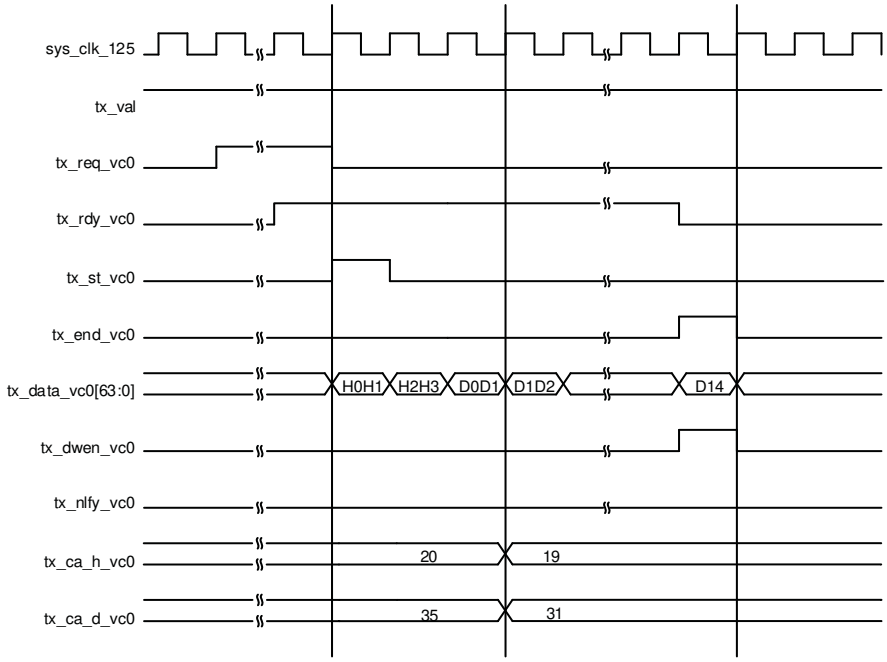

Figure 2.7. Transmit Interface 2.5G IP core Native x4 or 5G IP core Native x2, 4DW Header, Odd Number of DWs

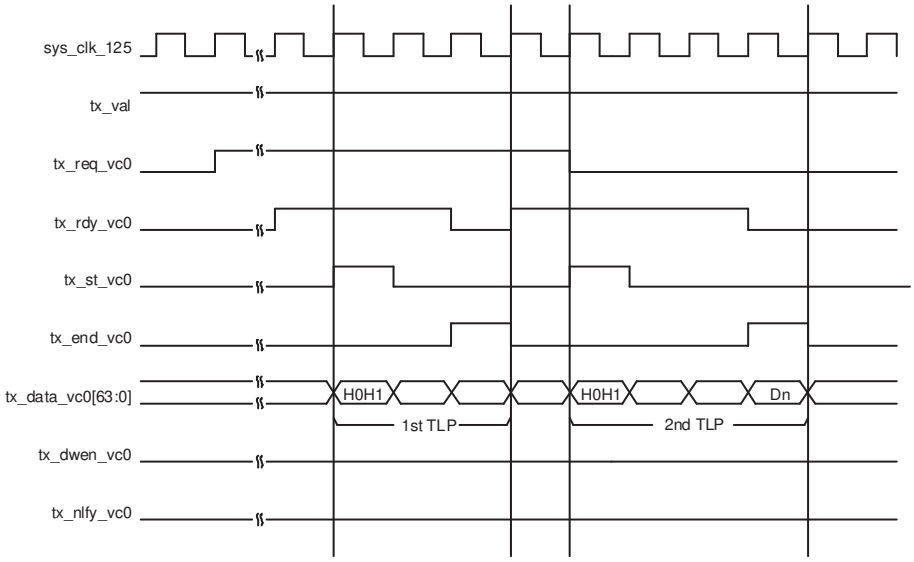

Figure 2.8. Transmit Interface 2.5G IP core Native x4 or 5G IP core Native x2, Burst of Two TLPs

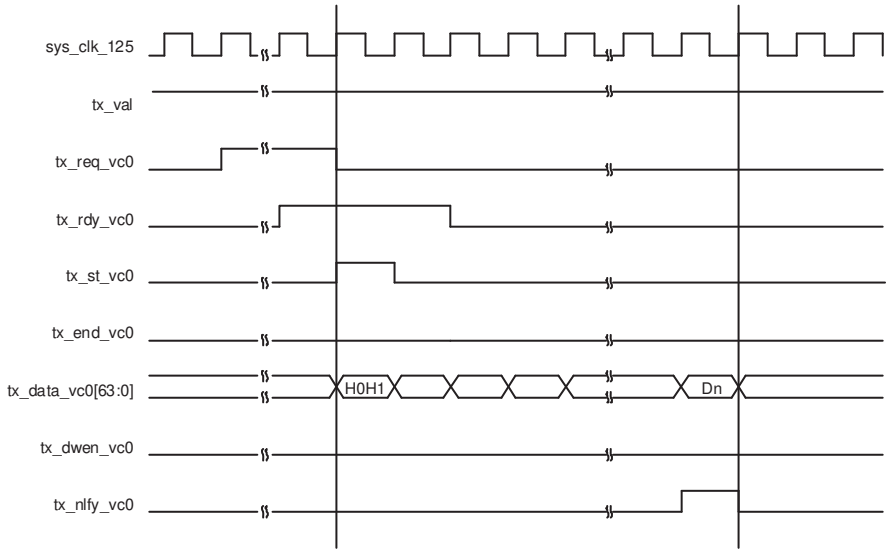

Figure 2.9. Transmit Interface 2.5 IP core Native x4 or 5G IP core Native x2, Nullified TLP

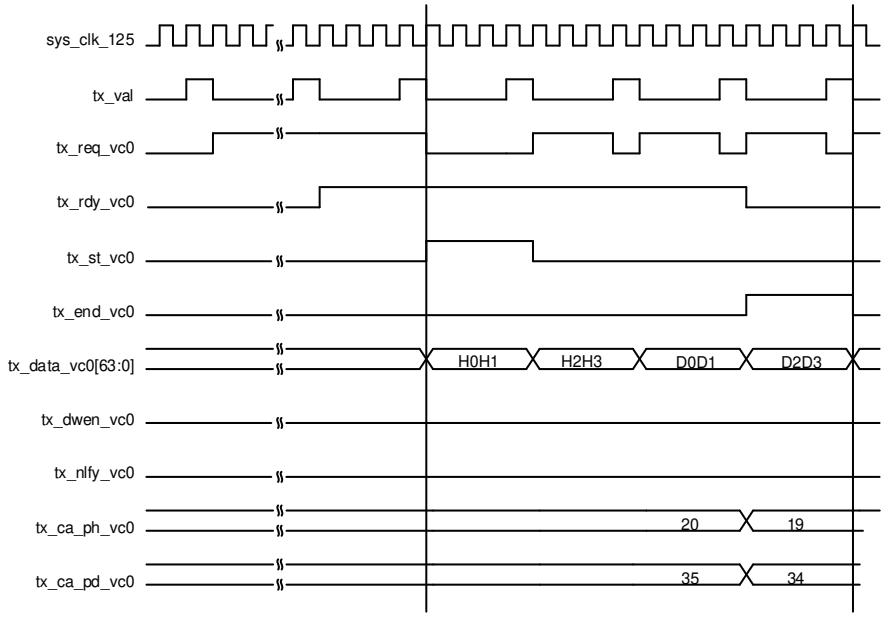

Figure 2.10. Transmit Interface 2.5G IP Core Downgraded x1 or 5G IP core Downgraded x1 at Gen1 Speed

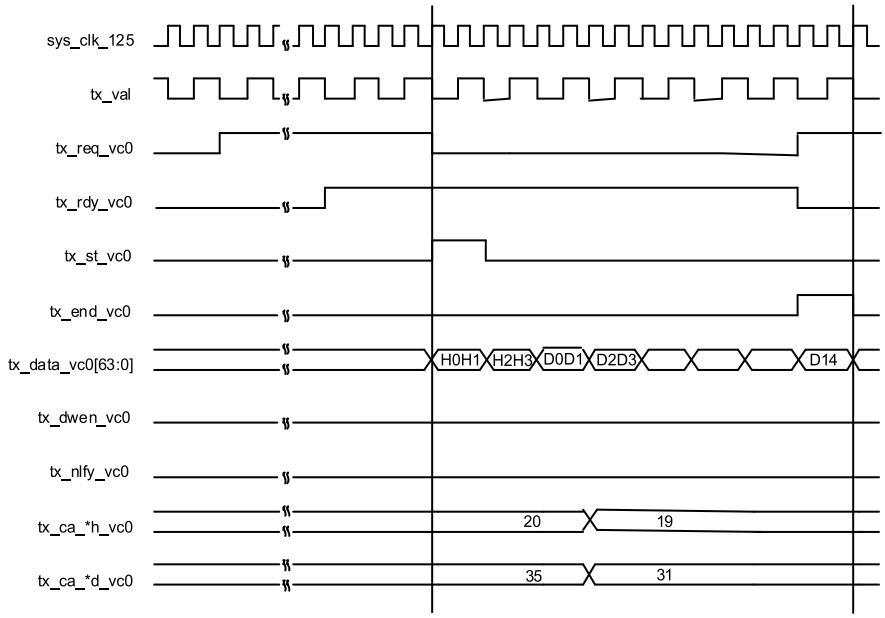

Figure 2.11. Transmit Interface 2.5G IP core Downgraded x2, 5G IP core Native x2 at Gen 1 speed or Downgraded x1 at Gen2 Speed

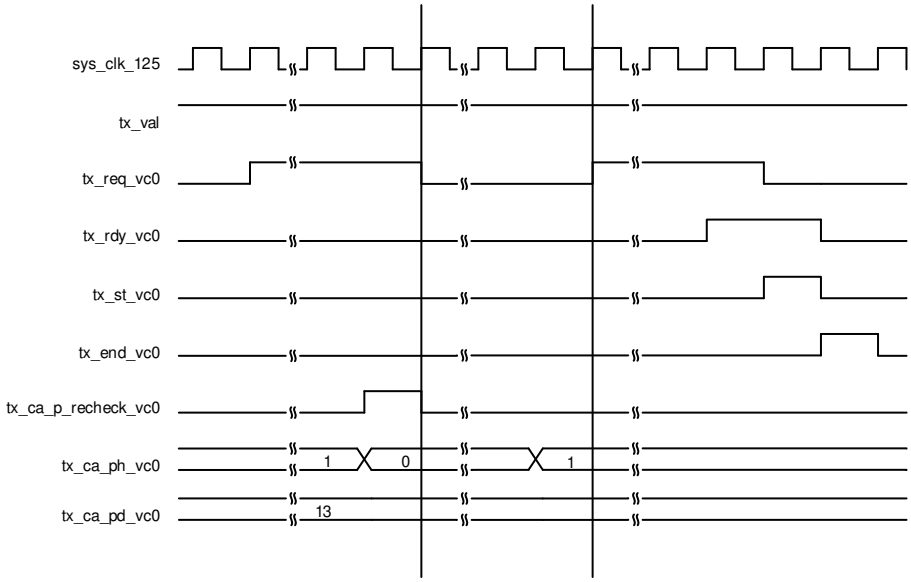

Figure 2.12. Transmit Interface 2.5G IP core Native x4 or 5G IP core Native x2, Posted Request with tx_ca_p-recheck Assertion

2.2.1.2. Transmit TLP Interface Waveforms for 2.5G IP Core Native x1

Figure 2.13 through Figure 2.16 provide timing diagrams for the transmit interface signals with a 16-bit datapath.

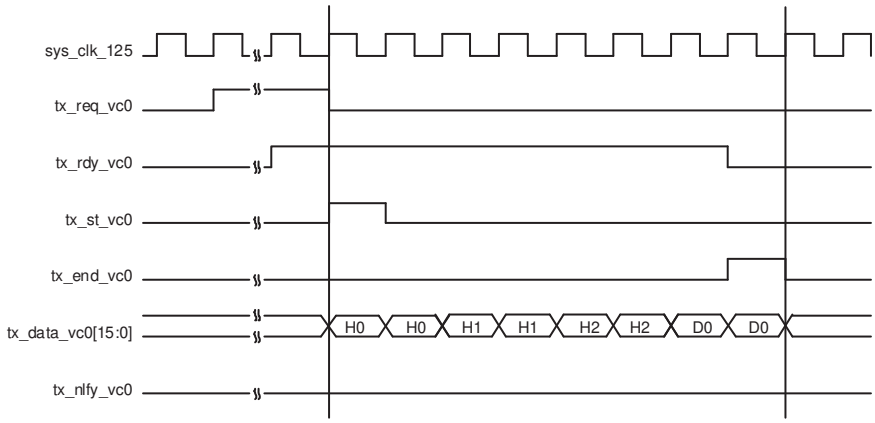

Figure 2.13. Transmit Interface Native x1, 3DW Header, 1 DW Data