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DATA SHEET

PCK2020

CK00 (100/133MHz) spread spectrum differential system clock generator

Product specification
Supersedes data of 2000 Jul 25

2000 Nov 13

Philips
Semiconductors

PHILIPS

CK00 (100/133MHz) spread spectrum differential system clock generator

PCK2020

FEATURES

- 3.3 V operation
- Four differential CPU clock pairs
- Ten PCI clocks at 3.3 V
- Four 66 MHz clocks at 3.3 V
- Two 48 MHz clocks at 3.3 V
- Two 14.318 MHz reference clocks
- 100 or 133 MHz operation
- Power management control pins
- CPU clock skew less than 200 ps cycle-to-cycle
- CPU clock skew less than 150 ps pin-to-pin
- 1.5 ns to 3.5 ns delay on PCI pins
- Spread Spectrum capability

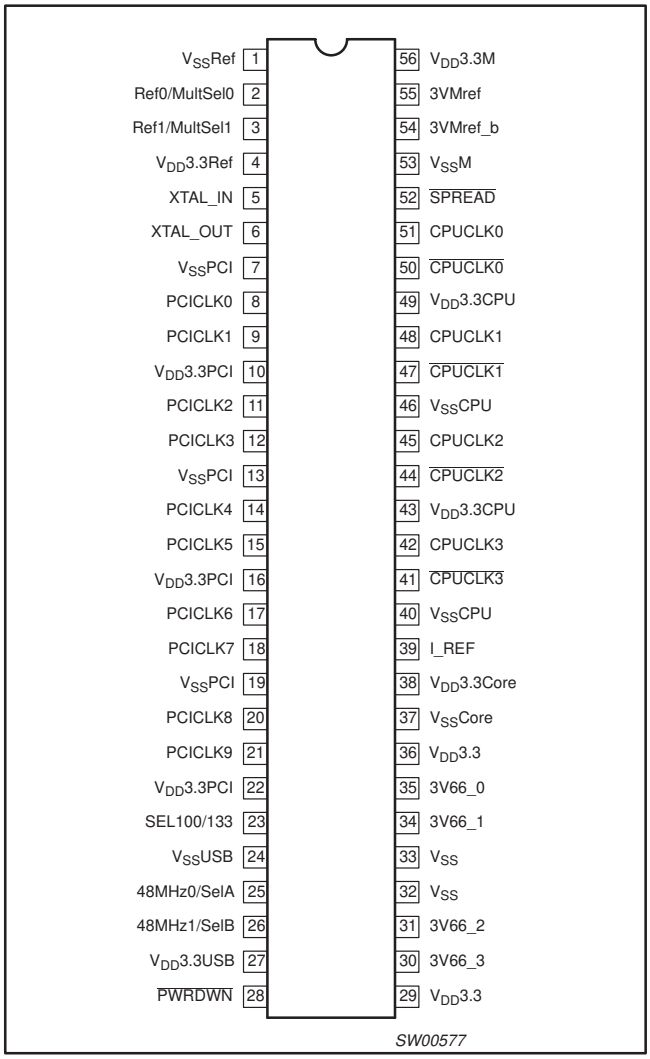
DESCRIPTION

The PCK2020 is a clock synthesizer/driver for a Pentium III and other similar processors.

The PCK2020 has four differential pair CPU current source outputs, two Mref clock outputs running at 1/2 the CPU clock frequency depending on the state of SEL133/100 pin and four 3V66 clocks running at 66 MHz. There are ten PCI clock outputs running at 33 MHz and two 48 MHz clocks. Finally, there are two 3.3 V reference clocks at 14.318 MHz. All clock outputs meet Intel's drive strength, rise/fall times, jitter, accuracy, and skew requirements.

The part possesses a dedicated power-down input pin for power management control. This input is synchronized on-chip and ensures glitch-free output transitions.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE (°C)	ORDER CODE	DRAWING NUMBER
56-Pin Plastic SSOP	0 to +70	PCK2020 DL	SOT371-1

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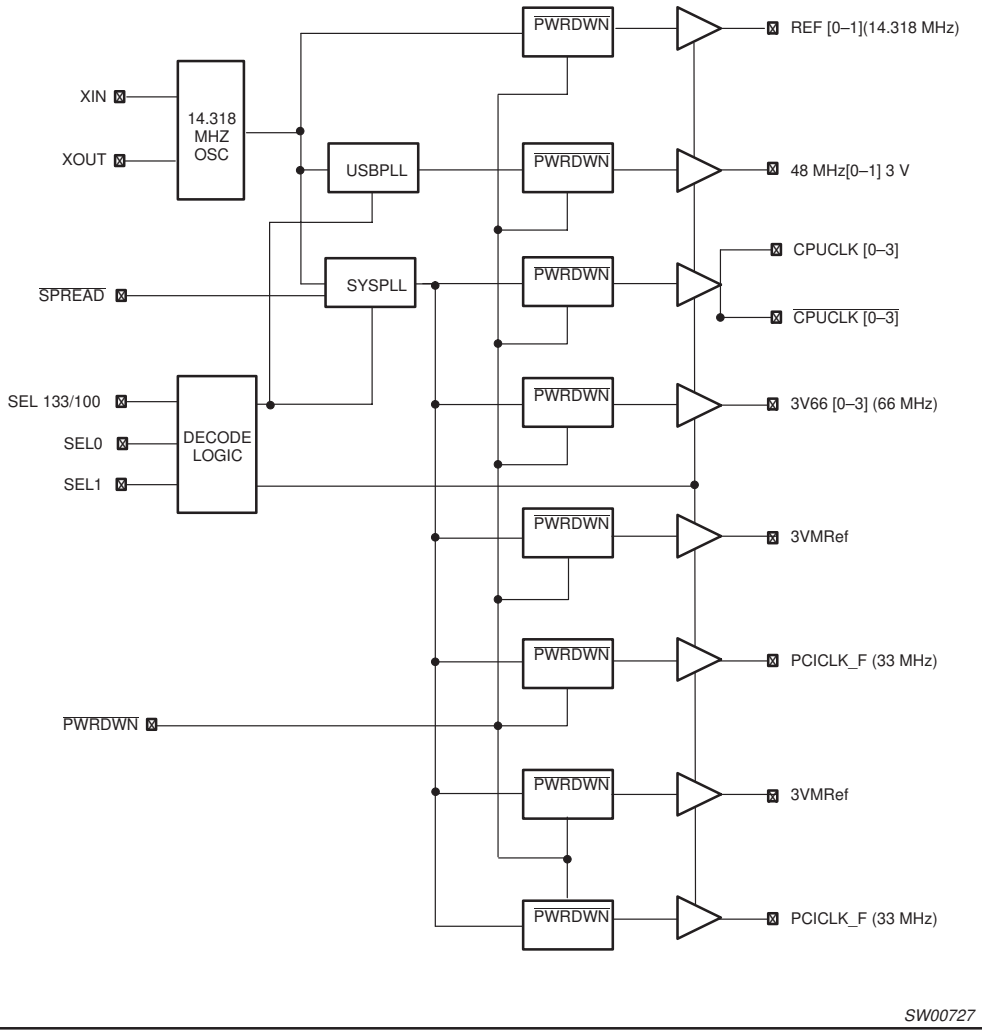
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	V_{SS}Ref	
2, 3	Ref0/MultSel0 Ref1/MultSel1	During power up, pins functions as a latched inputs that enables MULTSEL0 and MULTSEL1 prior to the pins being used for output of 3 V at 14.318 MHz. Part must be clocked to latch data in.
4	V_{DD}3.3Ref	
5	XTAL_IN	Crystal input
6	XTAL_OUT	Crystal output
7, 13, 19	V_{SS}PCI	
8, 9, 11, 12, 14, 15, 17, 18, 20, 21	PCICLK[0–9]	3.3 V PCI clock outputs fixed at 33 MHz.
10, 16, 22	V_{DD}3.3PCI	
23	SEL100/133	Select input pin for enabling 133 MHz or 100 MHz CPU outputs.
24	V_{SS}USB	
25, 26	48 MHz/SelA 48 MHz/SelB	3.3 V fixed 48 MHz clock outputs. During power up, pins functions as latched inputs that enables SELA and SELB prior to the pins being used for output of 3 V at 48 MHz. Part must be clocked to latch data in.
27	V_{DD}3.3USB	
28	$\overline{\text{PWRDWN}}$	Device enters power down mode when held low. Asserts low.
29, 36	V_{DD}3.3	
30, 31, 34, 35	3V66[0–3]	3.3 V fixed 66 MHz CPU clock outputs.
32, 33	V_{SS}	
37	V_{SS}Core	
38	V_{DD}3.3Core	3.3 V power supply for analog circuits.
39	I_REF	This pin controls the reference current for the host pairs. This pin requires a fixed precision resistor tied to ground in order to establish the correct current.
40, 46	V_{SS}CPU	
41, 44, 47, 50	$\overline{\text{CPUCLK}}$[0–3]	
42, 45, 48, 51	CPUCLK[0–3]	
43, 49	V_{DD}3.3CPU	
52	$\overline{\text{SPREAD}}$	Enables spread spectrum mode when held low on differential host outputs, MREF/MREF_B clocks, 66 MHz clocks, and 33 MHz PCI clocks. Asserts low.
53	V_{SS}M	
54	3VMref_b	3.3 V clock outputs running at 1/2 CPU clock frequency. 66 MHz or 50 MHz depending on the state of input pin SEL133/100. (Out of phase with 3VMREF output).
55	3VMref	3.3 V clock outputs running at 1/2 CPU clock frequency. 66 MHz or 50 MHz depending on the state of input pin SEL133/100.
56	V_{DD}3.3M	3.3 V power supply

BLOCK DIAGRAM



FUNCTION TABLES

SEL 100/133	SELA	SELB	HOST	M_{REF}	3V66	3V33 PCI	48 MHz	REF
0	0	0	100 MHz	50 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
0	0	1	105 MHz[1]	52.5 MHz[1]	70 MHz[1]	35 MHz[1]	48 MHz	14.318 MHz
0	1	0	200 MHz	50 MHz	66.7 MHz	33.3 MHz	N/A	N/A
0	1	1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
1	0	0	133 MHz	66.7 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
1	0	1	126.7 MHz[1]	63.3 MHz[1]	63.3 MHz[1]	31.7 MHz[1]	48 MHz	14.318 MHz
1	1	0	200 MHz	66.7 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
1	1	1	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK

NOTE:
1. These frequencies are for debug and thus can vary a small amount from the values listed at the vendor's discretion.

SEL 100/133	SELA	SELB	HOST
0	0	0	Active 100 MHz
0	0	1	Active 100 MHz – ~5% over-clock
0	1	0	200 MHz, 50 MHz M_{REF}
0	1	1	HI-Z all outputs
1	0	0	Active 133 MHz
1	0	1	Active 133.3 MHz minus ~5 under-clock
1	1	0	200 MHz, 66 MHz M_{REF}
1	1	1	Test mode

POWER DOWN MODE

$\overline{PWRDWN}$	HOST/HOST_BAR	MREF/MREF_B	3V66	PCI	48 MHz	REF	14.318/66 MHz Seeds
Asserts low 0 = Active	HOST = $2*I_{REF}$ HOST_BAR	LOW	LOW	LOW	LOW	OFF	LOW/(if applicable)

NOTE:
1. The differential outputs should have a voltage forced across them when power down is asserted.

SPREAD SPECTRUM FUNCTION TABLE

$\overline{SPREAD}$	FUNCTION	48 MHz PLL REF/$\overline{MULTSEL0}$ REF/$\overline{MULTSEL1}$
$\overline{1}$	HOST/PCI/3V66/M_{REF}/M_{REF_B} No spread	No spread
$\overline{0}$	HOST/PCI/3V66/M_{REF}/M_{REF_B} Down spread –0.5%	No spread

HOST SWING SELECT FUNCTIONS – TABLE 1

MULTSEL0	MULTSEL1	BOARD IMPEDANCE	I_{REF}	I_{OH}	V_{OH} @ I_{REF} = 2.32 mA
0	0	**60 Ω**	**R_{REF} = 475 1% I_{REF} = –2.32 mA**	**I_{OH} = 5*I_{REF}**	**0.71 V**
0	0	50 Ω	R_{REF} = 475 1% I_{REF} = –2.32 mA	I_{OH} = 5*I_{REF}	0.59 V
0	1	60 Ω	R_{REF} = 475 1% I_{REF} = –2.32 mA	I_{OH} = 6*I_{REF}	0.85 V
0	1	**50 Ω**	**R_{REF} = 475 1% I_{REF} = –2.32 mA**	**I_{OH} = 6$_{REF}$**	**0.71 V**
1	0	60 Ω	R_{REF} = 475 1% I_{REF} = –2.32 mA	I_{OH} = 4*I_{REF}	0.56 V
1	0	50 Ω	R_{REF} = 475 1% I_{REF} = –2.32 mA	I_{OH} = 4*I_{REF}	0.47 V
1	1	60 Ω	R_{REF} = 475 1% I_{REF} = –2.32 mA	I_{OH} = 7*I_{REF}	0.99 V
1	1	50 Ω	R_{REF} = 475 1% I_{REF} = –2.32 mA	I_{OH} = 7*I_{REF}	0.82 V
0	0	30 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 5*I_{REF}	0.75 V
0	0	25 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 5*I_{REF}	0.62 V
0	1	30 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 6*I_{REF}	0.90 V
0	1	25 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 6*I_{REF}	0.75 V
1	0	30 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 4*I_{REF}	0.60 V
1	0	25 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 4*I_{REF}	0.50 V
1	1	30 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 7*I_{REF}	1.05 V
1	1	25 Ω	R_{REF} = 221 1% I_{REF} = –5 mA	I_{OH} = 7*I_{REF}	0.84 V

NOTE:
1. In Table 1, the outputs are optimized for the configurations in **bold**.

	CONDITIONS	CONFIGURATION	LOAD	MIN.	MAX.
I_{OUT}	V_{DD} = 3.3 V	All combinations, see Table 1	Nominal test load for given configuration	–7% of I_{OH} See Table 1	+7% of I_{OH} See Table 1
I_{OUT}	V_{DD} = 3.3 V ±5%	All combinations, see Table 1	Nominal test load for given configuration	–12% of I_{OH} See Table 1	+12% of I_{OH} See Table 1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3 V supply		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$		–50	mA
V_I	DC input voltage	Note 2			V
I_{OK}	DC output diode current	$V_O > V_{DD}$ or $V_O < 0$		±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{DD}		±50	mA
T_{STG}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package plastic medium-shrink (SSOP)	For temperature range: –40 to +125°C above +55°C derate linearly with 11.3 mW/K		850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3 V supply voltage		3.135	3.465	V
A_{VDD}	DC 3.3 V analog supply voltage		3.135	3.465	V
C_L	Capacitive load on:				
	PCICLK	Must meet PCI 2.1 requirements	10	30	pF
	3V66	1 device load, possible 2 loads	10	30	pF
	48 MHz clock	1 device load	10	20	pF
	REF	1 device load	10	20	pF
	M_{REF}, M_{REF_BAR}	1 device load	10	30	pF
f_{REF}	Reference frequency, oscillator normal value		14.31818	14.31818	MHz
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

POWER MANAGEMENT

CONDITION	MAXIMUM 3.3 V SUPPLY CONSUMPTION MAXIMUM DISCRETE CAP LOADS, V_{DDL}= 3.465 V ALL STATIC INPUTS = V_{DD3} OR V_{SS}
Power-down mode ($\overline{PWRDWN}$ = 0)	60 mA
Full active 100/133 MHz	250 mA

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS			UNIT
					T_{amb} = 0°C to +70°C			
		V_{DD} (V)	OTHER		MIN	TYP	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465			2.0		V_{DD3} + 0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465			V_{SS} – 0.3		0.8	V
V_{OH3}	3.3 V output HIGH voltage REF, 3V48M, 3V66, MREF, MREF_BAR, 48 MHz	3.135 to 3.465	I_{OH} = –1 mA		2.0		–	V
V_{OL3}	3.3 V output LOW voltage REF, 3V48M, 3V66, MREF, MREF_BAR, 48 MHz	3.135 to 3.465	I_{OH} = 1 mA		–		0.4	V
V_{OHP}	3.3 V output HIGH voltage PCI	3.135 to 3.465	I_{OH} = –1 mA		2.4		–	V
V_{OLP}	3.3 V output LOW voltage PCI	3.135 to 3.465	I_{OH} = 1 mA		–		0.55	V
I_{OH}	PCI, 3V66 3VMREF 3VMREF_BAR output HIGH current	3.135	V_{OUT} = 1.0 V	Type 5 12–55 Ω	–33			mA
		3.465	V_{OUT} = 3.135 V				–33	
I_{OH}	48 MHz, REF output HIGH current	3.135	V_{OUT} = 1.0 V	Type 3 20–60 Ω	–29			mA
		3.465	V_{OUT} = 3.135 V				–23	
I_{OH}	HOST/HOST_BAR OUTPUT CURRENT	3.135 to 3.465	0.66 V	Type X1	–11			mA
			0.76 V				–12.7	
I_{OL}	PCI, 3V66 3VMREF 3VMREF_BAR output LOW current	3.135	V_{OUT} = 1.95 V	Type 5 12–55 Ω	30			mA
		3.465	V_{OUT} = 0.4 V				38	
I_{OL}	48 MHz, REF output LOW current	3.135	V_{OUT} = 1.95 V	Type 3 20–60 Ω	29			mA
		3.465	V_{OUT} = 0.4 V				27	
V_{OL}	HOST/HOST_BAR	V_{SS} = 0.0	Rs = 33.2 Ω Rp = 49.9 Ω	Type X1	0.0		0.05	V
$\pm I_I$	Input leakage current	3.365	0 < V_{IN} < V_{DD3}		–5		5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{DD} or GND	I_O = 0			10	µA
Cin	Input pin capacitance						5	pF
Cxtal	Crystal input capacitance				13.5		22.5	pF
Cout	Output pin capacitance						6	pF

NOTE:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC characteristics section.

AC CHARACTERISTICS

V_{DD3} = 3.3 V –5%; $f_{crystal}$ = 14.31818 MHz

HOST CLOCK OUTPUTS (SEE FIGURE 1 FOR WAVEFORMS AND FIGURE 6 FOR TEST SETUP)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNITS	NOTES
		133 MHz MODE		100 MHZ MODE			
		MIN	MAX	MIN	MAX		
T_{PKP}	HOST CLK period	7.5	7.65	10.0	10.2	ns	11, 14, 20
AbsMinPeriod	Absolute Minimum Host CLK Period	7.35	N/A	9.85	N/A	ns	11, 14, 20
T_{RISE}	HOST CLK rise time	175	700	175	700	ps	11, 15, 20
T_{FALL}	HOST CLK fall time	175	700	175	700	ps	11, 15, 20
T_{JITTER}	HOST CLK cycle-to-cycle jitter		200		200	ps	11, 12, 14, 20
DUTY CYCLE	Output duty cycle	45	55	45	55	%	11, 14, 20
T_{SKEW}	HOST CLK pin-to-pin skew		150		150	ps	11, 14, 20
Rise/Fall Matching	Rise and fall time matching		35%		35%		11, 16, 20
Vcrossover		45% V_{OH}	60% V_{OH}	45% V_{OH}	60% V_{OH}	V	11, 14, 20

MREF OUTPUTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNITS	NOTES
		133 MHz MODE		100 MHz MODE			
		MIN	MAX	MIN	MAX		
T_{PKP}	MREF period	15.0	15.3	20.0	20.4	ns	2, 9, 20
T_{PKH}	MREF HIGH time	5.25	N/A	7.5	N/A	ns	5, 10, 20
T_{PKL}	MREF LOW time	5.05	N/A	7.3	N/A	ns	6, 10, 20
T_{RISE}	MREF rise time	0.5	2.0	0.5	2.0	ns	8, 20
T_{FALL}	MREF fall time	0.5	2.0	0.5	2.0	ns	8, 20
T_{JITTER}	Cycle-to-cycle jitter		250		250	ps	18, 20
DUTY CYCLE	Output Duty Cycle	45	55	45	55	%	18, 20

3V66 OUTPUTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNIT	NOTES
		133 MHz MODE		100 MHz MODE			
		MIN	MAX	MIN	MAX		
T_{PKP}	3V66 period	15.0	16.0	15.0	16.0	ns	2, 4, 9, 20
T_{PKH}	3V66 HIGH time	5.25	N/A	5.25	N/A	ns	5, 10, 20
T_{PKL}	3V66 LOW time	5.05	N/A	5.05	N/A	ns	6, 10, 20
T_{RISE}	3V66 rise time	0.5	2.0	0.5	2.0	ns	8, 20
T_{FALL}	3V66 fall time	0.5	2.0	0.5	2.0	ns	8, 20
T_{JITTER}	Cycle-to-cycle jitter		300		300	ps	18, 20
DUTY CYCLE	Output Duty Cycle	45	55	45	55	%	18, 20
T_{SKEW}	Pin-to-pin skew		250		250	ps	20

PCI OUTPUTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNITS	NOTES
		133 MHz MODE		100 MHz MODE			
		MIN	MAX	MIN	MAX		
T_{PKP}	PCI period	30.0	N/A	30.0	N/A	ns	2, 3, 9, 20
T_{PKH}	PCI HIGH time	12.0	N/A	12.0	N/A	ns	5, 10, 20
T_{PKL}	PCI LOW time	12.0	N/A	12.0	N/A	ns	6, 10, 20
T_{RISE}	PCI rise time	0.5	2.0	0.5	2.0	ns	8, 20
T_{FALL}	PCI fall time	0.5	2.0	0.5	2.0	ns	8, 20
T_{JITTER}	Cycle-to-cycle jitter		500		500	ps	18, 20
DUTY CYCLE	Output Duty Cycle	45	55	45	55	%	18, 20
T_{SKEW}	Pin-to-pin skew		500		500	ps	18, 20

USB CLOCK OUTPUT, 48 MHz (LUMP CAPACITANCE TEST LOAD = 20 pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNITS	NOTES
		48 MHz					
		MIN	MAX	MIN	MAX		
f	Frequency, Actual	48.008				MHz	
f_D	Deviation from 48 MHz	+167				ppm	
T_{HKL}	3V48MHZCLK LOW time	5.05	N/A	5.05	N/A	ns	20
T_{RISE}	3V48MHZCLK rise time	1.0	4.0	1.0	4.0	ns	8, 20
T_{FALL}	3V48MHZCLK fall time	1.0	4.0	1.0	4.0	ns	8, 20
T_{JITTER}	Cycle-to-cycle jitter		350		350	ps	18, 20
DUTY CYCLE	Output Duty Cycle	45	55	45	55	%	18, 20

REF CLOCK OUTPUT, (LUMP CAPACITANCE TEST LOAD = 20 pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNITS	NOTES
		48 MHz					
		MIN	MAX	MIN	MAX		
f	Frequency, Actual	14.318				MHz	20
T_{HKL}	REF CLK LOW time	31.0	36.67	31.0	36.67	ns	20
T_{HKH}	REF CLK HIGH time	32.0	37.5	32.0	37.5	ns	20
T_{RISE}	REF CLK rise time	N/A	N/A	N/A	N/A	ns	8, 20
T_{FALL}	REF CLK fall time	N/A	N/A	N/A	N/A	ns	8, 20
T_{JITTER}	Cycle-to-cycle jitter		1000		1000	ps	18, 20
DUTY CYCLE	Output Duty Cycle	45	55	45	55	%	18, 20

ALL OUTPUTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C				UNITS	NOTES
		133 MHz MODE		100 MHz MODE			
		MIN	MAX	MIN	MAX		
TpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	ns	20
TpLZ, tpZH	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	ns	20
T_{STABLE}	All clock Stabilization from Power-up		3		3	ms	7, 20

GROUP OFFSET LIMITS

GROUP	OFFSET	MEASUREMENT LOADS (LUMPED)	MEASURE POINTS	NOTES
3V66 to PCI	1.5–3.5 ns 3V66 leads	3V66 @ 30 pf PCI @ 30 pf	3V66 @ 1.5 V PCI @ 1.5 V	19, 20

NOTES:
1. Output drivers must have monotonic rise/fall times through the specified V_{OL}/V_{OH} levels.
2. Period, jitter, offset and skew measured on rising edge @ 1.25 V for 2.5 V clocks and @ 1.5 V for 3.3 V clocks.
3. The PCI clock is the Host clock divided by four at Host = 133 MHz. PCI clock is the Host clock divided by three at Host = 100 MHz.
4. 3V66 is internal VCO frequency divided by four for Host = 133 MHz. 3V66 clock is internal VCO frequency divided by three at Host = 100 MHz.
5. T_{HKH} is measured at 2.0 V for 2.5 V outputs and 2.4 V for 3.3 V outputs as shown in Figure 7.
6. T_{HKL} is measured at 0.4 V for all outputs as shown in Figure 7.
7. The time is specified from when V_{DDQ} achieves its normal operating level (typical condition V_{DDQ} = 3.3 V) until the frequency output is stable and operating within specification.
8. T_{HRISE} and T_{HFALL} are measured as a transition through the threshold region V_{OL} = 0.4 V and V_{OH} = 2.4 V (1 mA) JEDEC specification.
9. The average period over any 1 μs period of time must be greater than the minimum specified period.
10. Calculated at minimum edge-rate (1 V/ns) to guarantee 45/55% duty-cycle. Pulse width is required to be wider at faster edge-rate to ensure duty-cycle specification is met.
11. Test load is Rs = 33.2 Ω, Rp = 49.9 Ω.
12. Must be guaranteed in a realistic system environment.
13. Configured for V_{OH} = 0.71 V in a 50 Ω environment.
14. Measured at crossing points.
15. Measured at 20% to 80%.
16. Determined as a fraction of 2* (Trp–Trn)/(Trp+Trn) where Trp is a rising edge and Trn is an intersecting falling edge.
17. Voltage measure point (Vm = 1.25 V). V_{DD} = 2.5 V.
18. Voltage measure point (Vm = 1.5 V). V_{DD} = 3.3 V.
19. All offsets are to be measured at rising edges.
20. Parameters are guaranteed by design.

AC WAVEFORMS

V_M = 1.25 V @ V_{DDL} and 1.5 V @ V_{DD3}
$V_X = V_{OL} + 0.3$ V
$V_Y = V_{OH} - 0.3$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

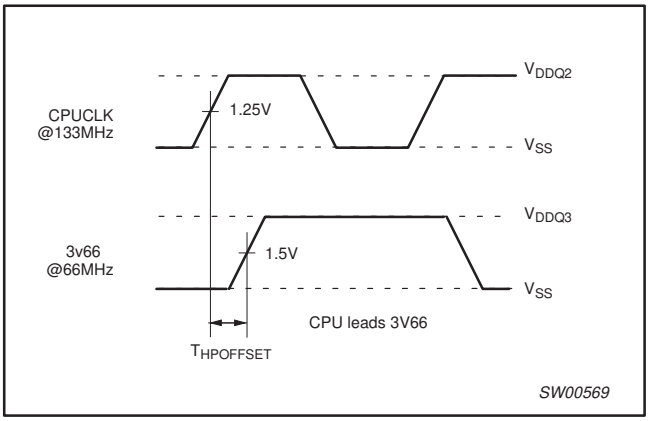


Figure 1. Host clock

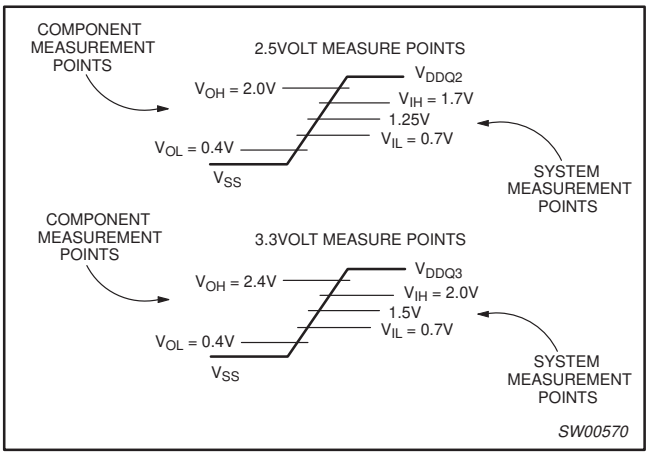


Figure 2. 3.3 V clock waveforms

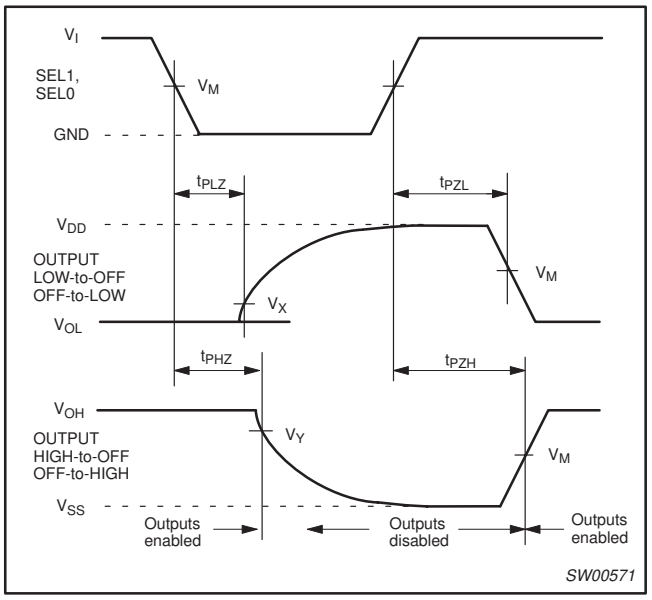


Figure 3. State enable and disable times

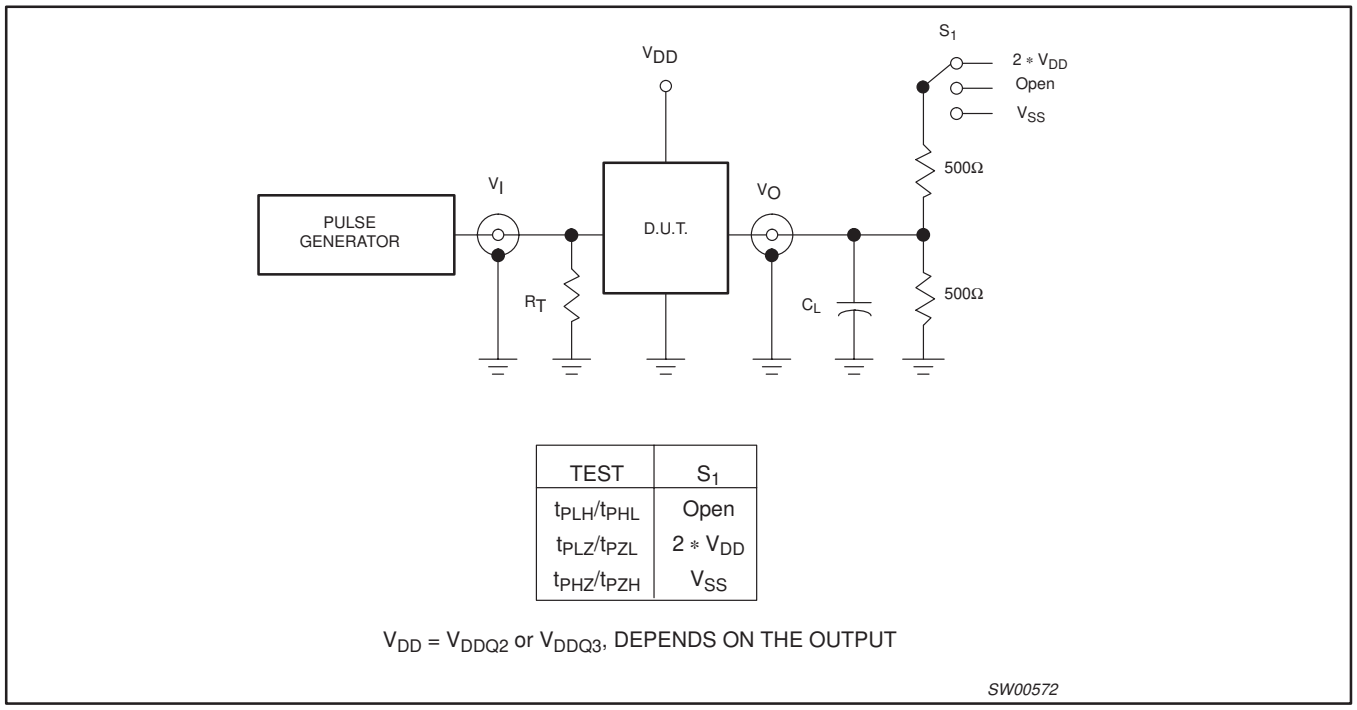


Figure 4. Load circuitry for switching times

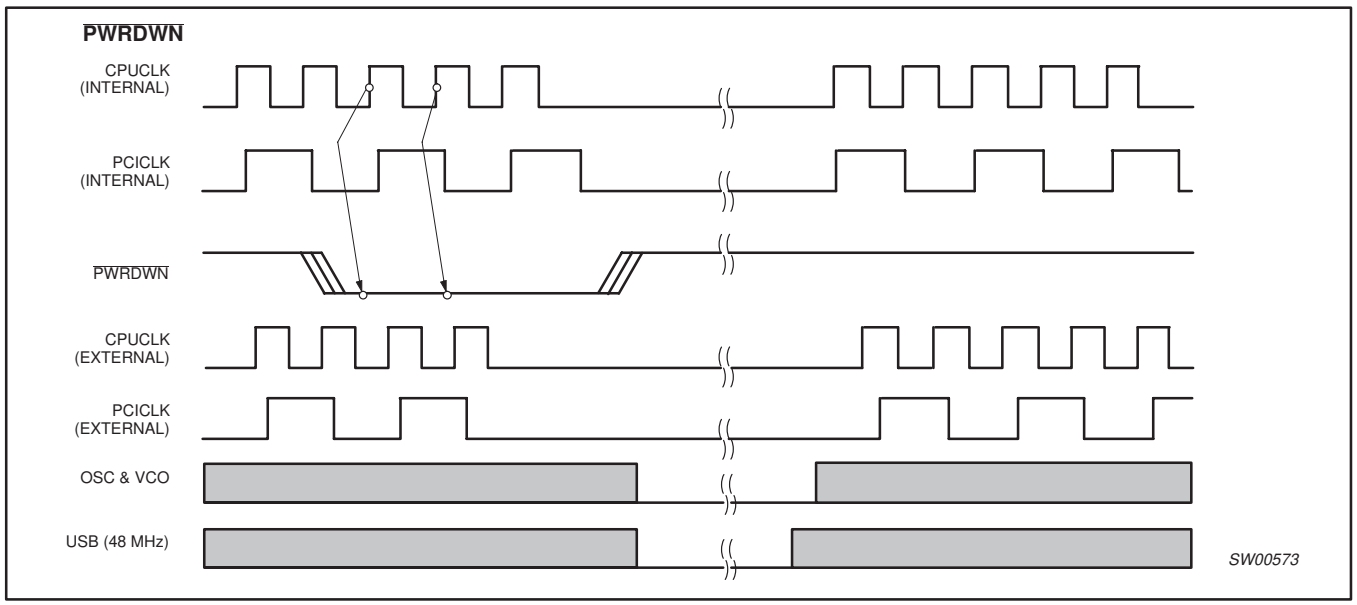


Figure 5. Power management

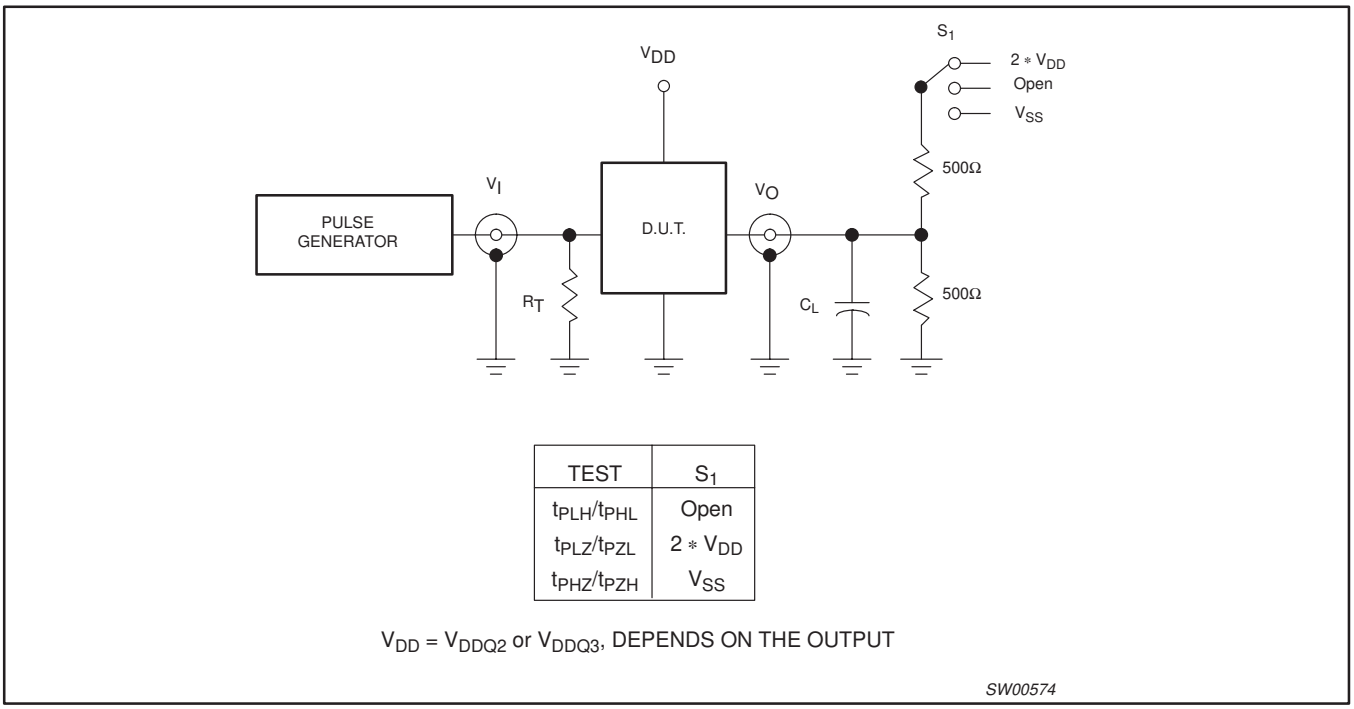


Figure 6. Host clock measurements

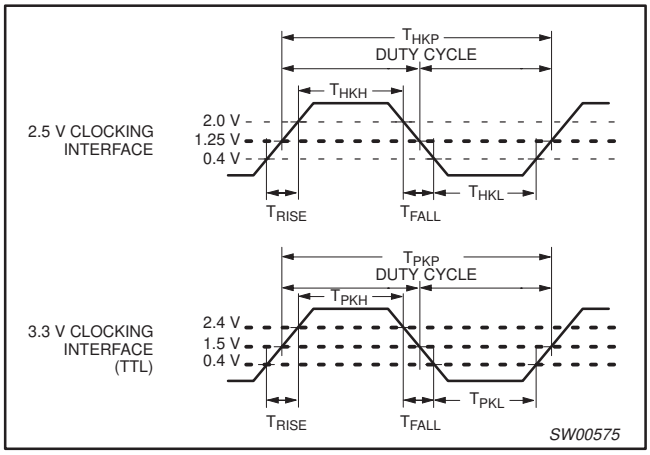
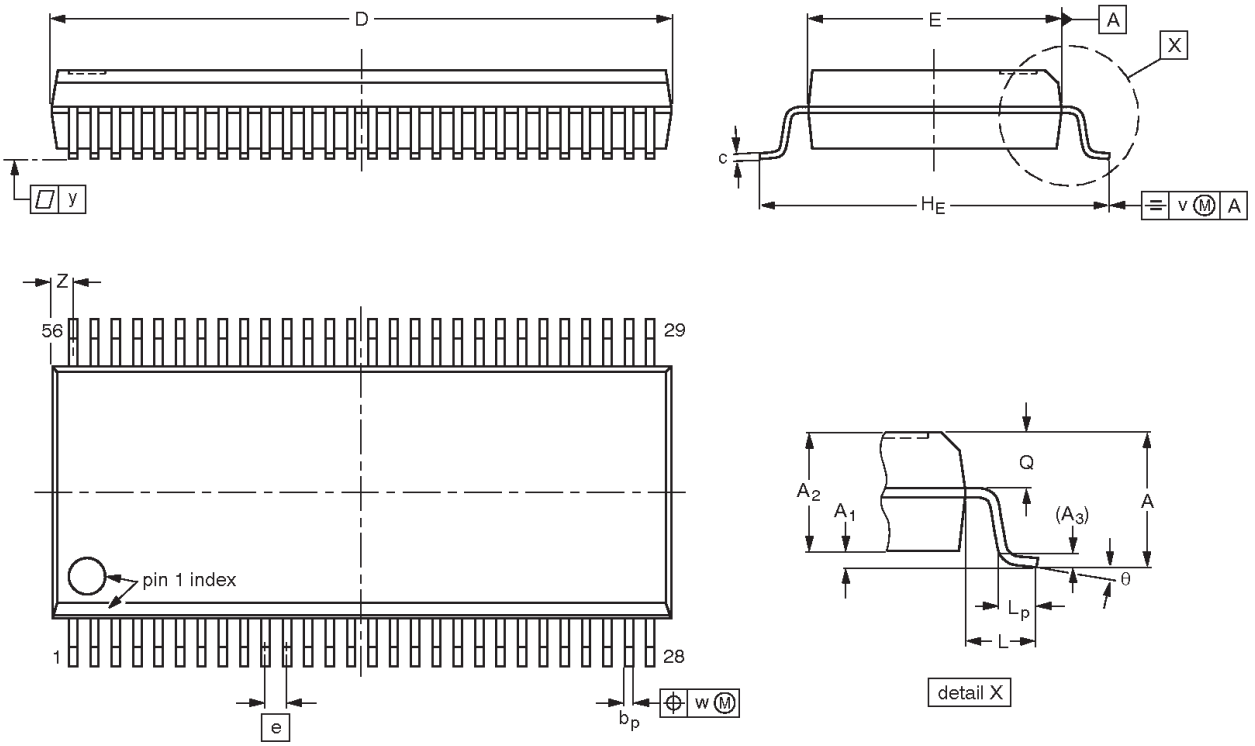
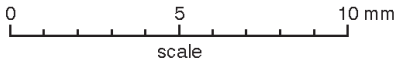


Figure 7. 2.5 V/3.3 V clock waveforms

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				~~95-02-04~~ 99-12-27

CK00 (100/133MHz) spread spectrum differential system clock generator

PCK2020

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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