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DATA SHEET

PCK2111
1:10 LVDS clock distribution device

Product Data
Supersedes data of 2002 May 14

2002 Dec 16

Philips
Semiconductors

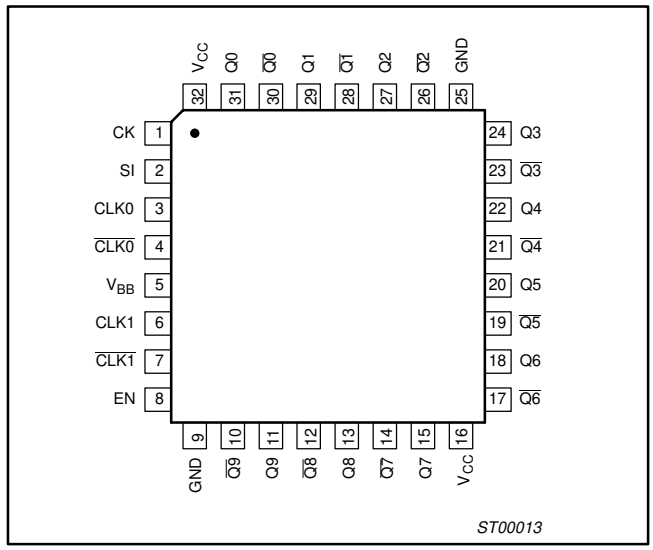
PHILIPS

1:10 LVDS clock distribution device PCK2111

FEATURES

- 100 ps part-to-part skew
- 35 ps output-to-output skew
- Differential design
- Meets LVDS specification for driver outputs and receiver inputs
- Reference voltage available output V_{BB}
- Low voltage V_{CC} range of +2.375 V to 2.625 V
- High signalling rate capability (above 622 MHz)
- Supports open, short, and terminated input fail-safe (HIGH output state)
- Programmable drivers power off control
- PCK2111 is identical to and replaces PTN2111
- Available in LQFP32 package

PIN CONFIGURATION



DESCRIPTION

The PCK2111 is a low skew programmable 1:10 LVDS clock distribution device. The selected input signal is fanned out to 10 identical differential outputs.

The PCK2111 features an 11-bit Shift Register with a serial-in and a Control Register. The purpose of the Control Register is to enable or power off each output clock channel and to select the clock input.

The PCK2111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device. The final result is a dependable guaranteed low skew device.

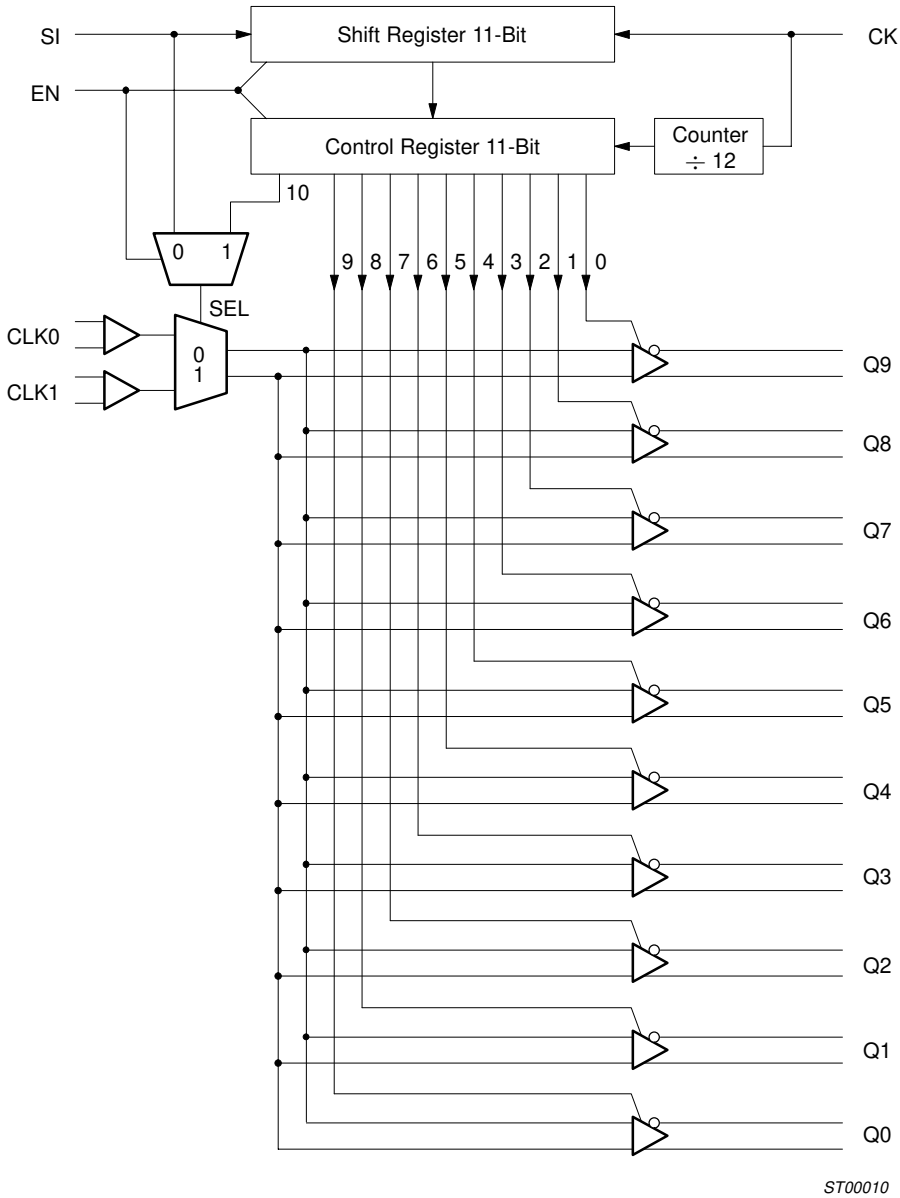
The PCK2111 can be used for high performance clock distribution in +2.5 V systems with LVDS levels. Designers can take advantage of the device's performance to distribute low skew clocks across the backplane or the board.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	CK	Control register clock
2	SI	Control register serial-in/CLK_SEL
3	CLK0	Differential input
4	$\overline{CLK0}$	Differential input
5	V_{BB}	Output reference voltage
6	CLK1	Differential input
7	$\overline{CLK1}$	Differential input
8	EN	Device enable/program
9, 25	GND	Ground
16, 32	V_{CC}	Supply voltage
31, 29, 27, 24, 22, 20, 18, 15, 13, 11	Q[0:9]	Differential outputs
30, 28, 26, 23, 21, 19, 17, 14, 12, 10	$\overline{Q}$[0:9]	Differential outputs

TYPE NUMBER	NAME	DESCRIPTION	VERSION
PCK2111BD	LQFP32	Plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm	SOT358-1

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation under these conditions is not implied.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{CC}	Supply voltage	-0.3 to 2.8	V
I_{OSD}	Driver short circuit current	continuous	
ESD	Electrostatic discharge (Human Body Model 1.5 kΩ, 100 pF)	>2	kV
T_j	Junction temperature	150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Supply voltage	2.375	2.625	V
V_{IR}	Receiver input voltage	GND	V_{CC}	
T_{amb}	Operating ambient temperature range in free air	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

T_{amb} = -40 °C to +85 °C unless otherwise specified; V_{CC} = 2.5 V ±5% (Notes 1, 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNIT
Driver						
V_{OD}	Output differential voltage	R_L = 100 Ω	250	350	450	mV
ΔV_{OD}	V_{OD} magnitude change	R_L = 100 Ω	—	—	50	mV
V_{OS}	Offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} magnitude change	R_L = 100 Ω	—	—	50	mV
I_{OSD}	Output short circuit current	V_O = 0 V	—	15	40	mA
		V_{OD} = 0 V	—	7	15	mA
Receiver						
V_{IDH}	Input threshold HIGH		—	—	100	mV
V_{IDL}	Input threshold LOW		-100	—	—	mV
I_{IN}	Input current	V_{IN} = 0 V	—	50	100	µA
		V_{IN} = V_{CC}	—	50	100	µA
Device						
V_{BB}	Output reference voltage	V_{CC} = 2.5 V; $\|I_{OUT}\| \leq$ 100 µA	1.15	1.25	1.35	V
I_{CCD}	Power supply current	All drivers enabled and loaded; input frequency = 800 MHz	—	190	230	mA
C_{IN}	Input capacitance	V_{IN} = 0 V to V_{CC}	—	5	—	pF
C_{OUT}	Output capacitance		—	5	—	pF
V_{IH}	Logic input HIGH threshold	V_{CC} = 2.5 V	2	—	—	V
V_{IL}	Logic input LOW threshold	V_{CC} = 2.5 V	—	—	0.8	V
I_I	Logic input current	V_{CC} = 2.5 V; V_{IN} = V_{CC} or GND	—	—	±10	µA

NOTES:
1. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
2. All typical values are given for V_{CC} = +2.5 V and T_{amb} = +25 °C, unless otherwise specified.
3. C_L includes probe and fixture capacitance.
4. Generator waveforms for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, 50% duty cycle.
5. The PCK2111 is a current mode device, and only functions to datasheet specifications when a resistive load is applied to the drives outputs.

AC ELECTRICAL CHARACTERISTICS (LVDS)

T_{amb} = -40 °C to +85 °C unless otherwise specified; V_{CC} = 2.5 V ±5% (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time LOW to HIGH	R_L = 100 Ω; C_L = 5 pF	—	460	560	ps
t_{THL}	Transition time HIGH to LOW	R_L = 100 Ω; C_L = 5 pF	—	460	560	ps
t_{PLH} t_{PHL}	Propagation delay to output		—	—	2	ns
f_{MAX}	Maximum input frequency		650	800	—	MHz
t_{skew}	Within-device skew		—	35	—	ps
	Part-to-part skew		—	100	—	ps
	Pulse skew		—	50	—	ps
t_{JITTER}	Cycle-to-cycle jitter		—	—	1	ps

NOTE:
1. Generator waveforms for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, 50% duty cycle.

CONTROL REGISTER SPECIFICATION

The PCK2111 is provided with an 11-bit shift register with a serial-in and a Control Register. The purpose is to enable or power-off each output clock channel and to select the clock input. The PCK2111 provides two working modes: Programmed mode, and Standard mode.

Programmed Mode (EN = 1)

The shift register has a serial input to load the working configuration. Once the configuration is loaded with 11 clock pulses, another clock pulse loads the configuration into the Control Register. To restart the configuration of the shift register, a reset of the state machine must be done with a clock pulse on CK, and the EN set to LOW. The Control Register can be configured only one time after each reset. D0 is the first bit shifted in, D10 is the last bit shifted in. Bit D0 controls Q9, D9 controls Q0, and D10 controls CLKIN.

Standard Mode (EN = 0)

In Standard Mode, the PCK2111 is not programmable. All clock buffer outputs are enabled. The LVDS clock input is selected from Clock0 or Clock1 with the SI pin, as shown in the Truth Table.

Table 1. Truth Table of State Machine Inputs

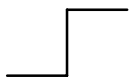
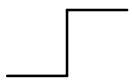
EN	SI	CK	OUTPUT
L	L	X	All outputs enabled, Clock0 selected, Control Register disabled.
L	H	X	All outputs enabled, Clock1 selected, Control Register disabled.
H	L		First stage stores “L”, other stages store the data of previous stage.
H	H		First stage stores “H”, other stages store the data of previous stage.
L	X		Reset of the state machine, Shift register, and Control Register.

Table 2. Configuration of the Control Register

Control Register bit	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
Function	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	CLK_SEL

Table 3. Truth Table of the Control Register

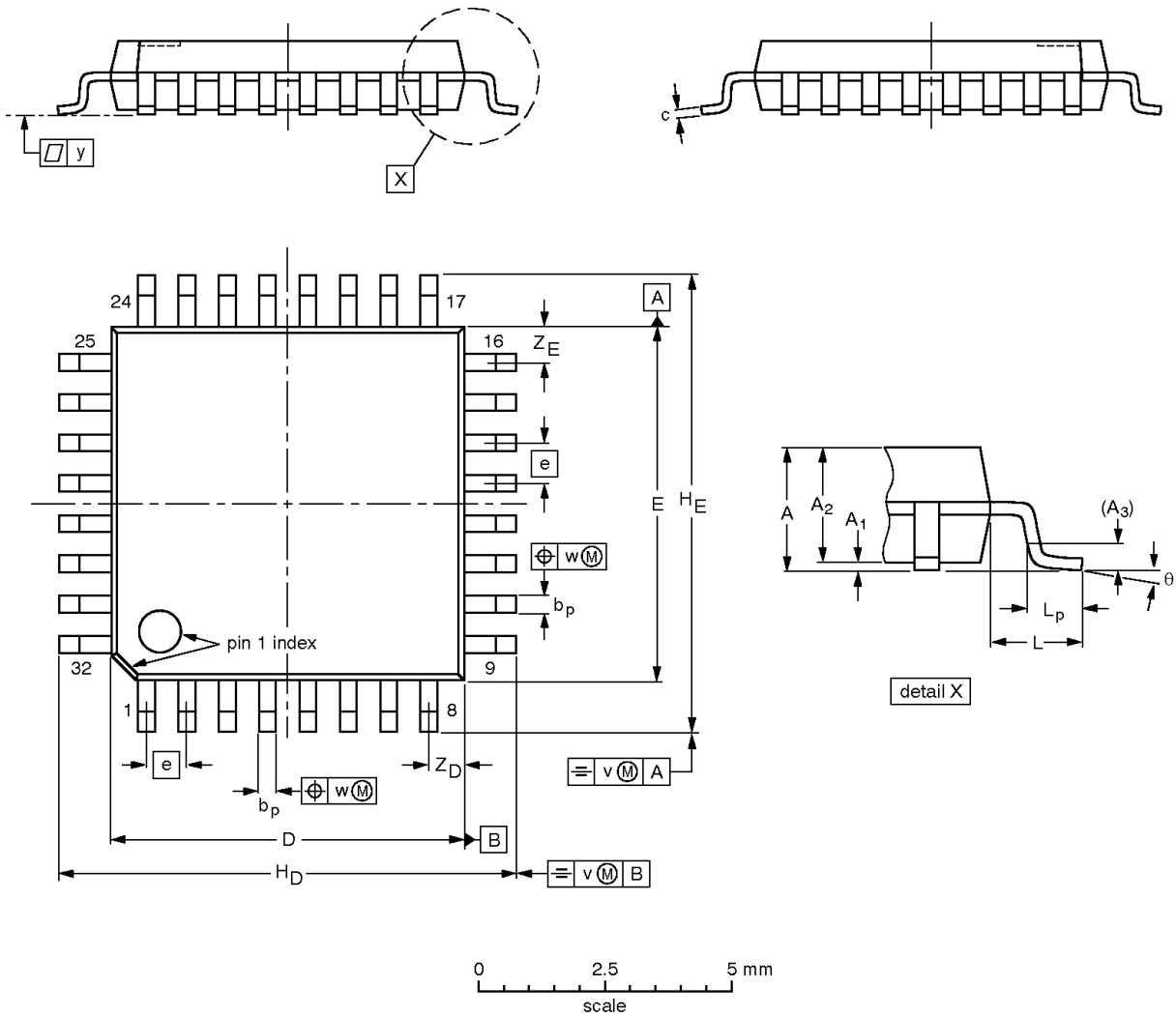
D10	Dn[0:9]	Qn[0:9]
L	H	Clock0
H	H	Clock1
X	L	Qn output disabled

X = Don’t Care

AC ELECTRICAL CHARACTERISTICS (Control Register)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum frequency of shift register		50	—	—	MHz
t_s	Clock to SI setup time		—	—	4.0	ns
t_h	Clock to SI hold time		—	—	1.0	ns
t_{rem}	Enable to clock removal time		—	—	4.0	ns
t_w	Minimum clock pulse width		5	—	—	ns

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm SOT358-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1	136E03	MS-026				~~99-12-27~~ 00-01-19

REVISION HISTORY

Rev	Date	Description
_2	20021216	Product data (9397 750 10861); ECN 853-2345 29262 of 09 December 2002 Modifications: • Addition of jitter specification to datasheet.
_1	20020514	Product data (9397 750 09823); ECN 853-2345 28198 of 14 May 2002.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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