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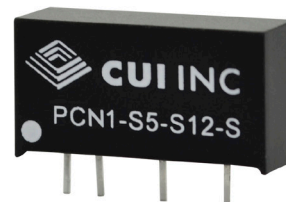
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**SERIES:** PCN1-S | **DESCRIPTION:** DC-DC CONVERTER

**FEATURES**

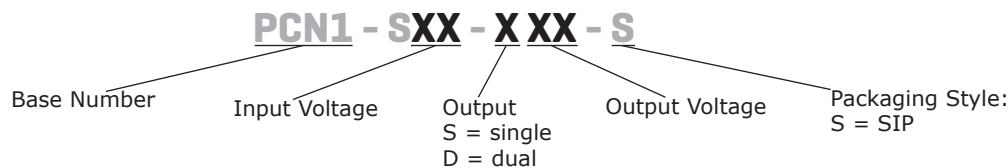
- up to 1 W isolated output
- industry standard SIP package
- nominal input voltages: 5, 12, 24 Vdc
- single/dual unregulated output
- 1,500 Vdc isolation voltage
- low ripple and noise
- -40 to 100°C
- efficiency up to 83%



MODEL	input voltage		output voltage	output current		output power	ripple & noise <sup>1</sup>	efficiency
	typ (Vdc)	range (Vdc)	(Vdc)	min (mA)	max (mA)	max (W)	max (mVp-p)	typ (%)
PCN1-S5-S5-S	5	4.5~5.5	5	0	200	1	75	79
PCN1-S5-S12-S	5	4.5~5.5	12	0	84	1	75	79
PCN1-S5-S15-S	5	4.5~5.5	15	0	67	1	75	79
PCN1-S5-D5-S	5	4.5~5.5	±5	0	±100	1	75	74
PCN1-S5-D12-S	5	4.5~5.5	±12	0	±42	1	75	78
PCN1-S5-D15-S	5	4.5~5.5	±15	0	±33	1	75	78
PCN1-S12-S5-S	12	10.8~13.2	5	0	200	1	75	80
PCN1-S12-S12-S	12	10.8~13.2	12	0	84	1	75	81
PCN1-S12-S15-S	12	10.8~13.2	15	0	67	1	75	81
PCN1-S12-D5-S	12	10.8~13.2	±5	0	±100	1	75	77
PCN1-S12-D12-S	12	10.8~13.2	±12	0	±42	1	75	80
PCN1-S12-D15-S	12	10.8~13.2	±15	0	±33	1	75	81
PCN1-S24-S5-S	24	21.6~26.4	5	0	200	1	75	80
PCN1-S24-S12-S	24	21.6~26.4	12	0	84	1	75	83
PCN1-S24-S15-S	24	21.6~26.4	15	0	67	1	75	81
PCN1-S24-D5-S	24	21.6~26.4	±5	0	±100	1	75	79
PCN1-S24-D12-S	24	21.6~26.4	±12	0	±42	1	75	81
PCN1-S24-D15-S	24	21.6~26.4	±15	0	±33	1	75	82

Notes: 1. At full load, nominal input, 20 MHz bandwidth oscilloscope, with a 0.33 μF ceramic capacitor on the output.  
 2. Required to add a 2.2 μF (5 & 12 Vdc input models) or 4.7 μF (24 Vdc input models) ceramic capacitor to the input to reduce input voltage stress.  
 3. All specifications are measured at Ta=25°C, nominal input voltage, and rated output load unless otherwise specified.

**PART NUMBER KEY**



## INPUT

parameter	conditions/description	min	typ	max	units
operating input voltage	5 Vdc input models	4.5	5	5.5	Vdc
	12 Vdc input models	10.8	12	13.2	Vdc
	24 Vdc input models	21.6	24	26.4	Vdc
surge voltage	for maximum of 100 ms				
	5 Vdc input models			9	Vdc
	12 Vdc input models			18	Vdc
	24 Vdc input models			30	Vdc
current	5 Vdc input models		250		mA
	12 Vdc input models		110		mA
	24 Vdc input models		50		mA
filter	capacitive				
input reverse polarity protection	no				
input fuse	0.5 A time delay fuse for all models (recommended)				

Notes: 1. Required to add a 2.2  $\mu$ F (5 & 12 Vdc input models) or 4.7  $\mu$ F (24 Vdc input models) ceramic capacitor to the input to reduce input voltage stress.

## OUTPUT

parameter	conditions/description	min	typ	max	units
maximum capacitive load	single output models			220	$\mu$ F
	dual output models			100	$\mu$ F
voltage accuracy				$\pm 3.0$	%
line regulation	1.0% change in input voltage			$\pm 1.2$	%
load regulation	from 20% load to full load			$\pm 10$	%
switching frequency	at nominal Vin, full load				
	24 Vdc input models		75		kHz
	all other models		100		kHz
temperature coefficient				$\pm 0.05$	%/ $^{\circ}$ C

## PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	momentary			1	s

## SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
isolation voltage	input to output for 1 minute	1,500			Vdc
isolation resistance	input to output	1,000			M $\Omega$
isolation capacitance	input to output		10		pF
conducted emissions	EN 55022 Class B (external circuit required, see Figure 4)				
MTBF	as per MIL-HDBK-217F, full load, GB, 25 $^{\circ}$ C		1,500,000		hours
RoHS	2011/65/EU				

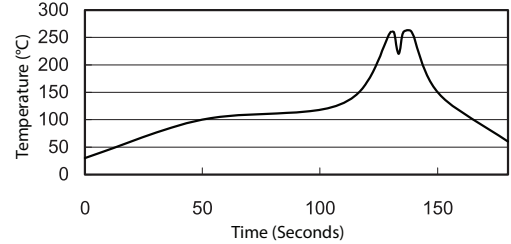
## ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curve	-40		100	$^{\circ}$ C
storage temperature		-55		125	$^{\circ}$ C
operating humidity	non-condensing			95	%

## SOLDERABILITY

parameter	conditions/description	min	typ	max	units
wave soldering	see wave soldering profile			260	°C

- Notes:
1. Soldering materials: Sn/Cu/Ni
  2. Ramp up rate during preheat: 1.4°C/s (from 50°C to 100°C)
  3. Soaking temperature: 0.5°C/s (from 100°C to 130°C), 60±20 seconds
  4. Peak temperature: 260°C, above 250°C for 3~6 seconds
  5. Ramp down rate during cooling: -10°C/s (from 260°C to 150°C)



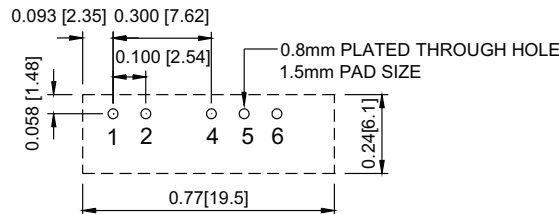
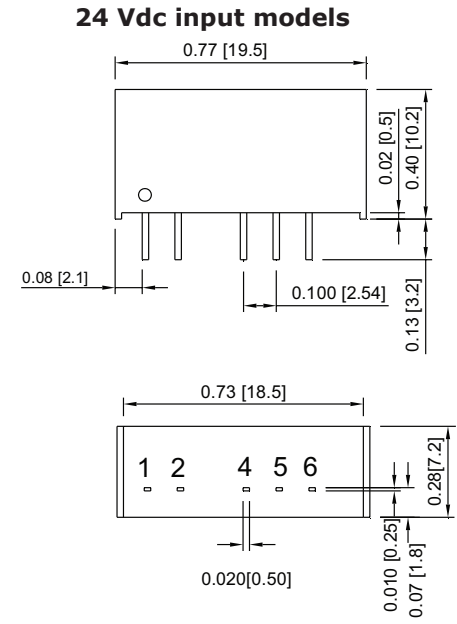
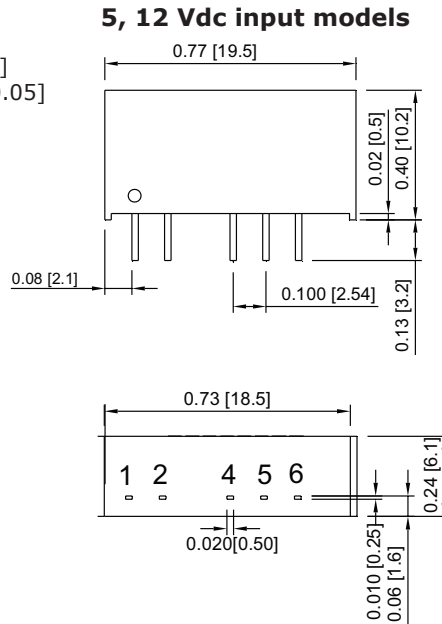
## MECHANICAL

parameter	conditions/description	min	typ	max	units
dimensions	5, 12 Vdc input models: 0.77 x 0.24 x 0.40 [19.5 x 6.1 x 10.2 mm] 24 Vdc input models: 0.77 x 0.28 x 0.40 [19.5 x 7.2 x 10.2 mm]				inches inches
case material	non-conductive black plastic				
weight	24 Vdc input models all other models		2.7 1.8		g g

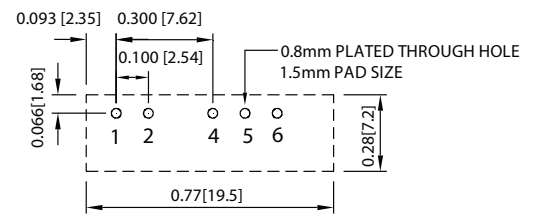
## MECHANICAL DRAWING

units: inches [mm]  
tolerance: X.XX ±0.01 [±0.25]  
          X.XXX ±0.005 [±0.13]  
pin section tolerance: ±0.002[±0.05]

PIN CONNECTIONS		
PIN	Function	
	Single	Dual
1	+Vin	+Vin
2	-Vin	-Vin
4	-Vout	-Vout
5	No pin	Common
6	+Vout	+Vout



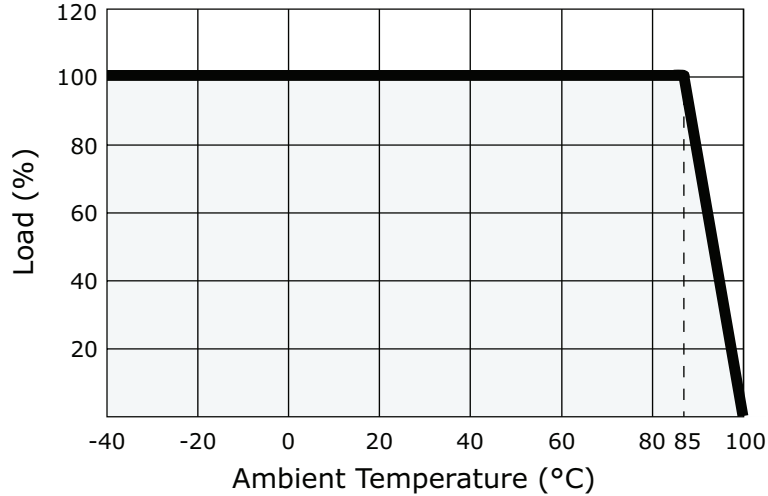
Recommended PCB Layout  
Top View



Recommended PCB Layout  
Top View

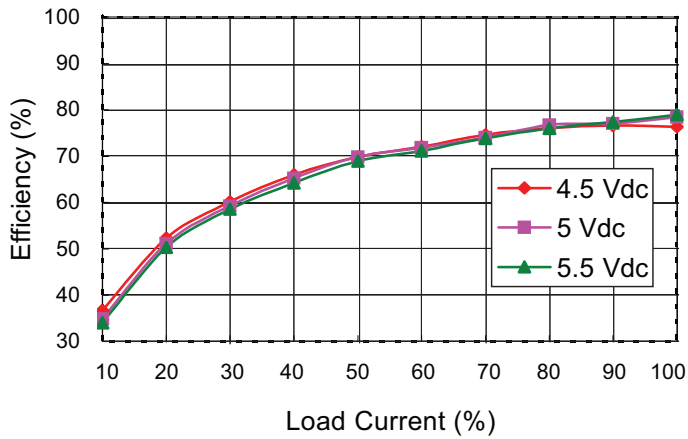
## DERATING CURVE

Temperature Derating Curve  
(Natural Convection)

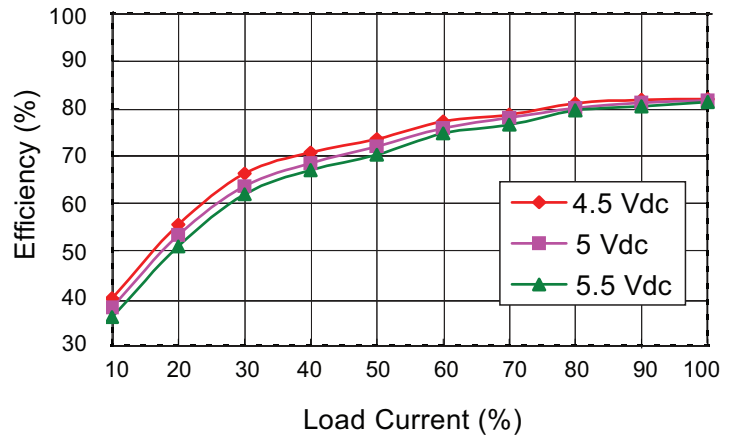


## EFFICIENCY CURVES

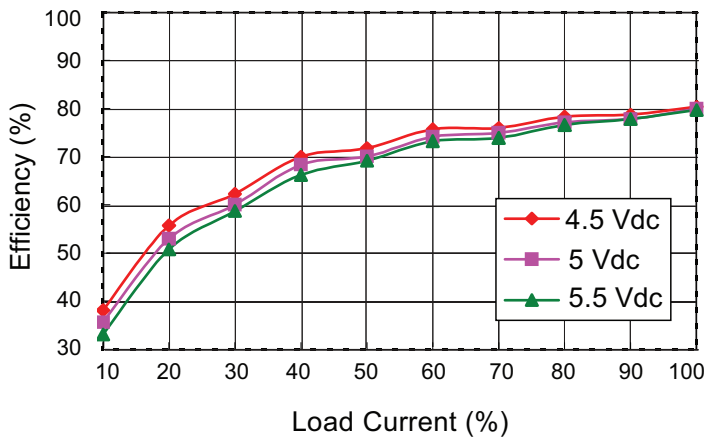
PCN1-S5-S5-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



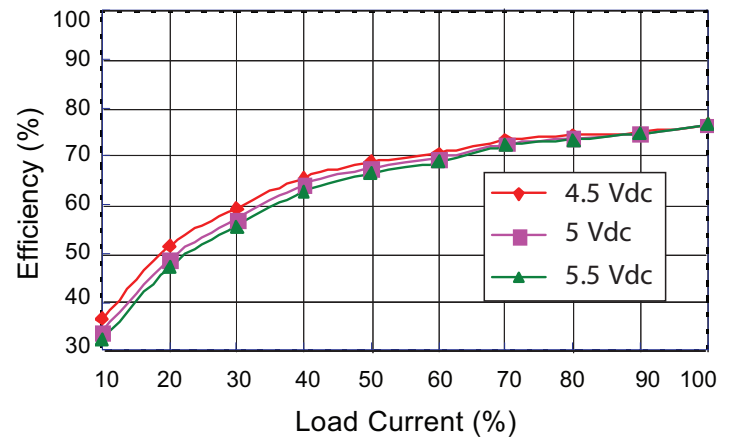
PCN1-S5-S12-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



PCN1-S5-S15-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)

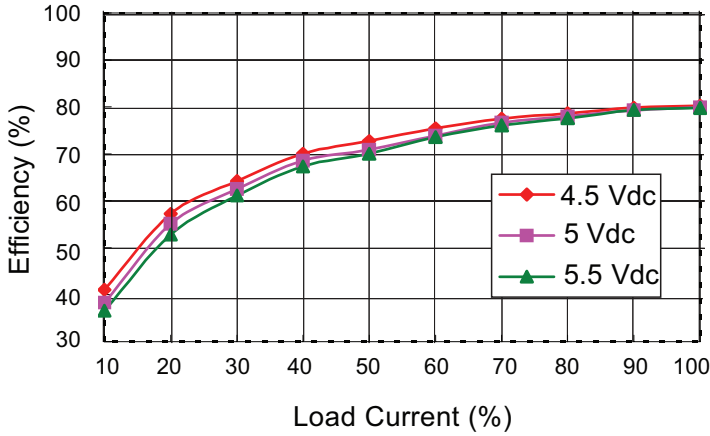


PCN1-S5-D5-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)

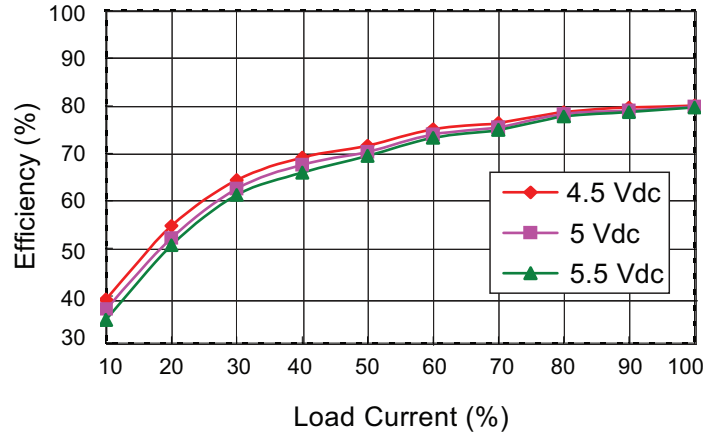


## EFFICIENCY CURVES (CONTINUED)

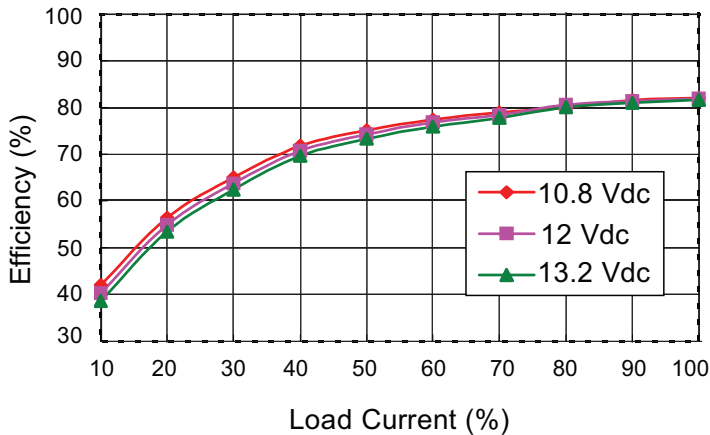
PCN1-S5-D12-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



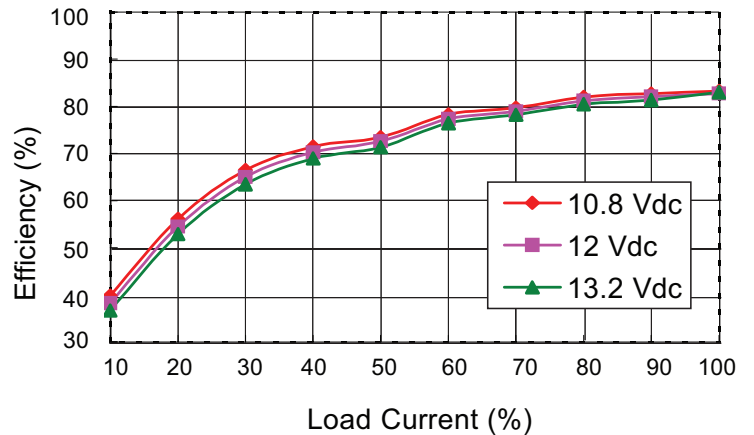
PCN1-S5-D15-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



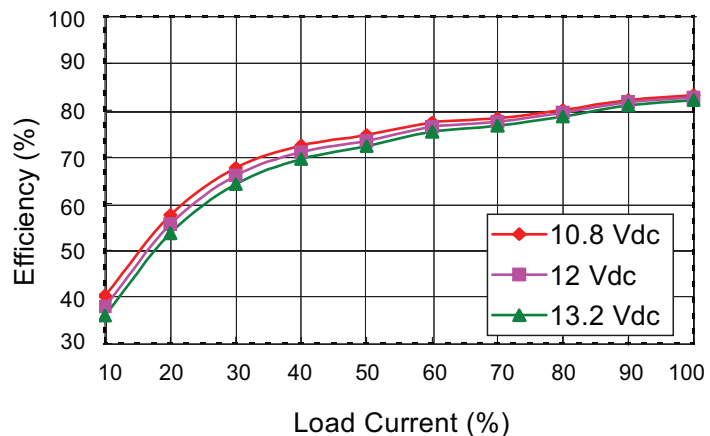
PCN1-S12-S5-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



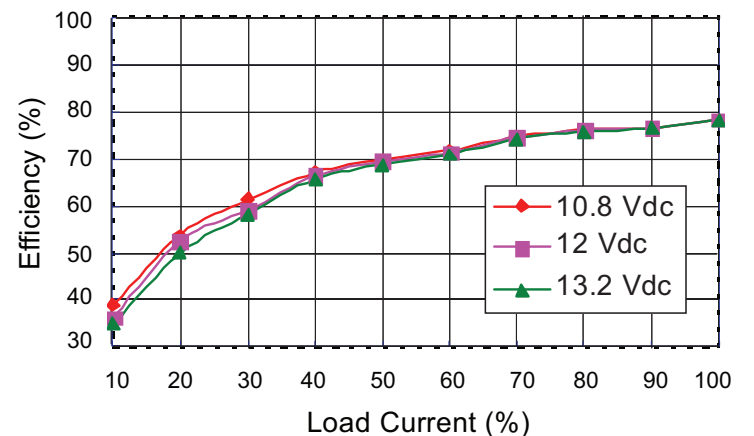
PCN1-S12-S12-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



PCN1-S12-S15-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)

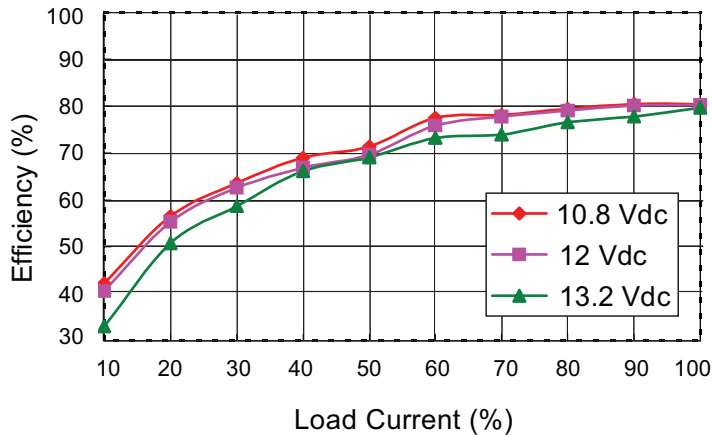


PCN1-S12-D5-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)

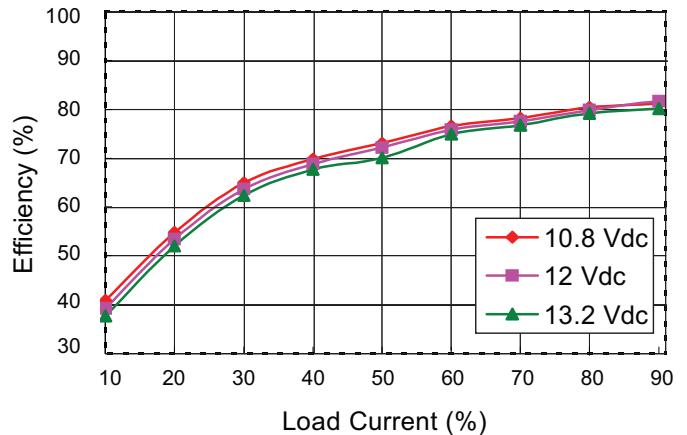


## EFFICIENCY CURVES (CONTINUED)

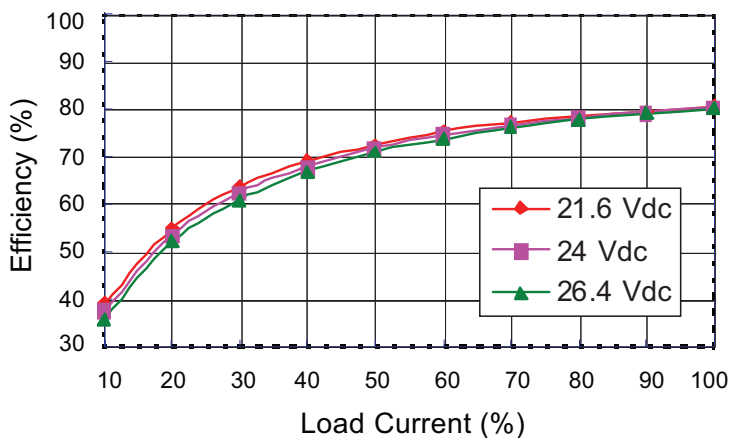
PCN1-S12-D12-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



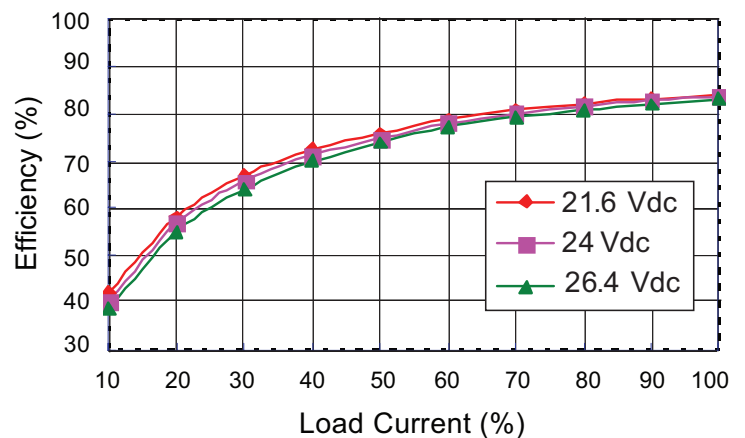
PCN1-S12-D15-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



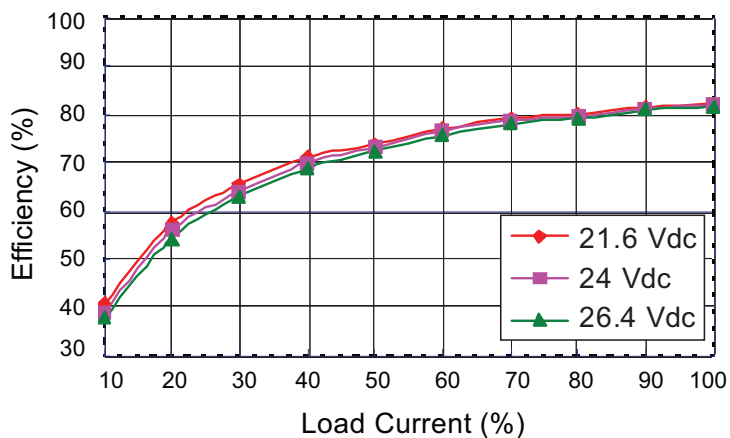
PCN1-S24-S5-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



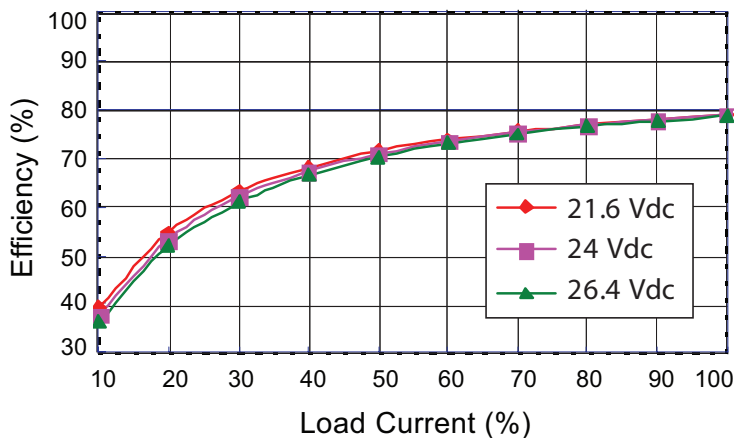
PCN1-S24-S12-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



PCN1-S24-S15-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)

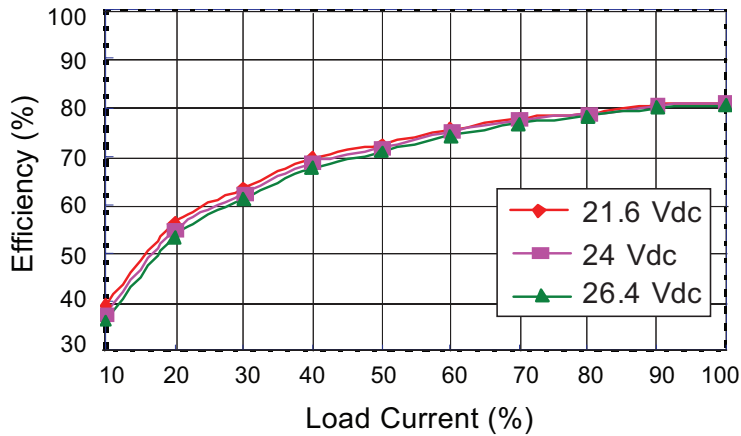


PCN1-S24-D5-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)

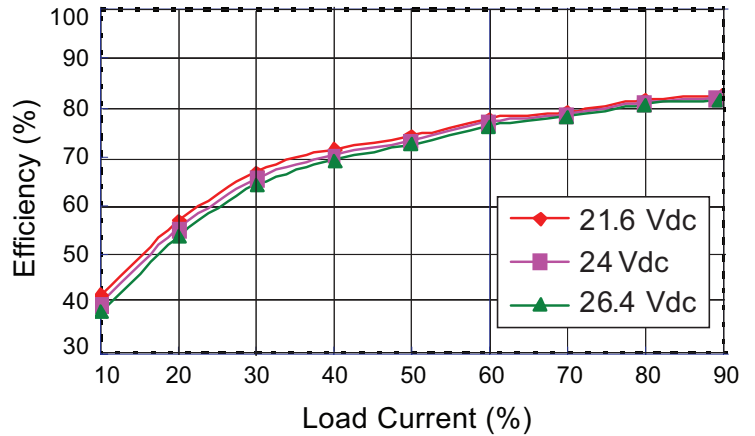


## EFFICIENCY CURVES (CONTINUED)

PCN1-S24-D12-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



PCN1-S24-D15-S Efficiency Curve  
(Efficiency vs. Line Voltage and Load Current)



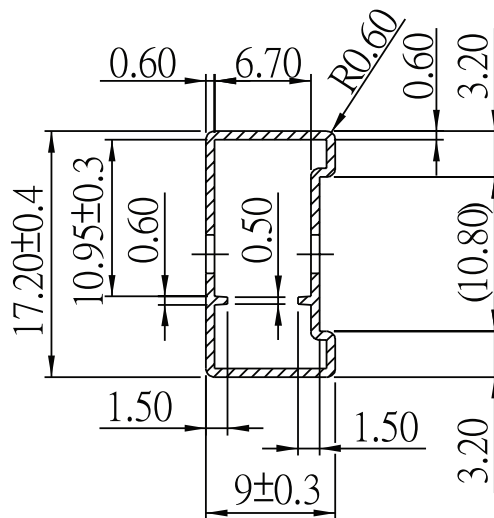
## PACKAGING

### 5, 12 Vdc input models

units: mm

Tube size: 17.2 x 9 x 340 mm

QTY: 16 pcs

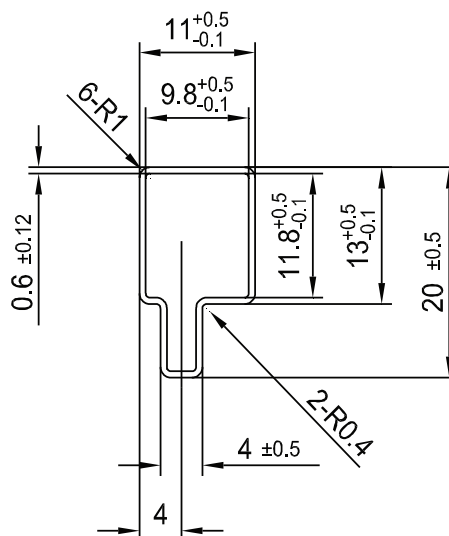


### 24 Vdc input models

units: mm

Tube size: 20 x 11 x 340 mm

QTY: 14 pcs

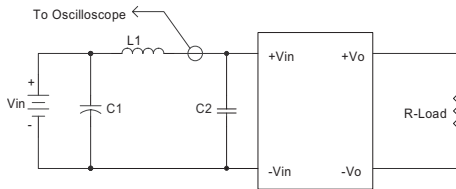




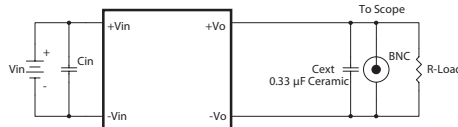
## TEST CONFIGURATIONS

### Input Ripple Current & Output Noise

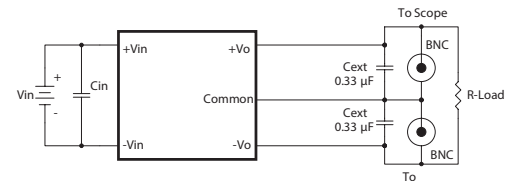
**Figure 1 Measuring Input Ripple Current**



**Figure 2 Measuring Output Ripple & Noise for Single Output Models**



**Figure 3 Measuring Output Ripple & Noise for Dual Output Models**



**Table 1**

L1	12 µH
C1	2.2 µF or 4.7 µF tantalum capacitor
C2	NC

**Table 2**

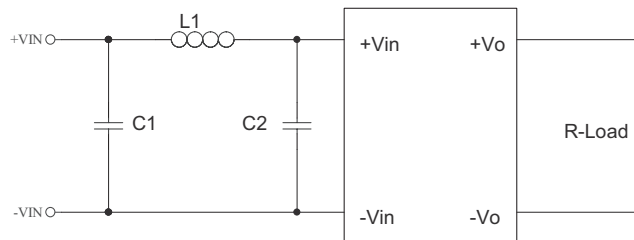
Input Voltage (Vdc)	Cin
5	2.2 µF ceramic capacitor
12	2.2 µF ceramic capacitor
24	4.7 µF ceramic capacitor

## EMC RECOMMENDED CIRCUIT

### Test Condition

Input Voltage: Nominal  
Output Load: Full Load

**Figure 4 Conducted Emissions Test Circuit**



**Table 3**

EN55022 Class B Recommended External Circuit Components			
Input Voltage (Vdc)	C1 <sup>1</sup>	C2 <sup>1</sup>	L1
5	4.7 µF / 25 V	4.7 µF / 25 V	10 µH
12	4.7 µF / 25 V	4.7 µF / 25 V	10 µH
24	10 µF / 50 V	10 µF / 50 V	7.5 µH

Notes: 1. Ceramic Capacitor

## REVISION HISTORY

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rev.	description	date
1.0	initial release	07/26/2016

The revision history provided is for informational purposes only and is believed to be accurate.



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