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PCU9955A

16-channel UFm 5 MHz I²C-bus 57 mA/20 V constant current LED driver

Rev. 3.1 — 29 June 2015 Product data sheet

1. General description

The PCU9955A is an Ultra Fast-mode (UFm) I²C-bus controlled 16-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 100 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCU9955A operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LED outputs allow up to 20 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

Gradation control for all current sources is achieved via the I²C-bus serial interface and allows user to ramp current automatically without MCU intervention. 8-bit DACs are available to adjust brightness levels for each LED current source. There are four selectable gradation control groups and each group has independently four registers to control ramp-up and ramp-down rate, step time, hold ON/OFF time and final hold ON output current. Two gradation operation modes are available for each group, one is single shot mode (output pattern once) and the other is continuous mode (output pattern repeat). Each channel can be set to either gradation mode or normal mode and assigned to any one of these four gradation control groups.

This device has built-in overtemperature detection circuitry. A thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCU9955A device is the first LED controller device in a new Ultra Fast-mode (UFm) I²C-bus family. UFm I²C-bus devices offer higher frequency (up to 5 MHz). The UFm I²C-bus slave devices operate in receive-only mode. That is, only I²C writes to the PCU9955A are supported. As such, there are no status registers in PCU9955A. The PCU9955A allows significantly higher data transfer rate compared to the Fast-mode Plus version (PCA9955A).

The active LOW output enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices must be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCU9955A devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. On power-up, PCU9955A has a unique Sub Call address to identify it as a 16-channel LED driver. This allows mixing of devices with different channel widths. Three hardware address pins on PCU9955A allow up to 125 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCU9955A through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features and benefits

- 16 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LED output delay to reduce EMI and surge currents
- Gradation control for all channels
  - Each channel can assign to one of four gradation control groups
  - Programmable gradation time and rate for ramp-up and/or ramp-down operations
  - Programmable step time (6-bit) from 0.5 ms (minimum) to 512 ms (maximum)
  - Programmable hold-on time after ramp-up and hold-off time after ramp-down (3-bit) from 0 s to 6 s
  - Programmable final ramp-up and hold-on current
  - Programmable brightness current output adjustment, either linear or exponential curve
- 16 constant current output channels can sink up to 57 mA, tolerate up to 20 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ±4 % between output channels
  - ±6 % between PCU9955A devices
- Thermal shutdown for overtemperature
- 5 MHz Ultra Fast-mode I²C-bus interface
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness fully ON using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %

- Output state change programmable on the Acknowledge (bit 9, this bit is always set to 1 by I²C-bus master) or the STOP condition to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- Three quinary hardware address pins allow 125 PCU9955A devices to be connected to the same I²C-bus and to be individually programmed
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCU9955As on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that $^1/_3$ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I²C-bus address.
- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on USDA/USCL inputs
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +85 °C operation
- ESD protection exceeds 4000 V HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: HTSSOP28

3. Applications

- Amusement products
- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices
- Fade-in and fade-out for breathlight control

4. Ordering information

Table 1. Ordering information

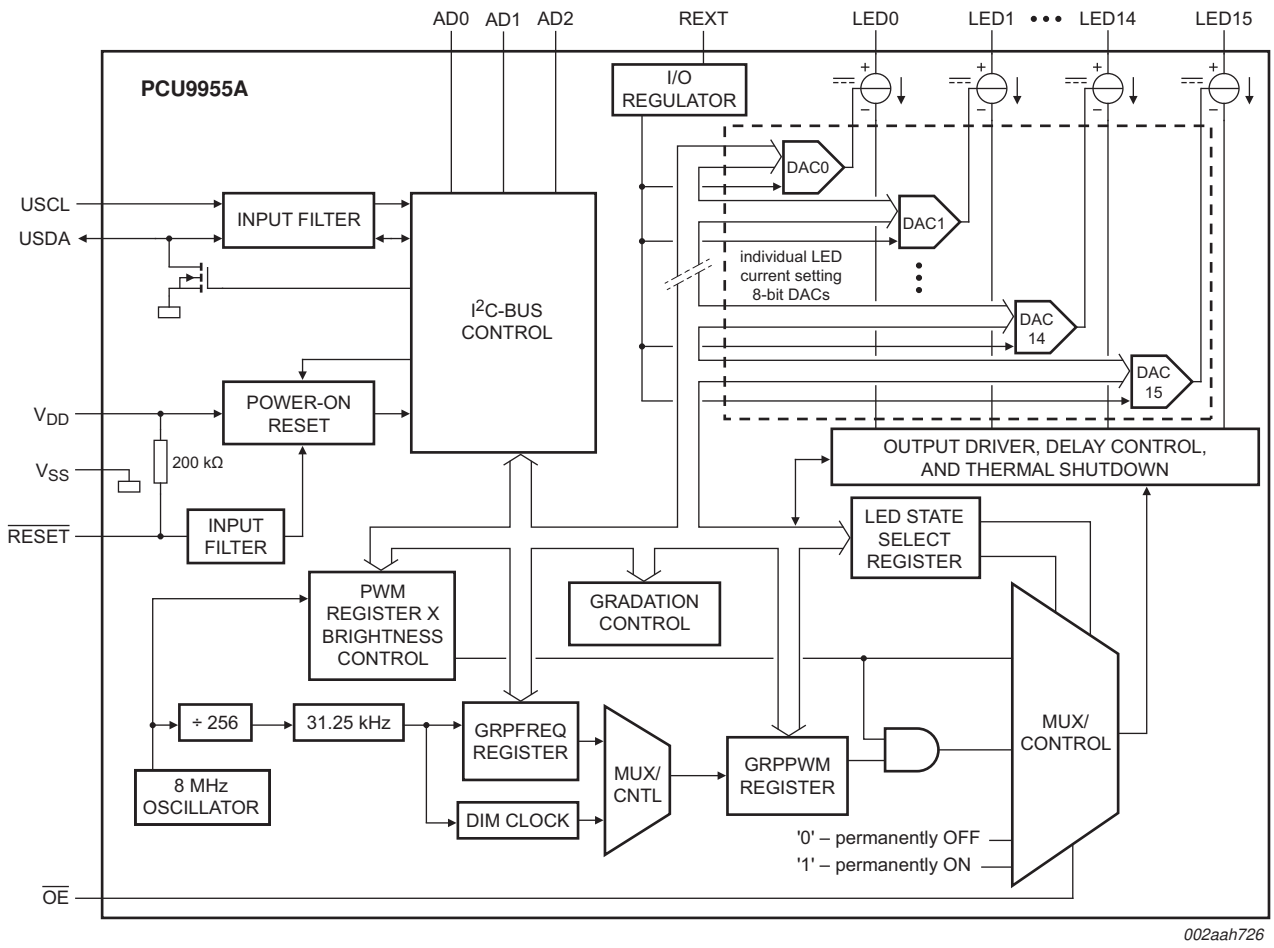
Type number	Topside mark	Package		
		Name	Description	Version
PCU9955ATW	PCU9955ATW	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-3

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCU9955ATW	PCU9955ATWJ	HTSSOP28	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

5. Block diagram



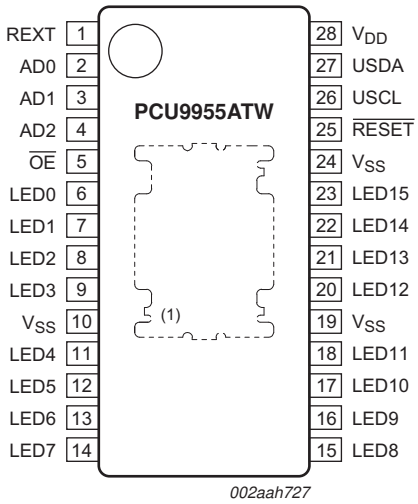
Dim repetition rate = 122 Hz.

Blink repetition rate = 15 Hz to every 16.8 seconds.

Fig 1. Block diagram of PCU9955A

6. Pinning information

6.1 Pinning



(1) Thermal pad; connected to V_{SS}.

Fig 2. Pin configuration for HTSSOP28

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
AD0	2	I	address input 0
AD1	3	I	address input 1
AD2	4	I	address input 2
$\overline{OE}$	5	I	active LOW output enable for LEDs
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	11	O	LED driver 4
LED5	12	O	LED driver 5
LED6	13	O	LED driver 6
LED7	14	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	20	O	LED driver 12

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
LED13	21	O	LED driver 13
LED14	22	O	LED driver 14
LED15	23	O	LED driver 15
$\overline{\text{RESET}}$	25	I	active LOW reset input
USCL	26	I	UFm serial clock line
USDA	27	I/O	UFm serial data line
V_{SS}	10, 19, 24 [1]	ground	supply ground
V_{DD}	28	power supply	supply voltage

[1] HTSSOP28 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCU9955A”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCU9955A there are a maximum of 125 possible programmable addresses using the three quinary hardware address pins.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCU9955A is shown in Figure 3. The 7-bit slave address is determined by the quinary input pads AD0, AD1 and AD2. Each pad can have one of five states (GND, pull-up, floating, pull-down, and V_{DD}) based on how the input pad is connected on the board. At power-up or hardware/software reset, the quinary input pads are sampled and set the slave address of the device internally. To conserve power, once the slave address is determined, the quinary input pads are turned off and will not be sampled until the next time the device is power cycled. Table 4 lists the five possible connections for the quinary input pads along with the external resistor values that must be used.

Table 4. Quinary input pad connection

Pad connection (pins AD2, AD1, AD0)[1]	Mnemonic	External resistor (kΩ)	
		Min.	Max.
tie to ground	GND	0	17.9
resistor pull-down to ground	PD	34.8	270
open (floating)	FLT	503	∞
resistor pull-up to V_{DD}	PU	31.7	340
tie to V_{DD}	V_{DD}	0	22.1

[1] These AD[2:0] inputs must be stable before the supply V_{DD} to the chip.

Table 5 lists all 125 possible slave addresses of the device based on all combinations of the five states connected to three address input pins AD0, AD1 and AD2.

Table 5. I²C-bus slave address

Hardware selectable input pins			I²C-bus slave address for PCU9955A			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
GND	GND	GND	1	01	0000001[1]	02h
GND	GND	PD	2	02	0000010[1]	04h
GND	GND	FLT	3	03	0000011[1]	06h
GND	GND	PU	4	04	0000100[1]	08h
GND	GND	V_{DD}	5	05	0000101[1]	0Ah
GND	PD	GND	6	06	0000110[1]	0Ch
GND	PD	PD	7	07	0000111[1]	0Eh
GND	PD	FLT	8	08	0001000	10h
GND	PD	PU	9	09	0001001	12h
GND	PD	V_{DD}	10	0A	0001010	14h
GND	FLT	GND	11	0B	0001011	16h
GND	FLT	PD	12	0C	0001100	18h
GND	FLT	FLT	13	0D	0001101	1Ah
GND	FLT	PU	14	0E	0001110	1Ch
GND	FLT	V_{DD}	15	0F	0001111	1Eh
GND	PU	GND	16	10	0010000	20h
GND	PU	PD	17	11	0010001	22h
GND	PU	FLT	18	12	0010010	24h
GND	PU	PU	19	13	0010011	26h
GND	PU	V_{DD}	20	14	0010100	28h
GND	V_{DD}	GND	21	15	0010101	2Ah
GND	V_{DD}	PD	22	16	0010110	2Ch
GND	V_{DD}	FLT	23	17	0010111	2Eh
GND	V_{DD}	PU	24	18	0011000	30h
GND	V_{DD}	V_{DD}	25	19	0011001	32h
PD	GND	GND	26	1A	0011010	34h
PD	GND	PD	27	1B	0011011	36h
PD	GND	FLT	28	1C	0011100	38h
PD	GND	PU	29	1D	0011101	3Ah
PD	GND	V_{DD}	30	1E	0011110	3Ch
PD	PD	GND	31	1F	0011111	3Eh
PD	PD	PD	32	20	0100000	40h
PD	PD	FLT	33	21	0100001	42h
PD	PD	PU	34	22	0100010	44h
PD	PD	V_{DD}	35	23	0100011	46h
PD	FLT	GND	36	24	0100100	48h
PD	FLT	PD	37	25	0100101	4Ah
PD	FLT	FLT	38	26	0100110	4Ch

Table 5. I²C-bus slave address *…continued*

Hardware selectable input pins			I²C-bus slave address for PCU9955A			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
PD	FLT	PU	39	27	0100111	4Eh
PD	FLT	V_{DD}	40	28	0101000	50h
PD	PU	GND	41	29	0101001	52h
PD	PU	PD	42	2A	0101010	54h
PD	PU	FLT	43	2B	0101011	56h
PD	PU	PU	44	2C	0101100	58h
PD	PU	V_{DD}	45	2D	0101101	5Ah
PD	V_{DD}	GND	46	2E	0101110	5Ch
PD	V_{DD}	PD	47	2F	0101111	5Eh
PD	V_{DD}	FLT	48	30	0110000	60h
PD	V_{DD}	PU	49	31	0110001	62h
PD	V_{DD}	V_{DD}	50	32	0110010	64h
FLT	GND	GND	51	33	0110011	66h
FLT	GND	PD	52	34	0110100	68h
FLT	GND	FLT	53	35	0110101	6Ah
FLT	GND	PU	54	36	0110110	6Ch
FLT	GND	V_{DD}	55	37	0110111	6Eh
FLT	PD	GND	56	38	0111000	70h
FLT	PD	PD	57	39	0111001	72h
FLT	PD	FLT	58	3A	0111010	74h
FLT	PD	PU	59	3B	0111011	76h
FLT	PD	V_{DD}	60	3C	0111100	78h
FLT	FLT	GND	61	3D	0111101	7Ah
FLT	FLT	PD	62	3E	0111110	7Ch
FLT	FLT	FLT	63	3F	0111111	7Eh
FLT	FLT	PU	64	40	1000000	80h
FLT	FLT	V_{DD}	65	41	1000001	82h
FLT	PU	GND	66	42	1000010	84h
FLT	PU	PD	67	43	1000011	86h
FLT	PU	FLT	68	44	1000100	88h
FLT	PU	PU	69	45	1000101	8Ah
FLT	PU	V_{DD}	70	46	1000110	8Ch
FLT	V_{DD}	GND	71	47	1000111	8Eh
FLT	V_{DD}	PD	72	48	1001000	90h
FLT	V_{DD}	FLT	73	49	1001001	92h
FLT	V_{DD}	PU	74	4A	1001010	94h
FLT	V_{DD}	V_{DD}	75	4B	1001011	96h
PU	GND	GND	76	4C	1001100	98h
PU	GND	PD	77	4D	1001101	9Ah
PU	GND	FLT	78	4E	1001110	9Ch

Table 5. I²C-bus slave address *…continued*

Hardware selectable input pins			I²C-bus slave address for PCU9955A			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
PU	GND	PU	79	4F	1001111	9Eh
PU	GND	V_{DD}	80	50	1010000	A0h
PU	PD	GND	81	51	1010001	A2h
PU	PD	PD	82	52	1010010	A4h
PU	PD	FLT	83	53	1010011	A6h
PU	PD	PU	84	54	1010100	A8h
PU	PD	V_{DD}	85	55	1010101	AAh
PU	FLT	GND	86	56	1010110	ACh
PU	FLT	PD	87	57	1010111	AEh
PU	FLT	FLT	88	58	1011000	B0h
PU	FLT	PU	89	59	1011001	B2h
PU	FLT	V_{DD}	90	5A	1011010	B4h
PU	PU	GND	91	5B	1011011	B6h
PU	PU	PD	92	5C	1011100	B8h
PU	PU	FLT	93	5D	1011101	BAh
PU	PU	PU	94	5E	1011110	BCh
PU	PU	V_{DD}	95	5F	1011111	BEh
PU	V_{DD}	GND	96	60	1100000	C0h
PU	V_{DD}	PD	97	61	1100001	C2h
PU	V_{DD}	FLT	98	62	1100010	C4h
PU	V_{DD}	PU	99	63	1100011	C6h
PU	V_{DD}	V_{DD}	100	64	1100100	C8h
V_{DD}	GND	GND	101	65	1100101	CAh
V_{DD}	GND	PD	102	66	1100110	CCh
V_{DD}	GND	FLT	103	67	1100111	CEh
V_{DD}	GND	PU	104	68	1101000	D0h
V_{DD}	GND	V_{DD}	105	69	1101001	D2h
V_{DD}	PD	GND	106	6A	1101010	D4h
V_{DD}	PD	PD	107	6B	1101011	D6h
V_{DD}	PD	FLT	108	6C	1101100	D8h
V_{DD}	PD	PU	109	6D	1101101	DAh
V_{DD}	PD	V_{DD}	110	6E	1101110	DCh
V_{DD}	FLT	GND	111	6F	1101111	DEh
V_{DD}	FLT	PD	112	70	1110000	E0h
V_{DD}	FLT	FLT	113	71	1110001	E2h
V_{DD}	FLT	PU	114	72	1110010	E4h
V_{DD}	FLT	V_{DD}	115	73	1110011	E6h
V_{DD}	PU	GND	116	74	1110100	E8h
V_{DD}	PU	PD	117	75	1110101	EAh
V_{DD}	PU	FLT	118	76	1110110	ECh

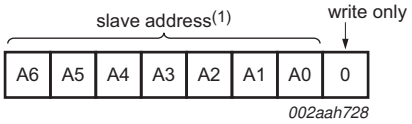
Table 5. I²C-bus slave address *...continued*

Hardware selectable input pins			I²C-bus slave address for PCU9955A			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
V_{DD}	PU	PU	119	77	1110111	EEh
V_{DD}	PU	V_{DD}	120	78	1111000[1]	F0h
V_{DD}	V_{DD}	GND	121	79	1111001[1]	F2h
V_{DD}	V_{DD}	PD	122	7A	1111010[1]	F4h
V_{DD}	V_{DD}	FLT	123	7B	1111011[1]	F6h
V_{DD}	V_{DD}	PU	124	7C	1111100[1]	F8h
V_{DD}	V_{DD}	V_{DD}	125	7D	1111101[1]	FAh

[1] See 'Remark' below.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- 'reserved for future use' I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)



(1) This slave address must match one of the 125 internal addresses as shown in Table 5.

Fig 3. PCU9955A slave address

The last bit of the address byte defines the operation to be performed. Only writes to PCU9955A are supported, therefore the last bit is set to 0. No read available with UFm I²C-bus.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled

See Section 7.3.11 "ALLCALLADR, LED All Call I²C-bus address" for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000X) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All of the PCU9955As on the I²C-bus recognize the address if sent by the I²C-bus master.

7.1.3 LED Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: ECh or 1110 110X
  - SUBADR2 register: ECh or 1110 110X
  - SUBADR3 register: ECh or 1110 110X
- Programmable through I²C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I²C-bus addresses are disabled.

Remark: At power-up SUBADR1 identifies this device as a 16-channel driver.

See Section 7.3.10 “LED Sub Call I²C-bus addresses for PCU9955A” for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.2 Control register

Following the slave address, LED All Call address or LED Sub Call address, the bus master sends a byte to the PCU9955A, which is stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register is accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF).

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.

reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 4. Control register

When the Auto-Increment Flag is set (AIF = logic 1), the seven low-order bits of the Control register are automatically incremented after a write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

Table 6. Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for registers (00h to 43h). D[6:0] roll over to 00h after the last register 43h is accessed.
1	0	1	Auto-Increment for individual brightness registers only (08h to 17h). D[6:0] roll over to 08h after the last register (17h) is accessed.
1	1	0	Auto-Increment for MODE1 to IREF15 control registers (00h to 27h). D[6:0] roll over to 00h after the last register (27h) is accessed.
1	1	1	Auto-Increment for global control registers and individual brightness registers (06h to 17h). D[6:0] roll over to 06h after the last register (17h) is accessed.

[1] AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 6 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 16 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF15 registers must be programmed with different settings during the same I²C-bus communication.

AIF + AI[1:0] = 111b is used when the 16 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that is addressed (write operation), and can be anywhere between 00h and 49h (as defined in Table 7). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See Table 6 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence is (in hexadecimal):
10 → 11 → … → 17 → 08 → 09 → … → 17 → 08 → 09 → … as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1010 0010, then the register addressing sequence is (in hexadecimal):
22 → 23 → … → 43 → 00 → 01 → … → 17 → 08 → 09 → … as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence is (in hexadecimal):
05 → 06 → … → 17 → 08 → 09 → … → 17 → 08 → 09 → … as long as the master keeps sending data.

Remark: Writing to registers marked 'not used' are ignored.

7.3 Register definitions

Table 7. Register summary

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	write only	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	write only	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	write only	LED output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	write only	LED output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	write only	LED output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	write only	LED output state 3
06h	0	0	0	0	1	1	0	GRPPWM	write only	group duty cycle control
07h	0	0	0	0	1	1	1	GRPFREQ	write only	group frequency
08h	0	0	0	1	0	0	0	PWM0	write only	brightness control LED0
09h	0	0	0	1	0	0	1	PWM1	write only	brightness control LED1
0Ah	0	0	0	1	0	1	0	PWM2	write only	brightness control LED2
0Bh	0	0	0	1	0	1	1	PWM3	write only	brightness control LED3
0Ch	0	0	0	1	1	0	0	PWM4	write only	brightness control LED4
0Dh	0	0	0	1	1	0	1	PWM5	write only	brightness control LED5
0Eh	0	0	0	1	1	1	0	PWM6	write only	brightness control LED6
0Fh	0	0	0	1	1	1	1	PWM7	write only	brightness control LED7
10h	0	0	1	0	0	0	0	PWM8	write only	brightness control LED8
11h	0	0	1	0	0	0	1	PWM9	write only	brightness control LED9
12h	0	0	1	0	0	1	0	PWM10	write only	brightness control LED10
13h	0	0	1	0	0	1	1	PWM11	write only	brightness control LED11
14h	0	0	1	0	1	0	0	PWM12	write only	brightness control LED12
15h	0	0	1	0	1	0	1	PWM13	write only	brightness control LED13
16h	0	0	1	0	1	1	0	PWM14	write only	brightness control LED14
17h	0	0	1	0	1	1	1	PWM15	write only	brightness control LED15
18h	0	0	1	1	0	0	0	IREF0	write only	output gain control register 0
19h	0	0	1	1	0	0	1	IREF1	write only	output gain control register 1
1Ah	0	0	1	1	0	1	0	IREF2	write only	output gain control register 2
1Bh	0	0	1	1	0	1	1	IREF3	write only	output gain control register 3
1Ch	0	0	1	1	1	0	0	IREF4	write only	output gain control register 4
1Dh	0	0	1	1	1	0	1	IREF5	write only	output gain control register 5
1Eh	0	0	1	1	1	1	0	IREF6	write only	output gain control register 6
1Fh	0	0	1	1	1	1	1	IREF7	write only	output gain control register 7

Table 7. Register summary *…continued*

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
20h	0	1	0	0	0	0	0	IREF8	write only	output gain control register 8
21h	0	1	0	0	0	0	1	IREF9	write only	output gain control register 9
22h	0	1	0	0	0	1	0	IREF10	write only	output gain control register 10
23h	0	1	0	0	0	1	1	IREF11	write only	output gain control register 11
24h	0	1	0	0	1	0	0	IREF12	write only	output gain control register 12
25h	0	1	0	0	1	0	1	IREF13	write only	output gain control register 13
26h	0	1	0	0	1	1	0	IREF14	write only	output gain control register 14
27h	0	1	0	0	1	1	1	IREF15	write only	output gain control register 15
28h	0	1	0	1	0	0	0	RAMP_RATE_GRP0	write only	ramp enable and rate control for group 0
29h	0	1	0	1	0	0	1	STEP_TIME_GRP0	write only	step time control for group 0
2Ah	0	1	0	1	0	1	0	HOLD_CNTL_GRP0	write only	hold ON/OFF time control for group 0
2Bh	0	1	0	1	0	1	1	IREF_GRP0	write only	output gain control for group 0
2Ch	0	1	0	1	1	0	0	RAMP_RATE_GRP1	write only	ramp enable and rate control for group 1
2Dh	0	1	0	1	1	0	1	STEP_TIME_GRP1	write only	step time control for group 1
2Eh	0	1	0	1	1	1	0	HOLD_CNTL_GRP1	write only	hold ON/OFF time control for group 1
2Fh	0	1	0	1	1	1	1	IREF_GRP1	write only	output gain control for group 1
30h	0	1	1	0	0	0	0	RAMP_RATE_GRP2	write only	ramp enable and rate control for group 2
31h	0	1	1	0	0	0	1	STEP_TIME_GRP2	write only	step time control for group 2
32h	0	1	1	0	0	1	0	HOLD_CNTL_GRP2	write only	hold ON/OFF time control for group 2
33h	0	1	1	0	0	1	1	IREF_GRP2	write only	output gain control for group 2
34h	0	1	1	0	1	0	0	RAMP_RATE_GRP3	write only	ramp enable and rate control for group 3
35h	0	1	1	0	1	0	1	STEP_TIME_GRP3	write only	step time control for group 3
36h	0	1	1	0	1	1	0	HOLD_CNTL_GRP3	write only	hold ON/OFF time control for group 3
37h	0	1	1	0	1	1	1	IREF_GRP3	write only	output gain control for group 3
38h	0	1	1	1	0	0	0	GRAD_MODE_SEL0	write only	gradation mode select register for channel 7 to channel 0
39h	0	1	1	1	0	0	1	GRAD_MODE_SEL1	write only	gradation mode select register for channel 15 to channel 8
3Ah	0	1	1	1	0	1	0	GRAD_GRP_SEL0	write only	gradation group select for channel 3 to channel 0
3Bh	0	1	1	1	0	1	1	GRAD_GRP_SEL1	write only	gradation group select for channel 7 to channel 4
3Ch	0	1	1	1	1	0	0	GRAD_GRP_SEL2	write only	gradation group select for channel 11 to channel 8

Table 7. Register summary *…continued*

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
3Dh	0	1	1	1	1	0	1	GRAD_GRP_SEL3	write only	gradation group select for channel 15 to channel 12
3Eh	0	1	1	1	1	1	0	GRAD_CNTL	write only	gradation control register for all four groups
3Fh	0	1	1	1	1	1	1	OFFSET	write only	Offset/delay on LEDn outputs
40h	1	0	0	0	0	0	0	SUBADR1	write only	I²C-bus subaddress 1
41h	1	0	0	0	0	0	1	SUBADR2	write only	I²C-bus subaddress 2
42h	1	0	0	0	0	1	0	SUBADR3	write only	I²C-bus subaddress 3
43h	1	0	0	0	0	1	1	ALLCALLADR	write only	All Call I²C-bus address
44h	1	0	0	0	1	0	0	PWMALL	write only	brightness control for all LEDn
45h	1	0	0	0	1	0	1	IREFALL	write only	output gain control for all registers IREF0 to IREF15
46h to 7Fh	-	-	-	-	-	-	-	reserved	write only	not used[1]

[1] Writing to reserved registers are ignored.

7.3.1 MODE1 — Mode register 1

Table 8. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AIF	W only	-	Not used.
6	AI1	W only	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 6.
5	AI0	W only	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 6.
4	SLEEP	W only	0*	Normal mode[1].
			1	Low-power mode. Oscillator off[2][3].
3	SUB1	W only	0	PCU9955A does not respond to I²C-bus subaddress 1.
			1*	PCU9955A responds to I²C-bus subaddress 1.
2	SUB2	W only	0*	PCU9955A does not respond to I²C-bus subaddress 2.
			1	PCU9955A responds to I²C-bus subaddress 2.
1	SUB3	W only	0*	PCU9955A does not respond to I²C-bus subaddress 3.
			1	PCU9955A responds to I²C-bus subaddress 3.
0	ALLCALL	W only	0	PCU9955A does not respond to LED All Call I²C-bus address.
			1*	PCU9955A responds to LED All Call I²C-bus address.

[1] It takes 500 µs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 µs window.

[2] No blinking, dimming or gradation control is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.3.2 MODE2 — Mode register 2

Table 9. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	-	-	not used (must write a logic 0)
6	-	-	-	not used (must write a logic 0)
5	DMBLNK	W only	0*	group control = dimming
			1	group control = blinking
4	-	-	-	not used (must write a logic 0)
3	OCH	W only	0*	outputs change on STOP condition
			1	outputs change on ACK, this ninth bit is always set to 1 by UFm I²C-bus master.
2	EXP_EN	W only	0*	linear adjustment for gradation control
			1	exponential adjustment for gradation control
1	-	-	0*	reserved (must write a logic 0)
0	-	-	1*	reserved (must write a logic 1)

Brightness adjustment for gradation control is either linear or exponential by setting the EXP_EN bit as shown in Figure 5. When EXP_EN = 0, linear adjustment scale is used. When EXP_EN = 1, exponential scale is used.

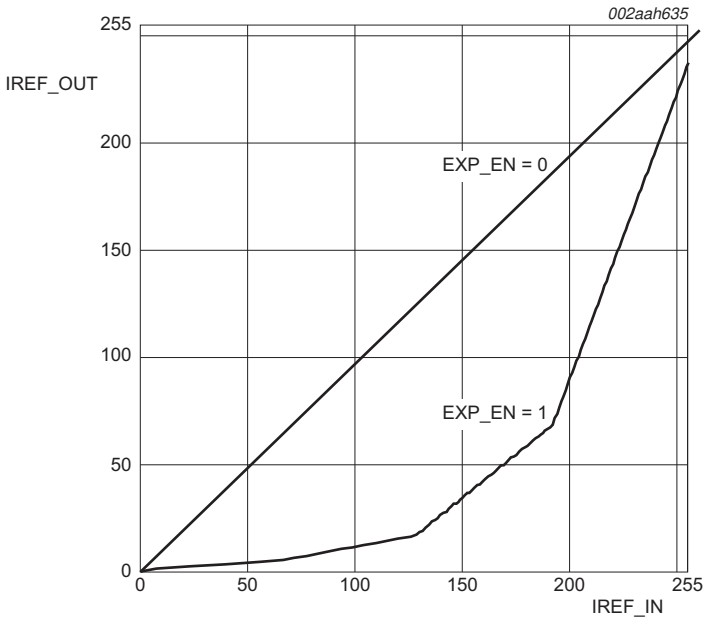


Fig 5. Linear and exponential adjustment curves

7.3.3 LEDOUT0 to LEDOUT3, LED driver output state

Table 10. LEDOUT0 to LEDOUT3 - LED driver output state registers (address 02h to 05h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	W only	10*	LED3 output state control
		5:4	LDR2	W only	10*	LED2 output state control
		3:2	LDR1	W only	10*	LED1 output state control
		1:0	LDR0	W only	10*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	W only	10*	LED7 output state control
		5:4	LDR6	W only	10*	LED6 output state control
		3:2	LDR5	W only	10*	LED5 output state control
		1:0	LDR4	W only	10*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	W only	10*	LED11 output state control
		5:4	LDR10	W only	10*	LED10 output state control
		3:2	LDR9	W only	10*	LED9 output state control
		1:0	LDR8	W only	10*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	W only	10*	LED15 output state control
		5:4	LDR14	W only	10*	LED14 output state control
		3:2	LDR13	W only	10*	LED13 output state control
		1:0	LDR12	W only	10*	LED12 output state control

LDRx = 00 — LED driver x is off (x = 0 to 15).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The $\overline{OE}$ pin can be used as external dimming/blinking control in this state.

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register (default power-up state) or PWMALL register for all LEDn outputs.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

7.3.4 GRPPWM, group duty cycle control

Table 11. GRPPWM - Group brightness control register (address 06h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
06h	GRPPWM	7:0	GDC[7:0]	W only	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 16 outputs is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.3.5 GRPFREQ, group frequency

Table 12. GRPFREQ - Group frequency register (address 07h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
07h	GRPFREQ	7:0	GFRQ[7:0]	W only	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a ‘Don’t care’ when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{15.26}(s) \quad (2)$$

7.3.6 PWM0 to PWM15, individual brightness control

Table 13. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	PWM0	7:0	IDC0[7:0]	W only	0000 0000*	PWM0 Individual Duty Cycle
09h	PWM1	7:0	IDC1[7:0]	W only	0000 0000*	PWM1 Individual Duty Cycle
0Ah	PWM2	7:0	IDC2[7:0]	W only	0000 0000*	PWM2 Individual Duty Cycle
0Bh	PWM3	7:0	IDC3[7:0]	W only	0000 0000*	PWM3 Individual Duty Cycle
0Ch	PWM4	7:0	IDC4[7:0]	W only	0000 0000*	PWM4 Individual Duty Cycle
0Dh	PWM5	7:0	IDC5[7:0]	W only	0000 0000*	PWM5 Individual Duty Cycle
0Eh	PWM6	7:0	IDC6[7:0]	W only	0000 0000*	PWM6 Individual Duty Cycle
0Fh	PWM7	7:0	IDC7[7:0]	W only	0000 0000*	PWM7 Individual Duty Cycle
10h	PWM8	7:0	IDC8[7:0]	W only	0000 0000*	PWM8 Individual Duty Cycle
11h	PWM9	7:0	IDC9[7:0]	W only	0000 0000*	PWM9 Individual Duty Cycle
12h	PWM10	7:0	IDC10[7:0]	W only	0000 0000*	PWM10 Individual Duty Cycle
13h	PWM11	7:0	IDC11[7:0]	W only	0000 0000*	PWM11 Individual Duty Cycle
14h	PWM12	7:0	IDC12[7:0]	W only	0000 0000*	PWM12 Individual Duty Cycle

Table 13. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description
…continued

Address	Register	Bit	Symbol	Access	Value	Description
15h	PWM13	7:0	IDC13[7:0]	W only	0000 0000*	PWM13 Individual Duty Cycle
16h	PWM14	7:0	IDC14[7:0]	W only	0000 0000*	PWM14 Individual Duty Cycle
17h	PWM15	7:0	IDC15[7:0]	W only	0000 0000*	PWM15 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FEh (99.2 % duty cycle = LED output at maximum brightness) and FFh (100 % duty cycle = LED output completed ON). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM do not have effective brightness control of LEDs due to edge rate control of LED output pins.

7.3.7 IREF0 to IREF15, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED15.

Table 14. IREF0 to IREF15 - LED output gain control registers (address 18h to 27h) bit description
*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
18h	IREF0	7:0	W only	00h*	LED0 output current setting
19h	IREF1	7:0	W only	00h*	LED1 output current setting
1Ah	IREF2	7:0	W only	00h*	LED2 output current setting
1Bh	IREF3	7:0	W only	00h*	LED3 output current setting
1Ch	IREF4	7:0	W only	00h*	LED4 output current setting
1Dh	IREF5	7:0	W only	00h*	LED5 output current setting
1Eh	IREF6	7:0	W only	00h*	LED6 output current setting
1Fh	IREF7	7:0	W only	00h*	LED7 output current setting
20h	IREF8	7:0	W only	00h*	LED8 output current setting
21h	IREF9	7:0	W only	00h*	LED9 output current setting
22h	IREF10	7:0	W only	00h*	LED10 output current setting
23h	IREF11	7:0	W only	00h*	LED11 output current setting
24h	IREF12	7:0	W only	00h*	LED12 output current setting
25h	IREF13	7:0	W only	00h*	LED13 output current setting
26h	IREF14	7:0	W only	00h*	LED14 output current setting
27h	IREF15	7:0	W only	00h*	LED15 output current setting

7.3.8 Gradation control

Gradation control is designed to use four independent groups of registers to program the full cycle of the gradation timing to implement on each selected channel. Each group has four registers to define the ramp rate, step time, hold ON/OFF time, and final hold ON current, as shown in Figure 6.

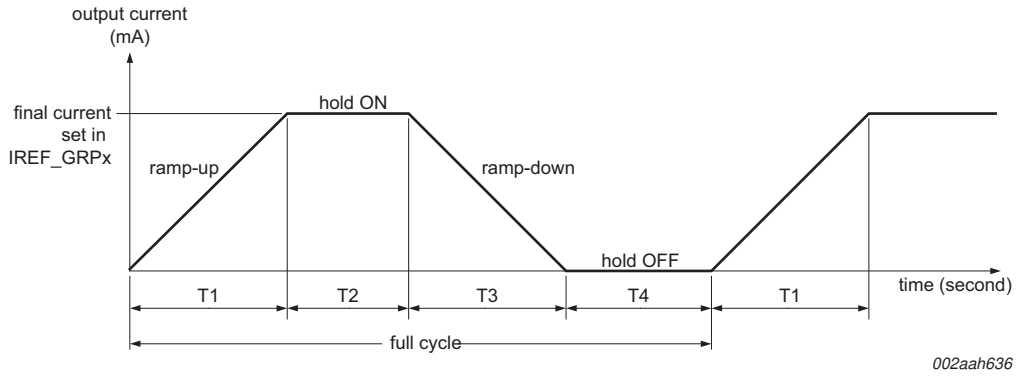


Fig 6. Gradation timing

- The 'final' and 'hold ON' current is defined in IREF_GRPx register value × (225 μA if REXT = 1 kΩ, or 112.5 μA if REXT = 2 kΩ).
- Ramp rate value and enable/disable ramp operation is defined in RAMP_RATE_GRPx register.
- Total number of ramp steps (or level changes) is calculated as 'IREF_GRPx value' ÷ 'ramp rate value in RAMP_RATE_GRPx'. If the total number is not an integer, the number is rounded up to the next integer.
- Time for each step is calculated as 'cycle time' × 'multiple factor' bits in STEP_TIME_GRPx register. Minimum time for one step is 0.5 ms (0.5 ms × 1) and maximum time is 512 ms (8 ms × 64).
- The ramp-up or ramp-down time (T1 or T3) is calculated as '(total steps + 1)' × 'step time'.
- Hold ON or OFF time (T2 or T4) is defined in HOLD_CNTL_GRPx register in the range of 0/0.25/0.5/0.75/1/2/4/6 seconds.
- Gradation start or stop with single shot mode (one full cycle only) or continuous mode (repeat full cycle) is defined in the GRAD_CNTL register for all groups.
- Each channel can be assigned to one of these four groups in the GRAD_GRP_SELx register.
- Each channel can set either normal mode or gradation mode operation in the GRAD_MODE_SELx register.

To enable the gradation operation, the following steps are required:

1. Program all gradation control registers except the gradation start bit in GRAD_CNTL register.
2. Program either LDRx = 01 (LED fully ON mode) only, or LDRx = 10 or 11 (PWM control mode) with individual brightness control PWMx register for duty cycle.
3. Program output current value IREFx register to non-zero, which enables LED output.

4. Set the gradation start bit in GRAD_CNTL register for enabling gradation operation.

7.3.8.1 RAMP_RATE_GRP0 to RAMP_RATE_GRP3, ramp rate control registers

Table 15. RAMP_RATE_GRP[0:3] - Ramp enable and rate control registers (address 28h, 2Ch, 30h, 34h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
28h	RAMP_RATE_GRP0	7	W only	0*	Ramp-up disable
2Ch	RAMP_RATE_GRP1			1	Ramp-up enable
30h	RAMP_RATE_GRP2	6	W only	0*	Ramp-down disable
34h	RAMP_RATE_GRP3			1	Ramp-down enable
		5:0	W only	0x00*	Ramp rate value per step is defined from 1 (00h) to 64 (3Fh)[1][2]

[1] Total number of ramp steps is defined as 'IREF_GRP[7:0]' ÷ 'ramp_rate[5:0]'. (Round up to next integer if it is not an integer number.)

[2] Per step current increment or decrement is calculated by the (ramp_rate × I_{ref}), where the I_{ref} reference current is 112.5 μA (REXT = 2 kΩ) or 225 μA (REXT = 1 kΩ).

7.3.8.2 STEP_TIME_GRP0 to STEP_TIME_GRP3, step time control registers

Table 16. STEP_TIME_GRP[0:3] - Step time control registers (address 29h, 2Dh, 31h, 35h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
29h	STEP_TIME_GRP0	7	W only	0*	reserved (must write a logic 0)
2Dh	STEP_TIME_GRP1	6	W only	0*	Cycle time is set to 0.5 ms
31h	STEP_TIME_GRP2			1	Cycle time is set to 8 ms
35h	STEP_TIME_GRP3	5:0	W only	0x00*	Multiple factor per step, the multiple factor is defined from 1 (00h) to 64 (3Fh)[1]

[1] Step time = cycle time (0.5 ms or 8 ms) × multiple factor (1 ~ 64); minimum step time is 0.5 ms and maximum step time is 512 ms.

7.3.8.3 HOLD_CNTL_GRP0 to HOLD_CNTL_GRP3, hold ON and OFF control registers

Table 17. HOLD_CNTL_GRP[0:3] - Hold ON and OFF enable and time control registers (address 2Ah, 2Eh, 32h, 36h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Ah 2Eh 32h 36h	HOLD_CNTL_GRP0 HOLD_CNTL_GRP1 HOLD_CNTL_GRP2 HOLD_CNTL_GRP3	7	W only	0*	Hold ON disable
				1	Hold ON enable
		6	W only	0*	Hold OFF disable
				1	Hold OFF enable
		5:3	W only	000*	Hold ON time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s
		2:0	W only	000*	Hold OFF time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s

[1] Hold ON or OFF minimum time is 0 s and maximum time is 6 s.

7.3.8.4 IREF_GRP0 to IREF_GRP3, output gain control

Table 18. IREF_GRP[0:3] - Final and hold ON output gain setting registers (address 2Bh, 2Fh, 33h, 37h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Bh 2Fh 33h 37h	IREF_GRP0 IREF_GRP1 IREF_GRP2 IREF_GRP3	7:0	W only	00h*	Final ramp-up and hold ON output current gain setting[1]

[1] Output current = I_{ref} × IREF_GRPx[7:0], where I_{ref} is reference current. If REXT = 2 kΩ, then I_{ref} = 112.5 μA, or if REXT = 1 kΩ, then I_{ref} = 225 μA.

7.3.8.5 GRAD_MODE_SEL0 to GRAD_MODE_SEL1, gradation mode select registers

Table 19. GRAD_MODE_SEL[0:1] - Gradation mode select register for channel 15 to channel 0 (address 38h, 39h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1][2]
38h	GRAD_MODE_SEL0	7:0	W only	00*	Normal operation mode for channel 7 to channel 0
				FFh	Gradation operation mode for channel 7 to channel 0
39h	GRAD_MODE_SEL1	7:0	W only	00*	Normal operation mode for channel 15 to channel 8
				FFh	Gradation operation mode for channel 15 to channel 8

[1] Each bit represents one channel that can set either 0 for normal mode (use IREFx to set individual LED output current), or 1 for gradation mode (use IREF_GRPx to set group LEDs output current.).

[2] In gradation mode, it only affects the source of the IREF current level and does not affect the PWMx operation or LEDOUTx register function. It is possible to use the gradation feature, individual PWMx and group PWM simultaneously.

7.3.8.6 GRAD_GRP_SEL0 to GRAD_GRP_SEL3, gradation group select registers

Table 20. GRAD_GRP_SEL[0:3] - Gradation group select register for channel 15 to channel 0 (address 3Ah, 3Bh, 3Ch, 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1]
3Ah	GRAD_GRP_SEL0	7:6	W only	00*	Gradation group select for LED3 output
		5:4	W only	00*	Gradation group select for LED2 output
		3:2	W only	00*	Gradation group select for LED1 output
		1:0	W only	00*	Gradation group select for LED0 output
3Bh	GRAD_GRP_SEL1	7:6	W only	01*	Gradation group select for LED7 output
		5:4	W only	01*	Gradation group select for LED6 output
		3:2	W only	01*	Gradation group select for LED5 output
		1:0	W only	01*	Gradation group select for LED4 output
3Ch	GRAD_GRP_SEL2	7:6	W only	10*	Gradation group select for LED11 output
		5:4	W only	10*	Gradation group select for LED10 output
		3:2	W only	10*	Gradation group select for LED9 output
		1:0	W only	10*	Gradation group select for LED8 output
3Dh	GRAD_GRP_SEL3	7:6	W only	11*	Gradation group select for LED15 output
		5:4	W only	11*	Gradation group select for LED14 output
		3:2	W only	11*	Gradation group select for LED13 output
		1:0	W only	11*	Gradation group select for LED12 output

[1] LED[3:0] outputs default assigned to group 0; LED[7:4] outputs default assigned to group 1; LED[11:8] outputs default assigned to group 2; LED[15:12] outputs default assigned to group 3.

7.3.8.7 GRAD_CNTL, Gradation control register

Table 21. GRAD_CNTL - Gradation control register for group 3 to group 0 (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Eh	GRAD_CNTL	7	W only	0*	Gradation stop for group 3[1]
				1	Gradation start for group 3[2]
		6	W only	0*	Single shot operation for group 3
				1	Continuous operation for group 3
		5	W only	0*	Gradation stop for group 2[1]
				1	Gradation start for group 2[2]
		4	W only	0*	Single shot operation for group 2
				1	Continuous operation for group 2
		3	W only	0*	Gradation stop for group 1[1]
				1	Gradation start for group 1[2]
		2	W only	0*	Single shot operation for group 1
				1	Continuous operation for group 1
		1	W only	0*	Gradation stop for group 0[1]
				1	Gradation start for group 0[2]
		0	W only	0*	Single shot operation for group 0
				1	Continuous operation for group 0

[1] When the gradation operation is forced to stop by writing 0, the output current stops immediately and is frozen at the last output level.

[2] Writing 1 to this bit starts the gradation operation, and writing 0 to this bit forces the gradation operation to stop when single mode is not completed or continuous mode is running.