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PC7447A
PowerPC 7447A RISC Microprocessor

Datasheet

Features

- 3000 Dhrystone 2.1 MIPS at 1.3 GHz
- Selectable Bus Clock (30 CPU Bus Dividers up to 28x)
- Selectable MPx/60x Interface Voltage (1.8V, 2.5V)
- P_D Typically 18W at 1.33 GHz at V_{DD} = 1.3V; 8.0W at 1 GHz at V_{DD} = 1.1V Full Operating Conditions
- Nap, Doze and Sleep Power Saving Modes
- Superscalar (Four Instructions Fetched Per Clock Cycle)
- 4 GB Direct Addressing Range
- Virtual Memory: 4 Hexabytes (2^{52})
- 64-bit Data and 36-bit Address Bus Interface
- Integrated L1: 32 KB Instruction and 32 KB Data Cache
- Integrated L2: 512 KB
- 11 Independent Execution Units and three Register Files
- Write-back and Write-through Operations
- f_{INT} Max = 1.167 MHz
- f_{BUS} Max = 133 MHz/166 MHz

Description

The PC7447A host processor is a high-performance, low-power, 32-bit implementations of the PowerPC® Reduced Instruction Set Computer (RISC) architecture combined with a full 128-bit implementation of Freescale's AltiVec technology.

This microprocessor is ideal for leading-edge embedded computing and signal processing applications. The PC7447A features 512 KB of on-chip L2 cache. The PC7447A microprocessor has no backside L3 cache, allowing for a smaller package designed as a pin-for-pin replacement for the PC7447 microprocessor. This device benefits from a silicon-on-insulator (SOI) CMOS process technology, engineered to help deliver tremendous power savings without sacrificing speed. A low-power version of the PC7447A microprocessor is also available.

Figure 1-1 on page 2 shows a block diagram of the PC7447A. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit. The memory storage subsystem supports the MPX bus protocol and a subset of the 60x bus protocol to the main memory and other system resources.

Note that the PC7447A is a footprint-compatible, drop-in replacement in a PC7447 application if the core power supply is 1.3V.

Screening

- Full Military Temperature Range (T_J = -55°C, +125°C)
- Industrial Temperature Range (T_J = -40°C, +110°C)

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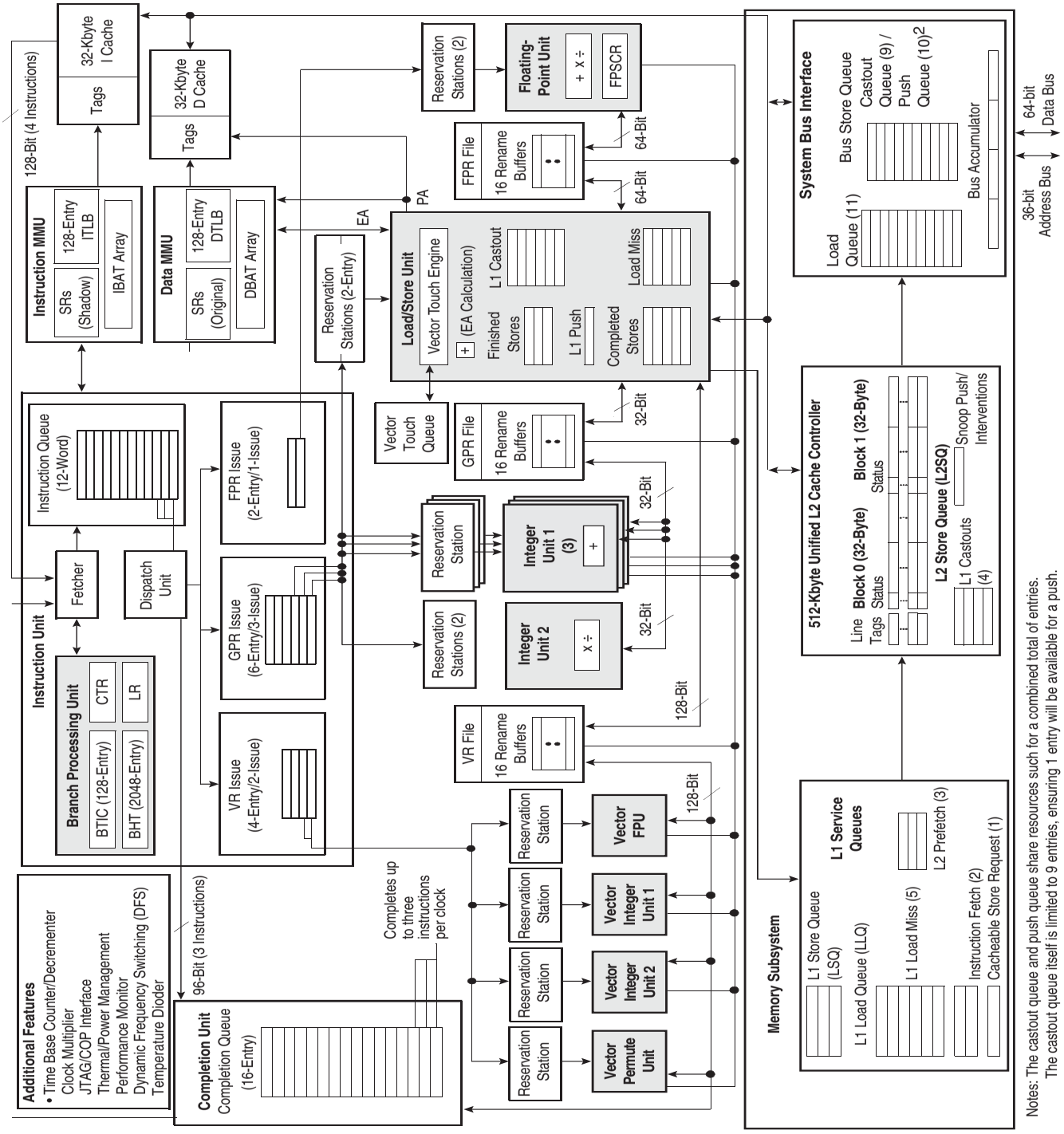
1. Block Diagram

Figure 1-1. PC7447A Microprocessor Block Diagram



Notes: The castout queue and push queue share resources such for a combined total of entries.
The castout queue itself is limited to 9 entries, ensuring 1 entry will be available for a push.

2. Features

This section summarizes features of the PC7447A implementation of the PowerPC architecture.

Major features of the PC7447A are as follows:

- High-performance, superscalar microprocessor
  - Up to four instructions can be fetched from the instruction cache at a time
  - Up to 12 instructions can be in the instruction queue (IQ)
  - Up to 16 instructions can be at some stage of execution simultaneously
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.

    2048-entry branch history table (BHT) with two bits per entry for four levels of prediction: not taken, strongly not taken, taken, and strongly taken

    Up to three outstanding speculative branches

    Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream

    Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (BCLR) instructions

  - Four integer units (IUs) that share 32 GPRs for integer operands

    Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.

    IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.

  - Five-stage FPU and a 32-entry FPR file

    Fully IEEE® 754-1985-compliant FPU for both single- and double-precision operations

    Supports non-IEEE mode for time-critical operations

    Hardware support for denormalized number

Thirty-two 64-bit FPRs for single- or double-precision operands

– Four vector units and 32-entry vector register file (VRs)

Vector permute unit (VPU)

Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, vaddsbs, vaddshs, and vaddsws).

Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, vmhaddshs, vmhraddshs, and vmladduhm).

Vector floating-point unit (VFPU)

– Three-stage load/store unit (LSU)

Supports integer, floating-point, and vector instruction load/store traffic

Four-entry vector touch queue (VTQ) supports all four architectures of the AltiVec data stream operations

Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput

Four-cycle FPR load latency (single, double) with one-cycle throughput

No additional delay for misaligned access within double-word boundary
Dedicated adder calculates effective addresses (EAs)

Supports store gathering

Performs alignment, normalization, and precision conversion for floating-point data

Executes cache control and TLB instructions

Performs alignment, zero padding, and sign extension for integer data

Supports hits under misses (multiple outstanding misses)

Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  – Instructions can only be dispatched from the three lowest IQ entries: IQ0, IQ1, and IQ2
  – A maximum of three instructions can be dispatched to the issue queues per clock cycle
  – Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue)

- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard Architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 512-Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - Cache write-back or write-through operation programmable on a per-page or per-block basis 64-byte, two-sectored line size
  - Parity support on cache
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address

  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation look aside buffers (TLBs)

    Both TLBs are 128-entry, two-way set-associative, and use a LRU replacement algorithm

    TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).
- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and the L2 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - A new dynamic frequency switching (DFS) feature allows the processor core frequency to be halved through software to reduce power consumption
  - The following three power-saving modes are available to the system:

    Nap: Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol.

    Sleep: Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.

    Deep sleep: When the part is in the deep Sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.

  - Instruction cache throttling provides control of instruction fetching to limit device temperature
  - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST), factory test only
- Reliability and serviceability
  - Parity checking on system bus
  - Parity checking on the L1 and L2 caches

3. General Parameters

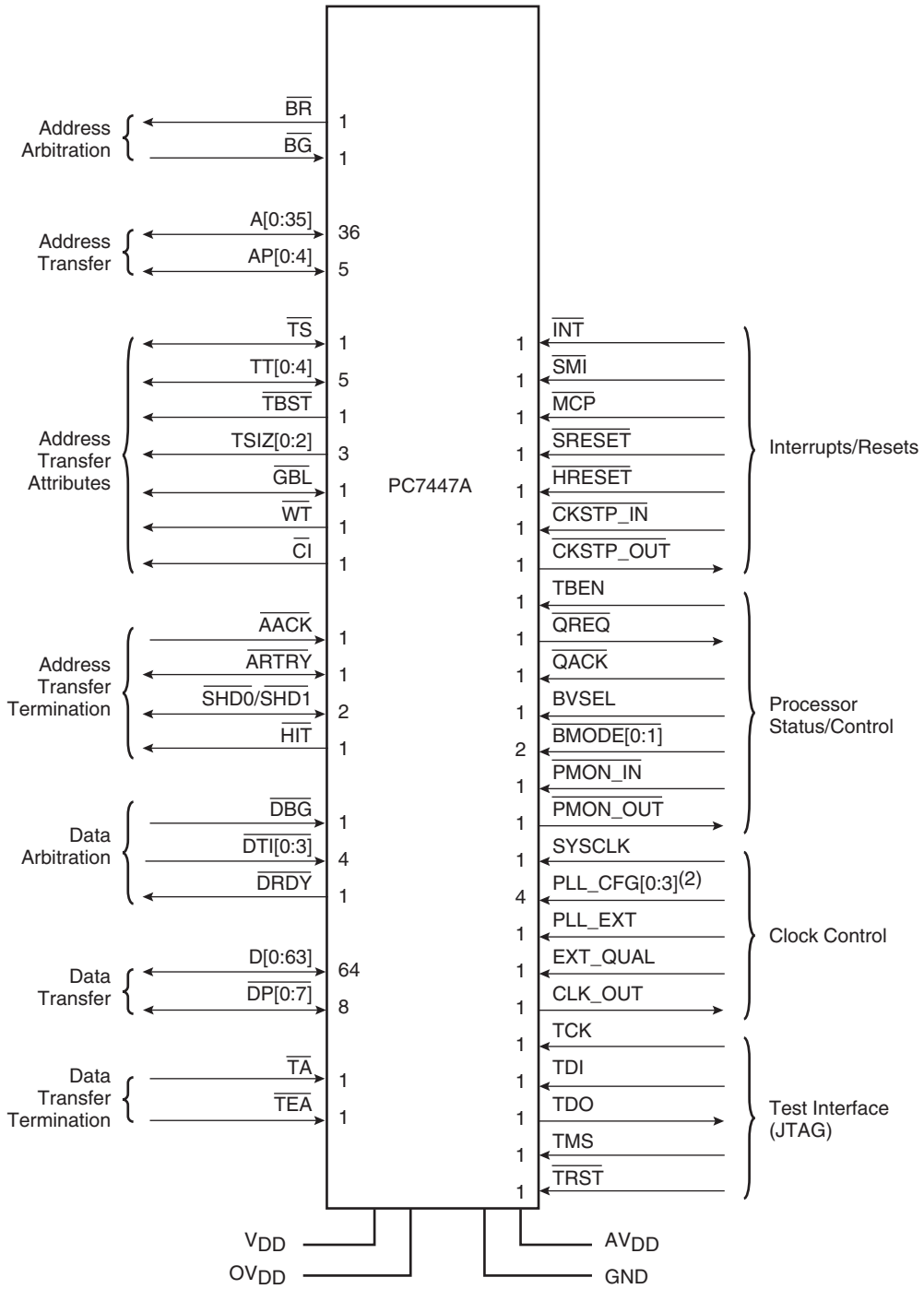
Table 3-1 provides a summary of the general parameters of the PC7447A.

Table 3-1. Device Parameters

Parameter	Description
Technology	0.13 µm CMOS, nine-layer metal
Die size	8.51 mm × 9.86 mm
Transistor count	48.6 million
Logic design	Fully-static
Packages	Surface mount 360 ceramic ball grid array (HITCE)
Core power supply	1.3V ± 50 mV and 1.1V ± 50 mV DC nominal
I/O power supply	1.8V ± 5% DC, or 2.5V ±5% DC

4. Signal Description

Figure 4-1. PC7447A Microprocessor Signal Groups



Note: For the PC7447A, there are 5 PLL_CFG signals, (PLL_CFG[0:4]

5. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7447A in compliance with e2v standard screening.

6. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

6.1 Design and Construction

6.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 8-1, Table 6-2 and Figure 4-1.

6.2 Absolute Maximum Ratings

The tables in this section describe the PC7447A DC electrical characteristics. Table 6-1 provides the absolute maximum ratings.

Table 6-1. Absolute Maximum Ratings(1)

Symbol	Characteristic		Maximum Value	Unit
V_{DD}(2)	Core supply voltage		-0.3 to 1.60	V
AV_{DD}(2)	PLL supply voltage		-0.3 to 1.60	V
OV_{DD}(3)(4)	Processor bus supply voltage	BVSEL = 0	-0.3 to 1.95	V
OV_{DD}(3)(5)		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	-0.3 to 2.7	V
V_{IN}(6)(7)	Input voltage	Processor bus	-0.3 to OV_{DD} + 0.3	V
V_{IN}		JTAG signals	-0.3 to OV_{DD} + 0.3	V
T_{STG}	Storage temperature range		-55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 6-2 on page 10. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
3. Caution: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8V mode.
5. BVSEL must be set to HRESET or 1, such that the bus is in 2.5V mode.
6. Caution: V_{IN} must not exceed OV_{DD} by more than 0.3V at any time including during power-on reset.
7. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration shown in Figure 6-1 on page 10.

6.3 Recommended Operating Conditions

Table 6-2 provides the recommended operating conditions for the PC7447A.

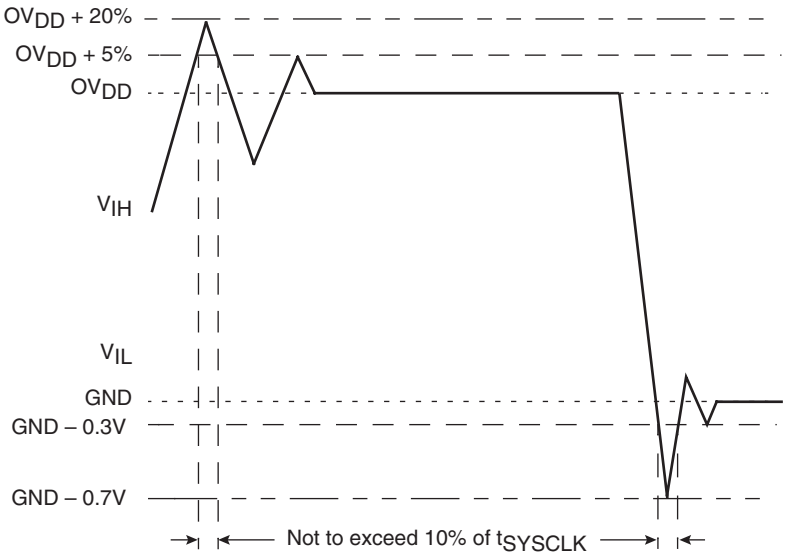
Table 6-2. Recommended Operating Conditions(1)

Symbol	Characteristic		Recommended Value		Unit
			Min	Max	
V_{DD}	Core supply voltage		1.3V ± 50 mV or 1.1V ± 50 mV		V
AV_{DD}(2)	PLL supply voltage		1.3V ± 50 mV or 1.1V ± 50 mV		V
OV_{DD}	Processor bus supply voltage	BVSEL = 0	1.8V ± 5%		V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	2.5V ± 5%		
V_{IN}	Input voltage	Processor bus	GND	OV_{DD}	V
V_{IN}		JTAG signals	GND	OV_{DD}	
T_J	Die-junction temperature		-55	125°C	°C

Notes: 1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

2. This voltage is the input to the filter discussed in Section "PLL Power Supply Filtering" on page 41 and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

Figure 6-1. Overshoot/Undershoot Voltage



The PC7447A provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7447A core voltage must always be provided at a nominal 1.3V (see Table 6-2 on page 10 for the actual recommended core voltage). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OVDD power pins. Table 6-3 on page 11 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary.

Table 6-3. Input Threshold Voltage Setting[1]

BVSEL Signal	Processor Bus Input Threshold is Relative to:	Notes
0	1.8V	[2]
¬$\overline{\text{HRESET}}$	Not available	
$\overline{\text{HRESET}}$	2.5V	
1	2.5V	

Notes: 1. Caution: The input threshold selection must agree with the OV_{DD} voltages supplied. See notes in Table 6-1 on page 9.
2. If used, pull-down resistors should be less than 250Ω.

6.4 Thermal Characteristics

6.4.1 Package Characteristics

Table 6-4. Package Thermal Characteristics[1]

Symbol	Characteristic	Value	Unit
$R_{\theta JA}$[2][3]	Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	26	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	19	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board	20	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board	16	°C/W
$R_{\theta JB}$[5]	Junction-to-board thermal resistance	10	°C/W
$R_{\theta JC}$[6]	Junction-to-case thermal resistance	< 0.1	°C/W

Notes: 1. See "Thermal Management Information" on page 12 for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between the die and the case top surface as measured with the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

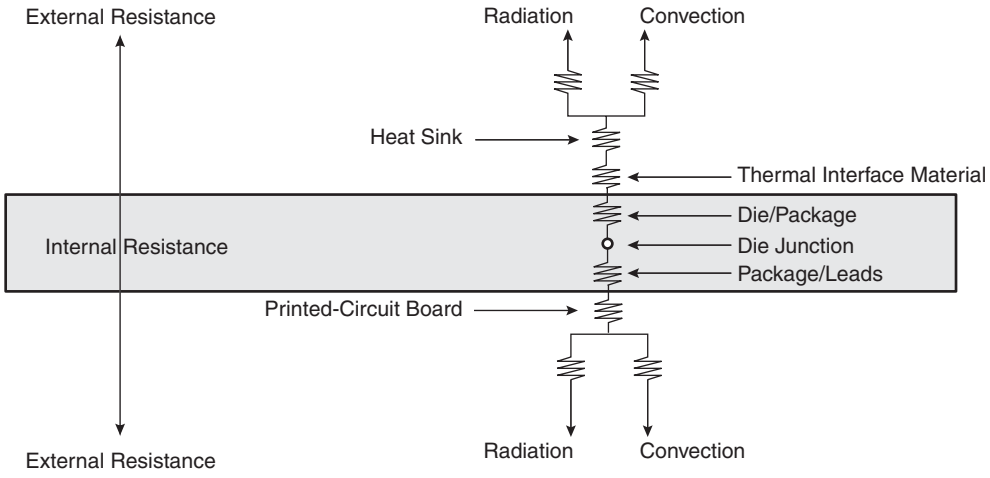
6.4.2 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 6-4 on page 11, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-ball thermal resistance

Figure 9-2 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 6-2. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note the internal versus external package resistance.

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

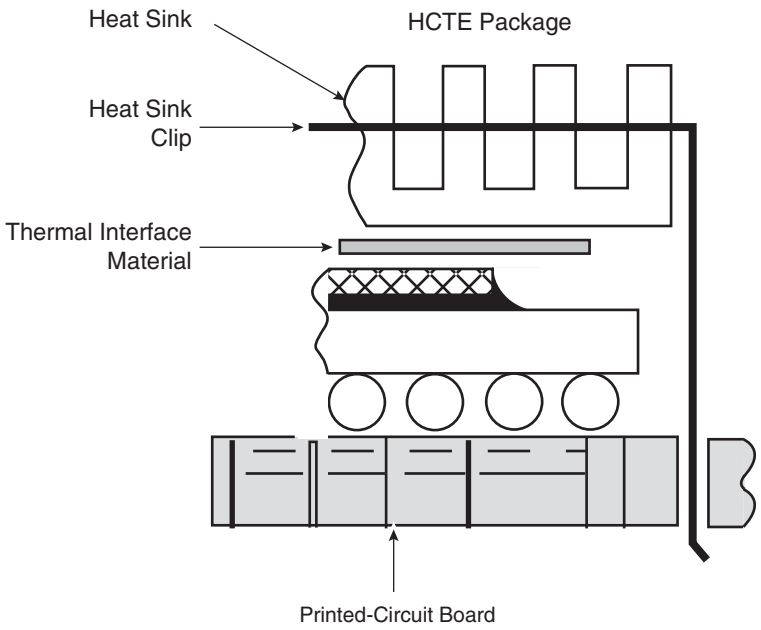
Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

6.4.3 Thermal Management Information

This section provides thermal management information for the high coefficient of the thermal expansion ceramic ball grid array (HITCE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design – the heat sink, airflow, and thermal interface material. The PC7447A implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Table 6-6 on page 19 for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see section “Temperature Diode” on page 16 for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods – spring clips to holes in the printed-circuit board or package, and mounting clips and screw assembly (see Figure 6-3); however, due to the potentially large mass of the heat sink, attachment through the printed-circuit board is suggested. If a spring clip is used, the spring force should not exceed ten pounds.

Figure 6-3. Package Exploded Cross-sectional View with Several Heat Sink Options



6.4.4 Thermal Interface Materials

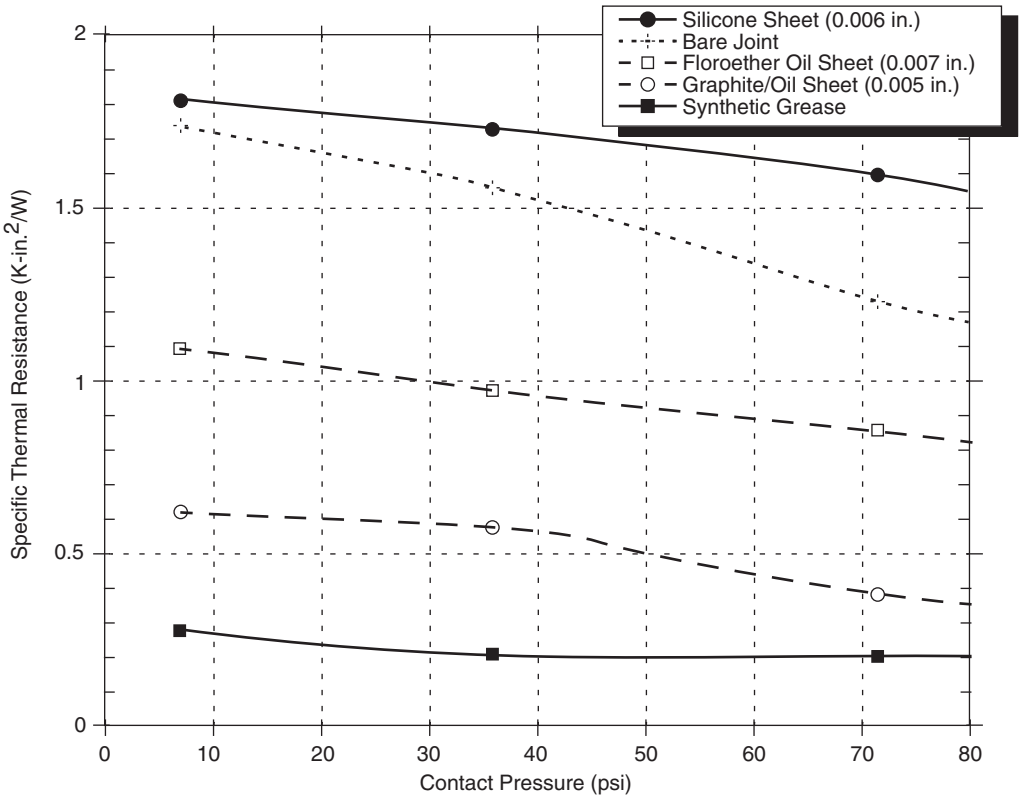
A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-4 on page 14 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure.

As shown, the performance of these thermal interface materials improves with increasing contact pressure.

The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 6-3 on page 13). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the PC7447A. Of course, the selection of any thermal interface material depends on many factors – thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

Figure 6-4. Thermal Performance of Select Thermal Interface Material



6.4.4.1 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_J is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_J) should be maintained less than the value specified in Table 6-2 on page 10. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, an HITCE package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7W, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 18.7W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 6-2 on page 10.

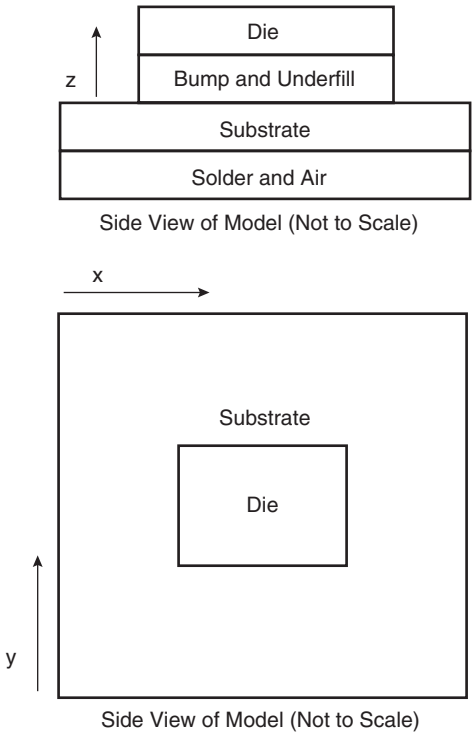
Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature – airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the PC7447A thermal model is shown in Figure 6-5 on page 16. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die, and bump-underfill, have the same size as the die. The silicon die should be modeled 9.5 × 9.5 × 0.7 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 7.3 × 9.3 × 0.7 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m × K) in the xy-plane and 1.9 W/(m × K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm, and has 8.1 W/(m × K) isotropic conductivity in the xy-plane and 4 W/(m × K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and are 0.6 mm thick. They can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m × K) in the xy-plane direction and 3.8 W/(m × K) in the direction of the z-axis.

Figure 6-5. Recommended Thermal Model of PC7447A

Conductivity	Value	Unit
Bump and Underfill (7.3 x 9.3 x 0.070 mm)		
k_x	0.6	W/(m x K)
k_y	0.6	
k_z	1.9	
Substrate (25 x 25 x 1.2 mm)		
k_x	8.1	
k_y	8.1	
k_z	4.0	
Solder Ball and Air (25 x 25 x 0.6 mm)		
k_x	0.034	
k_y	0.034	
k_z	3.8	



6.4.4.2 Temperature Diode

The PC7447A has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices. These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each PC7447A's internal diode.

The following are the specifications of the PC7447A on-board temperature diode:

$V_f > 0.40V$

$V_f < 0.90V$

Operating range 2 - 300 µA

Diode leakage < 10 nA at 125°C

Ideality factor over 5 µA – 150 µA at 60°C: 1 <= n <= TBD

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fW} = I_s\left[e^{\frac{qV_f}{nKT}} - 1\right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[In\frac{I_H}{I_L}\right]$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron (1.6×10^{-19} C)

n = Ideality factor (normally 1.0)

K = Boltzman's constant (1.38×10^{-23} Joules/K)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$V_H - V_L = 1.986 \times 10^{-4} \times nT$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1{,}986 \times 10^{-4}}$$

6.4.4.3 *Dynamic Frequency Switching (DFS)*

The new DFS feature in the PC7447A adds the ability to divide the processor-to-system bus ratio by two during normal functional operation by setting the HID1[DFS1] bit. The frequency change occurs in 1 clock cycle, and no idle waiting period is required to switch between modes. Additional information regarding DFS can be found in the MPC7450 RISC Microprocessor Family User's Manual.

6.4.4.4 *Power Consumption with DFS Enabled*

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}(P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 6-6 on page 19)

P_{DS} = Deep sleep mode power consumption (see Table 6-6 on page 19)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

6.4.4.5 *Bus-to-Core Multiplier Constraints with DFS*

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:4] during hard reset. Specifically, because the PC7447A does not support quarter clock ratios or the 1x multiplier, the DFS feature is limited to integer PLL multipliers of 4x and higher. The complete listing is shown in Table 6-5 on page 18.

Table 6-5. Valid Divide Ratio Configurations

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 12-1 on page 39)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
2x	N/A
3x	N/A
4x	2x
5x	2.5x
5.5x	2x
6x	3x
6.5x	N/A
7x	3.5x
7.5x	N/A
8x	4x
8.5x	N/A
9x	4.5x
9.5x	N/A
10x	5x
10.5x	N/A
11x	5.5x
11.5x	N/A
12x	6x
12.5x	N/A
13x	6.5x
13.5x	N/A
14x	7x
15x	7.5x
16x	8x
17x	8.5x
18x	9x
20x	10x
21x	10.5x
24x	12x
28x	14x

6.4.4.6 *Minimum Core Frequency Requirements with DFS*

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 9-2 on page 25. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

6.4.5 Power Consumption

Table 6-6 provides the power consumption for the PC7447A. For information regarding power consumption when dynamic frequency switching is enabled, See "Dynamic Frequency Switching (DFS)" on page 17.

Table 6-6. Power Consumption for PC7447A

	Processor (CPU) Frequency					
	1000	**1167**	**1267**	**1333**(5)	**1420**	**Unit**
Full-Power Mode						
Core Power Supply	1.1	1.1	1.3	1.3	1.3	
Typical(1)(2)	8	9.2	18.3	18	21	W
Maximum(1)(3)	11.5	13	26	25	30	W
Nap Mode						
Typical(1)(2)	1.3	1.3	4.1	3.3	4.1	W
Sleep Mode						
Typical(1)(2)	1.3	1.3	4.1	3.3	4.1	W
Deep Sleep Mode (PLL Disabled)						
Typical(1)(2)	1.2	1.2	4	3.2	4	W

Notes:
1. These values apply for all valid processor buses. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 6-2 on page 10) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz
3. Maximum power is the average measured at nominal V_{DD} and maximum operating junction temperature (see Table 6-2 on page 10) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Power consumption for these devices is artificially constrained during screening to assure lower power consumption than other speed grades.

7. Pin Assignment

Figure 7-1 shows the pinout of the PC7447A, 360 high coefficient of the thermal expansion ceramic ball grid array (HITCE) package as viewed from the top surface. Figure 7-2 shows the side profile of the HITCE package to indicate the direction of the top surface view.

Figure 7-1. Pinout of the PC7447A, 360 HITCE Package as Viewed from the Top Surface

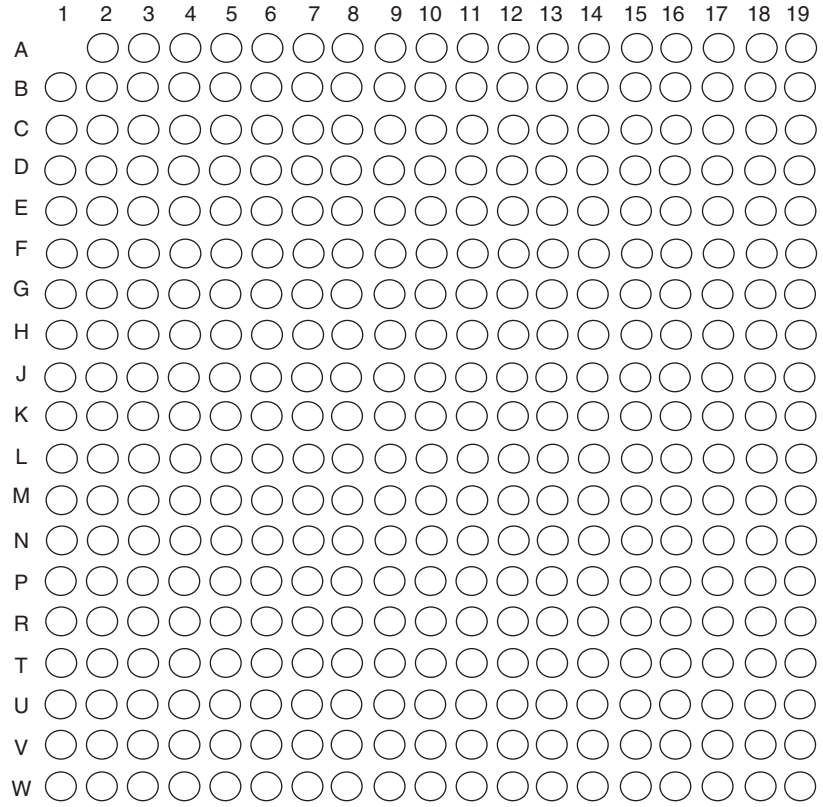
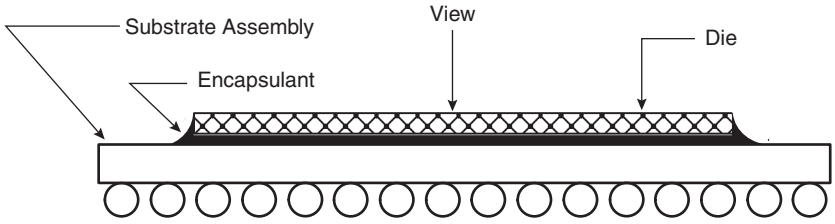


Figure 7-2. Side View of the CBGA Package



8. Pinout Listings

Table 8-1 provides the pinout listing for the PC7447A, 360 HITCE package. The pinouts of the PC7447A and PC7447 are pin compatible but there have been some changes. A PC7447A may be populated on a board designed for a PC7447 provided all pins defined as 'Not Connected' for the PC7447 are unterminated as required by the PC7457 RISC Microprocessor Specification. The PC7447A uses pins previously marked 'Not Connected' for the temperature diode pins and for additional power and ground connections. Because these 'Not Connected' pins in the PC7447 360 pin package are not driven in functional mode, a PC7447 can be populated in a PC7447A board. See section "Connection Recommendations" on page 41 for additional information.

Note: This pinout is not compatible with the PC750, PC7400, or PC7410 360 BGA package.

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package

Signal Name	Pin Number	Active	I/O	I/F Select(1)
A[0:35](2)	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL
AP[0:4](2)	C1, E3, H6, F5, G7	High	I/O	BVSEL
$\overline{\text{ARTRY}}$(3)	N2	Low	I/O	BVSEL
AV_{DD}	A8	–	Input	BVSEL
$\overline{\text{BG}}$	M1	Low	Input	BVSEL
$\overline{\text{BMODE0}}$(4)	G9	Low	Input	BVSEL
$\overline{\text{BMODE1}}$(5)	F8	Low	Input	BVSEL
$\overline{\text{BR}}$	D2	Low	Output	BVSEL
BVSEL(1)(6)	B7	High	Input	BVSEL
$\overline{\text{CI}}$(3)	J1	Low	Output	BVSEL
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL
CLK_OUT	H2	High	Output	BVSEL
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	BVSEL
$\overline{\text{DBG}}$	M2	Low	Input	BVSEL
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	BVSEL
$\overline{\text{DRDY}}$(7)	R3	Low	Output	BVSEL
DTI[0:3](8)	G1, K1, P1, N1	High	Input	BVSEL
EXT_QUAL(9)	A11	High	Input	BVSEL
$\overline{\text{GBL}}$	E2	Low	I/O	BVSEL

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	–	–	N/A
GND[15]	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	–	–	N/A
GND_SENSE[19]	G12, N13	–	–	N/A
$\overline{\text{HIT}}$[7]	B2	Low	Output	BVSEL
$\overline{\text{HRESET}}$	D8	Low	Input	BVSEL
$\overline{\text{INT}}$	D4	Low	Input	BVSEL
L1_TSTCLK[9]	G8	High	Input	BVSEL
L2_TSTCLK[10]	B3	High	Input	BVSEL
No Connect[11]	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	–	–	–
$\overline{\text{LSSD\_MODE}}$[6][12]	E8	Low	Input	BVSEL
$\overline{\text{MCP}}$	C9	Low	Input	BVSEL
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	–	–	N/A
OV_{DD}_SENSE[16]	E18, G18	–	–	N/A
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	BVSEL
$\overline{\text{PMON\_IN}}$[13]	D9	Low	Input	BVSEL
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	BVSEL
$\overline{\text{QACK}}$	G5	Low	Input	BVSEL
$\overline{\text{QREQ}}$	P4	Low	Output	BVSEL
$\overline{\text{SHD}}$[0:1][3]	E4, H5	Low	I/O	BVSEL
$\overline{\text{SMI}}$	F9	Low	Input	BVSEL
$\overline{\text{SRESET}}$	A2	Low	Input	BVSEL
SYSCLK	A10	–	Input	BVSEL
$\overline{\text{TA}}$	K6	Low	Input	BVSEL
TBEN	E1	High	Input	BVSEL
$\overline{\text{TBST}}$	F11	Low	Output	BVSEL
TCK	C6	High	Input	BVSEL
TDI[6]	B9	High	Input	BVSEL
TDO	A4	High	Output	BVSEL
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL
TEMP_ANODE[17]	N18			
TEMP_CATHODE[17]	N19			

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
TEST[0:3][12]	A12, B6, B10, E10	–	Input	BVSEL
TEST[4][9]	D10	–	Input	BVSEL
TMS[6]	F1	High	Input	BVSEL
$\overline{\text{TRST}}$[6][14]	A5	Low	Input	BVSEL
$\overline{\text{TS}}$[3]	L4	Low	I/O	BVSEL
TSIZ[0:2]	G6, F7, E7	High	Output	BVSEL
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	BVSEL
$\overline{\text{WT}}$[3]	D3	Low	Output	BVSEL
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	–	–	N/A
V_{DD}[15]	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	–	–	N/A
V_{DD}_SENSE[18]	G13, N12	–	–	N/A

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, connect BVSEL to either GND (selects 1.8V), or to $\overline{\text{HRESET}}$ or OV_{DD} (selects 2.5V); see Table 6-3 on page 11. If used, the pull-down resistor should be less than 250Ω. Because these settings may change in future products, it is recommended BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{IN} or supply voltages see Table 6-2 on page 10.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the PC7447A and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the PC7447A is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the PC7447, have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. These pins were NCs on the PC7447. They may be left unconnected for backward compatibility with these devices, but it is recommended they be connected in new designs to facilitate future products. See section "Connection Recommendations" on page 41 for more information.
16. These pins were OV_{DD} pins on the PC7447. These pins are internally connected to OV_{DD} and are intended to allow an external device to detect the I/O voltage level present inside the device package. If unused, they must be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.

18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.

Note: Caution must be exercised when performing boundary scan test operations on a board designed for a PC7447A but populated with an PC7447. This is because in the PC7447 it is possible to drive the latches associated with the former 'No Connect' pins in the PC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal PC7447 latches do not cause these pins to be driven during board testing.

9. Electrical Characteristics

9.1 Static Characteristics

Table 9-1 provides the DC electrical characteristics for the PC7447A.

Table 9-1. DC Electrical Specifications (see Table 6-2 on page 10 for Recommended Operating Conditions)

Symbol	Characteristic	Nominal Bus Voltage(1)	Min	Max	Unit	Notes
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)
I_{TSI}	High-impedance (off-state) leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)(4)
V_{OH}	Output high voltage at I_{OH} = -5 mA	1.8	OV_{DD} - 0.45	–	V	
		2.5	1.8	–		
V_{OL}	Output low voltage at I_{OL} = 5 mA	1.8	–	0.45	V	
		2.5	–	0.6		
C_{IN}	Capacitance, V_{IN} = 0V f = 1 MHz — All other inputs		–	8	pF	(5)
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakge current, $V_{IN} = GV_{DD}/OV_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)

Notes: 1. Nominal voltages; see Table 6-2 on page 10 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.

3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. Excludes signals with internal pull ups: BVSEL, $\overline{\text{LSSD\_MODE}}$, TDI, TMS, and $\overline{\text{TRST}}$. Characterization of leakage current for these signals is currently being conducted.

9.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7447A. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section "Clock AC Specifications" on page 25 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals, and can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; See "Ordering Information" on page 46. for information on ordering parts. DFS is described in Section "Dynamic Frequency Switching (DFS)" on page 17.

9.2.1 Clock AC Specifications

Table 9-2 provides the clock AC timing specifications as defined in Figure 9-1 on page 26 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 9-2 on page 25 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7447A will be a function of the AC timings of the PC7447A, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 9-2 on page 25.

Table 9-2. Clock AC Timing Specifications (See Table 6-2 on page 10 for Recommended Operating Conditions)

		Maximum Processor Core Frequency									
		1000 MHz		1267 MHz		1333 MHz		1420 MHz			
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3		V_{DD} = 1.3			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
f_{CORE}	Processor core frequency	600	1000	600	1267	600	1333	600	1420	MHz	(1)(8)(9)
f_{VCO}	VCO frequency	1200	2000	1200	2533	1200	2667	1200	2840	MHz	(1)(9)
f_{SYSCLK}	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz	(1)(2)(8)
t_{SYSCLK}	SYSCLK cycle time	6.0	30	6	30	6	30	6	30	ns	(2)
t_{KR}, t_{KF}	SYSCLK rise and fall time	–	1.0	–	1	–	1	–	1	ns	(3)
t_{KHKL}/t_{SYSCLK}	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	40	60	%	(4)
	SYSCLK jitter(5)(6)	–	150	–	150	–	150	–	150	ps	(5)(6)
	Internal PLL relock time(7)	–	100	–	100	–	100	–	100	µs	(7)