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Features

- 3000 Dhrystone 2.1 MIPS at 1.3 GHz
- Selectable Bus Clock (30 CPU Bus Dividers up to 28x)
- 13 Selectable Core-to-L3 Frequency Divisors
- Selectable MPx/60x Interface Voltage (1.8V, 2.5V)
- Selectable L3 Interface of 1.8V or 2.5V
- P_D Typical 12.6W at 1 GHz at V_{DD} = 1.3V; 8.3W at 1 GHz at V_{DD} = 1.1V, Full Operating Conditions
- Nap, Doze and Sleep Modes for Power Saving
- Superscalar (Four Instructions Fetched Per Clock Cycle)
- 4 GB Direct Addressing Range
- Virtual Memory: 4 Hexabytes (2^{52})
- 64-bit Data and 36-bit Address Bus Interface
- Integrated L1: 36 KB Instruction and 32 KB Data Cache
- Integrated L2: 512 KB
- 11 Independent Execution Units and Three Register Files
- Write-back and Write-through Operations
- f_{INT} Max = 1 GHz (1.2 GHz to be Confirmed)
- f_{BUS} Max = 133 MHz/166 MHz

Description

The PC7457 is implementations of the PowerPC® microprocessor family of reduced instruction set computer (RISC) microprocessors. This document describes pertinent electrical and physical characteristics of the PC7457.

The PC7457 is the fourth implementation of the fourth generation (G4) microprocessors from Freescale. The PC7457 implements the full PowerPC 32-bit architecture and is targeted at networking and computing systems applications. The PC7457 consists of a processor core, a 512 Kbyte L2, and an internal L3 tag and controller which support a glueless backside L3 cache through a dedicated high-bandwidth interface.

The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit. The memory storage subsystem supports the MPX bus interface to main memory and other system resources. The L3 interface supports 1, 2, or 4M bytes of external SRAM for L3 cache and/or private memory data. For systems implementing 4M bytes of SRAM, a maximum of 2M bytes may be used as cache; the remaining 2M bytes must be private memory.

Note that the PC7457 is a footprint-compatible, drop-in replacement in a PC7455 application if the core power supply is 1.3V.

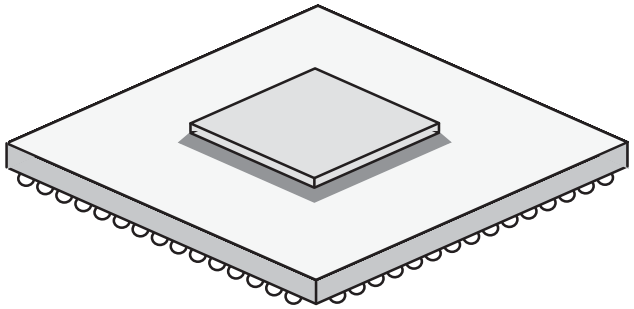
PowerPC 7457 RISC Microprocessor

PC7457

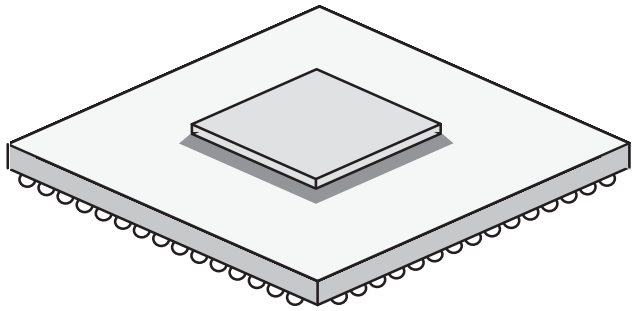
Rev. 5345D–HIREL–07/06

Screening

- CBGA Upscreenings Based on Atmel Standards
- Full Military Temperature Range (T_J = -55° C, +125° C), Industrial Temperature Range (T_J = -40° C, +110° C)
- HCTE Package for the 7457



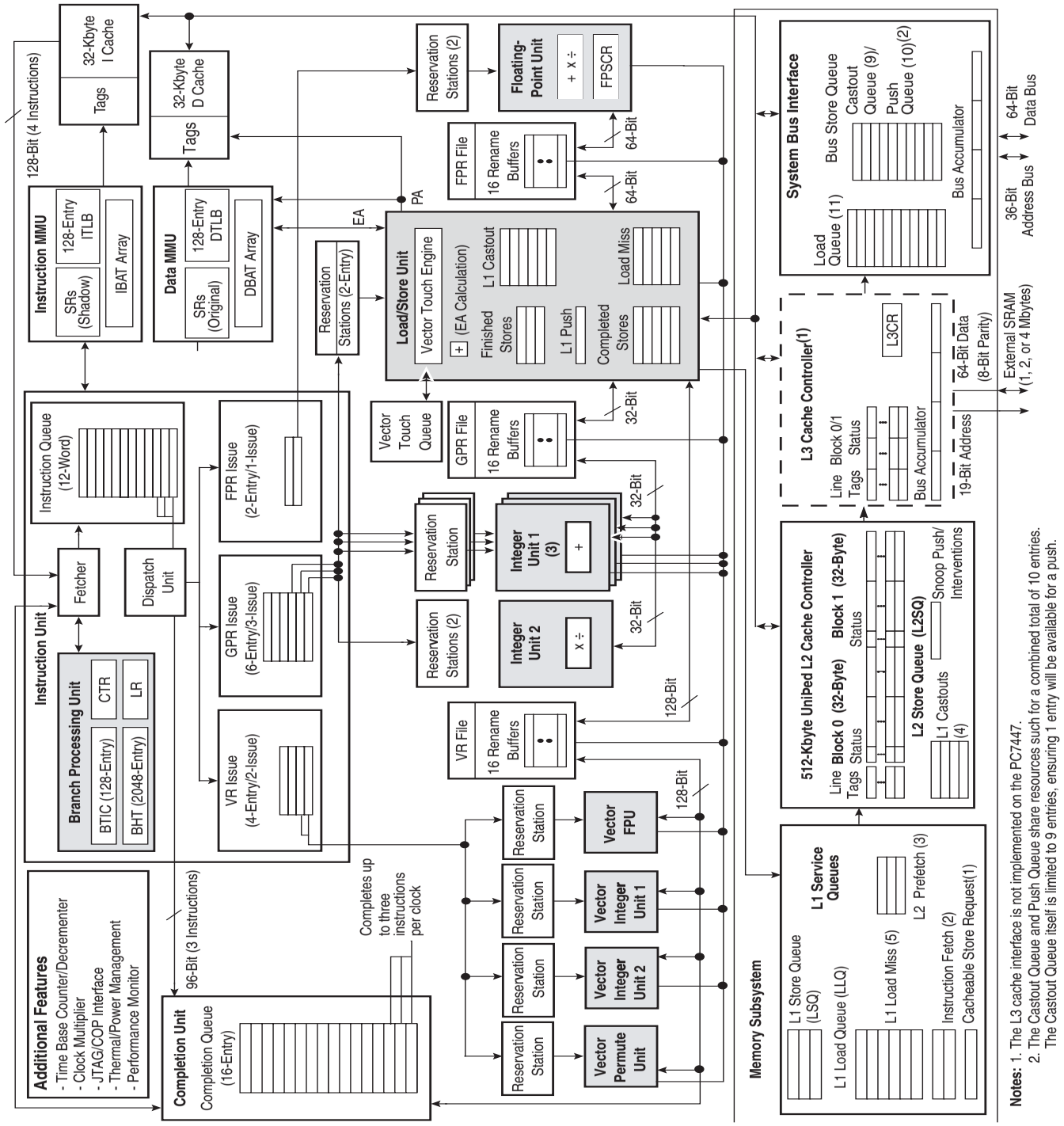
G suffix
CBGA 483
Ceramic Ball Grid Array



GH suffix
HITCE 483
Ceramic Ball Grid Array

1. Block Diagram

Figure 1-1. PC7457 Microprocessor Block Diagram



Notes: 1. The L3 cache interface is not implemented on the PC7447.
2. The Castout Queue and Push Queue share resources such for a combined total of 10 entries. The Castout Queue itself is limited to 9 entries, ensuring 1 entry will be available for a push.

2. General Parameters

Table 2-1 provides a summary of the general parameters of the PC7457.

Table 2-1. Device Parameters

Parameter	Description
Technology	0.13 µm CMOS, nine-layer metal
Die size	9.1 mm × 10.8 mm
Transistor count	58 million
Logic design	Fully-static
Packages	PC7447: surface mount 360 ceramic ball grid array (CBGA) PC7457: surface mount 483 ceramic ball grid array (CBGA) + HiTCE CBGA
Core power supply	1.3V ±500 mV DC nominal or 1.1V ±50 mV (nominal, see "Recommended Operating Conditions(1)" on page 12
I/O power supply	1.8V ±5% DC, or 2.5V ±5% for recommended operating conditions

3. Overview

This section summarizes features of the PC7457 implementation of the PowerPC architecture. Major features of the PC7457 are as follows:

- High-performance, superscalar microprocessor
  - As many as 4 instructions can be fetched from the instruction cache at a time
  - As many as 3 instructions can be dispatched to the issue queues at a time
  - As many as 12 instructions can be in the instruction queue (IQ)
  - As many as 16 instructions can be at some stage of execution simultaneously
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control

- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction

    128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream

    2048-entry branch history table (BHT) with two bits per entry for four levels of prediction – not-taken, strongly not-taken, taken, and strongly taken

    Up to three outstanding speculative branches

    Branch instructions that don't update the count register (CTR) or link register (LR) are often removed from the instruction stream

Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (BCLR) instructions

– Four integer units (IUs) that share 32 GPRs for integer operands

Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions

IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions

– Five-stage FPU and a 32-entry FPR file

Fully IEEE 754-1985-compliant FPU for both single- and double-precision operations

Supports non-IEEE mode for time-critical operations

Hardware support for denormalized numbers

Thirty-two 64-bit FPRs for single- or double-precision operands

– Four vector units and 32-entry vector register file (VRs)

Vector permute unit (VPU)

Vector integer unit 1 (VIU1) handles short-latency AltiVec integer instructions, such as vector add instructions (vaddsbs, vaddshs, and vaddsws, for example)

Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (vmhaddshs, vmhraddshs, and vmladduhm, for example)

Vector floating-point unit (VFPU)

– Three-stage load/store unit (LSU)

Supports integer, floating-point, and vector instruction load/store traffic

Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations

Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with one-cycle throughput

Four-cycle FPR load latency (single, double) with one-cycle throughput

No additional delay for misaligned access within double-word boundary

Dedicated adder calculates effective addresses (EAs)

Supports store gathering

Performs alignment, normalization, and precision conversion for floating-point data

Executes cache control and TLB instructions

Performs alignment, zero padding, and sign extension for integer data

Supports hits under misses (multiple outstanding misses)

Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries – IQ0, IQ1, and IQ2
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle
  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue)
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 Instruction and data caches (Harvard Architecture)
  - 32 Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis

  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding
- Level 2 (L2) cache interface
  - On-chip, 512 Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - PLRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte, two-sectored line size
  - Parity support on cache
- Level 3 (L3) cache interface (not implemented on PC7447)
  - Provides critical double-word forwarding to the requesting unit
  - Internal L3 cache controller and tags
  - External data SRAMs
  - Support for 1, 2, and 4M bytes (MB) total SRAM space
  - Support for 1 or 2 MB of cache space
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte (1 MB) or 128-byte (2 MB) sectored line size
  - Private memory capability for half (1 MB minimum) or all of the L3 SRAM space for a total of 1-, 2-, or 4-MB of private memory
  - Supports MSUG2 dual data rate (DDR) synchronous Burst SRAMs, PB2 pipelined synchronous Burst SRAMs, and pipelined (register-register) Late Write synchronous Burst SRAMs
  - Supports parity on cache and tags
  - Configurable core-to-L3 frequency divisors
  - 64-bit external L3 data bus sustains 64-bit per L3 clock cycle
- Separate memory management units (MMUs) for Instructions and data
  - 52-bit virtual address; 32- or 36-bit physical address
  - Address translation for 4 Kbyte pages, variable-sized blocks, and 256M bytes segments

  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    Both TLBs are 128-entry, two-way set-associative, and use LRU replacement algorithm
    TLBs are hardware- or software-reloadable (that is, on a TLB miss a page table search is performed in hardware or by system software)

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2/L3 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and L2/L3 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.6V processor core
  - The following three power-saving modes are available to the system:

    Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol

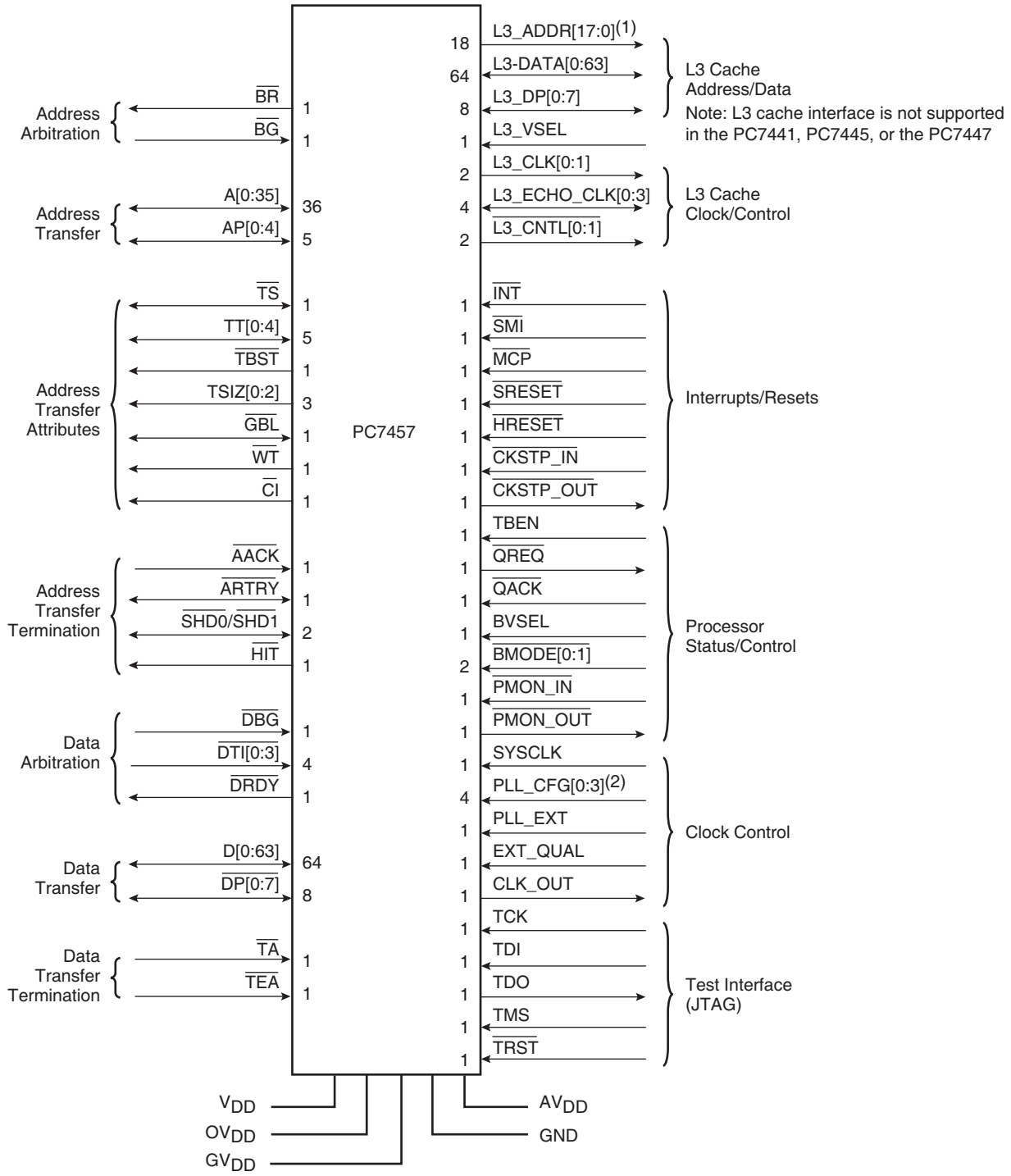
    Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled

    Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state

  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and a PC7457-specific thermal management exception
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST) – factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

4. Signal Description

Figure 4-1. PC7457 Microprocessor Signal Groups



Notes: 1. For the PC7457, there are 19 L3_ADDR signals, (L3_ADDR[0:18].
2. For the PC7447 and PM7457, there are 5 PLL_CFG signals, (PLL_CFG[0:4].

5. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7457 in compliance with Atmel standard screening.

6. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

6.1 Design and Construction

6.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in "Recommended Operating Conditions(1)" on page 12 and Figure 4-1 on page 10.

6.1.2 Absolute Maximum Ratings(1)

Symbol	Characteristic		Maximum Value	Unit
V_{DD}(2)	Core supply voltage		-0.3 to 1.60	V
AV_{DD}(2)	PLL supply voltage		-0.3 to 1.60	V
OV_{DD}(3)(4)	Processor bus supply voltage	BVSEL = 0	-0.3 to 1.95	V
OV_{DD}(3)(5)		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	-0.3 to 2.7	V
GV_{DD}(3)(6)	L3 bus supply voltage	L3VSEL = ¬$\overline{\text{HRESET}}$	-0.3 to 1.65	V
GV_{DD}(3)(7)		L3VSEL = 0	-0.3 to 1.95	V
GV_{DD}(3)(8)		L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	-0.3 to 2.7	V
V_{IN}(9)(10)	Input voltage	Processor bus	-0.3 to OV_{DD} + 0.3	V
V_{IN}(9)(10)		L3 bus	-0.3 to GV_{DD} + 0.3	V
V_{IN}		JTAG signals	-0.3 to OV_{DD} + 0.3	V
T_{STG}	Storage temperature range		-55 to 150	°C

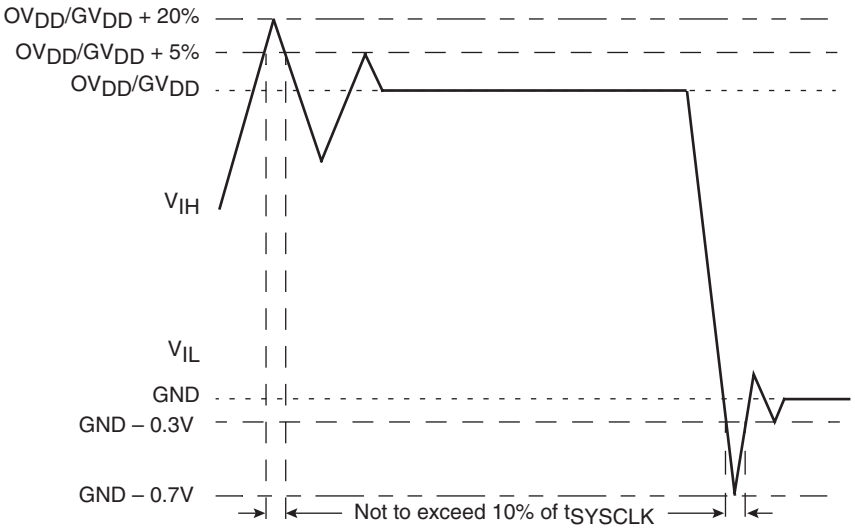
Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions(1)" on page 12. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD}/GV_{DD} by more than 1V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: OV_{DD}/GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5V mode.
6. L3VSEL must be set to ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), such that the bus is in 1.5V mode.
7. L3VSEL must be set to 0, such that the bus is in 1.8V mode.
8. L3VSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5V mode.
9. Caution: V_{IN} must not exceed OV_{DD} or GV_{DD} by more than 0.3V at any time including during power-on reset.
10. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 6-1.

6.1.3 Recommended Operating Conditions[1]

Symbol	Characteristic		Recommended Value		Unit
			Min	Max	
V_{DD}	Core supply voltage		1.3V ±50 mV or 1.1V ±50 mV		V
AV_{DD}[2]	PLL supply voltage		1.3V ±50 mV or 1.1V ±50 mV		V
OV_{DD}	Processor bus supply voltage	BVSEL = 0	1.8V ±5%		V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	2.5V ±5%		V
GV_{DD}	L3 bus supply voltage	L3VSEL = 0	1.8V ±5%		V
GV_{DD}		L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	2.5V ±5%		V
GV_{DD}[3]		L3VSEL = ¬$\overline{\text{HRESET}}$	1.5V ±5%		V
V_{IN}	Input voltage	Processor bus	GND	OV_{DD}	V
V_{IN}		L3 bus	GND	GV_{DD}	V
V_{IN}		JTAG signals	GND	OV_{DD}	V
T_J	Die-junction temperature		-55	125	°C

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. This voltage is the input to the filter discussed in Section "PLL Power Supply Filtering" on page 50 and not necessarily the voltage at the AV_{DD} pin which may be reduced from V_{DD} by the filter.
3. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Figure 6-1. Overshoot/Undershoot Voltage



The PC7457 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7457 core voltage must always be provided at nominal 1.3V (see "Recommended Operating Conditions[1]" on page 12 for actual recommended core voltage). Voltage to the L3 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 6-1. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or GV_{DD} power pins.

Table 6-1. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L3VSEL Signal[1]	L3 Bus Input Threshold is Relative to:	Notes
0	1.8V	0	1.8V	(2)(3)
¬$\overline{\text{HRESET}}$	Not available	¬$\overline{\text{HRESET}}$	1.5V	(2)(4)
$\overline{\text{HRESET}}$	2.5V	$\overline{\text{HRESET}}$	2.5V	(2)
1	2.5V	1	2.5V	(2)

Notes:
1. Not implemented on PC7447.
2. Caution: The input threshold selection must agree with the OV_{DD}/GV_{DD} voltages supplied. See notes in "Absolute Maximum Ratings[1]" on page 11.
3. If used, pull-down resistors should be less than 250Ω
4. Applicable to L3 bus interface only. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

6.2 Thermal Characteristics

6.2.1 Package Characteristics

Table 6-2. Package Thermal Characteristics[1]

Symbol	Characteristic	Value		Unit
		PC7447 CBGA	PC7457 CBGA	
$R_{\theta JA}$[2][3]	Junction-to-ambient thermal resistance, natural convection	22	20	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	14	14	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board	16	15	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board	11	11	°C/W
$R_{\theta JB}$[5]	Junction-to-board thermal resistance	6	6	°C/W
$R_{\theta JC}$[6]	Junction-to-case thermal resistance	< 0.1	< 0.1	°C/W
	Coefficient of thermal expansion	6.8	6.8	ppm/°C

Notes:
1. See "Thermal Management Information" on page 15 for more details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

6.2.2 Package Thermal Characteristics for HCTE

Table 6-3 provides the package thermal characteristics for the PC7457, HCTE.

Table 6-3. Package Thermal Characteristics for HCTE Package

Characteristic	Symbol	Value	Unit
		PC755 HCTE	
Junction-to-bottom of balls(1)	$R\theta_J$	3.9	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board(1)(2)	$R\theta_{JMA}$	16.8	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	7.6	°C/W

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-6 with the board horizontal

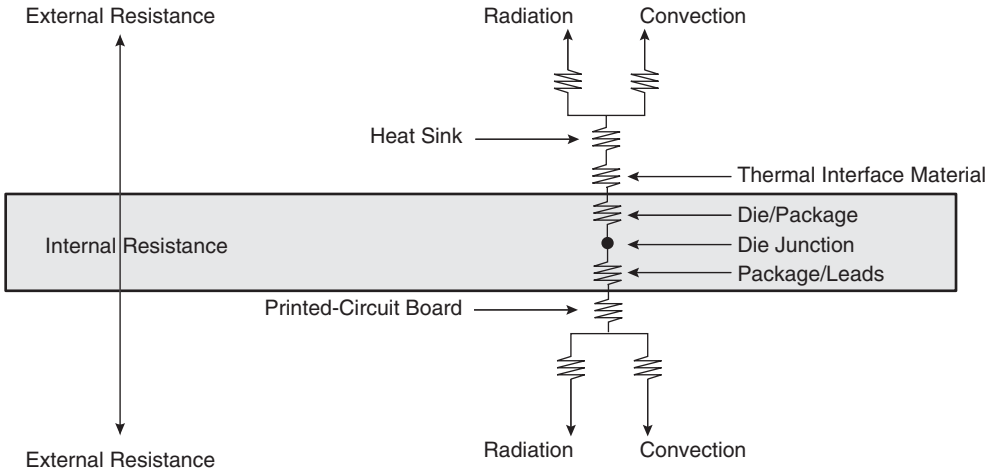
6.2.3 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 6-1 on page 13, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (actually top-of-die since silicon die is exposed) thermal resistance
- The die junction-to-ball thermal resistance

Figure 15-3 on page 55 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 6-2. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note the internal versus external package resistance.

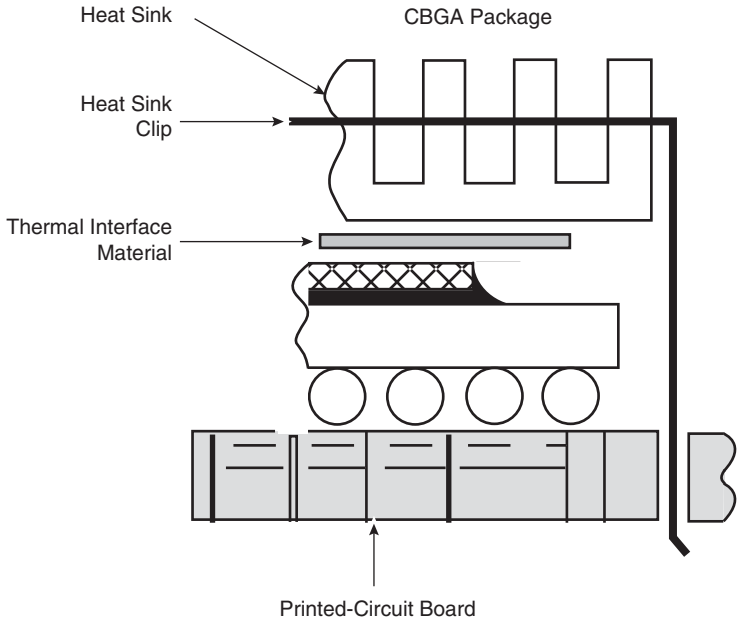
Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

6.2.4 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design – the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods – spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 15-2 on page 52); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. If a spring clip is used, the spring force should not exceed 10 pounds.

Figure 6-3. Package Exploded Cross-sectional View with Several Heat Sink Options



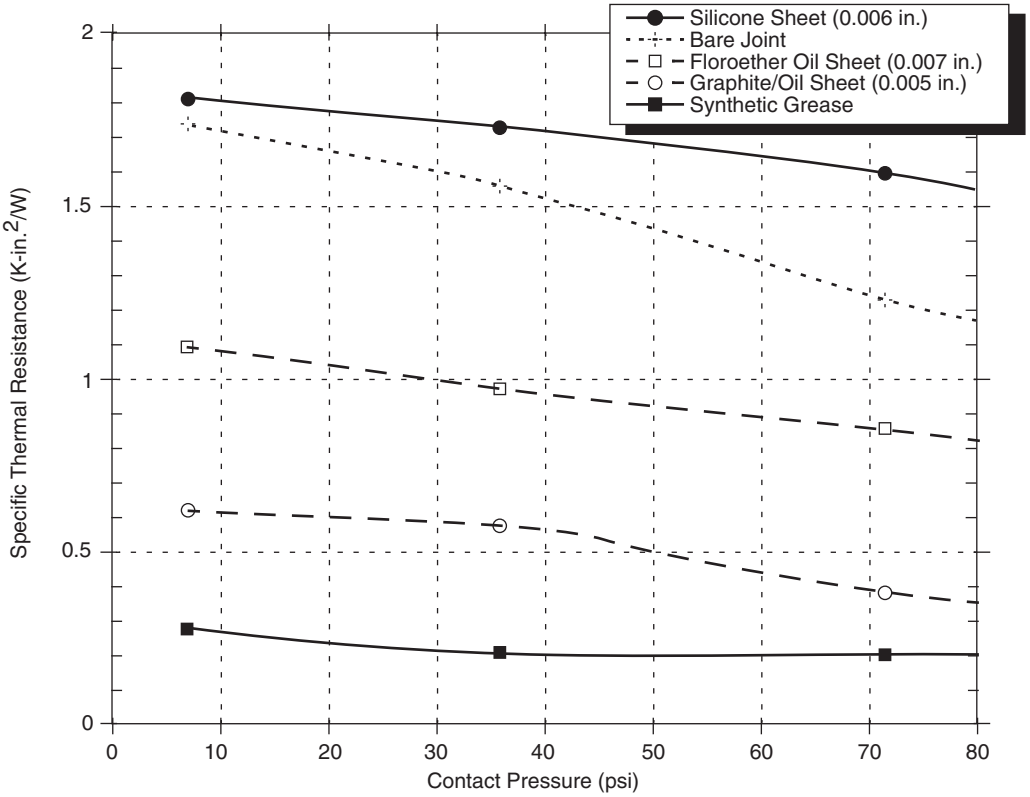
6.2.5 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-3 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure.

The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 15-2 on page 52). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the PC7457. Of course, the selection of any thermal interface material depends on many factors – thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 6-4. Thermal Performance of Select Thermal Interface Material



6.2.5.1 *Heat Sink Selection Example*

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_J is the die-junction temperature
T_I is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_J) should be maintained less than the value specified in "Recommended Operating Conditions(1)" on page 12. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40° C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10° C.

The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5° C/W. For example, assuming a Ta of 30° C, a Tr of 5° C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7W, the following expression for T_J is obtained:

Die-junction temperature: T_J = 30° C + 5° C + (0.1° C/W + 1.5° C/W + θ_{sa}) × 18.7W

For this example, a $R_{\theta sa}$ value of 2.1° C/W or less is required to maintain the die junction temperature below the maximum value of "Recommended Operating Conditions(1)" on page 12.

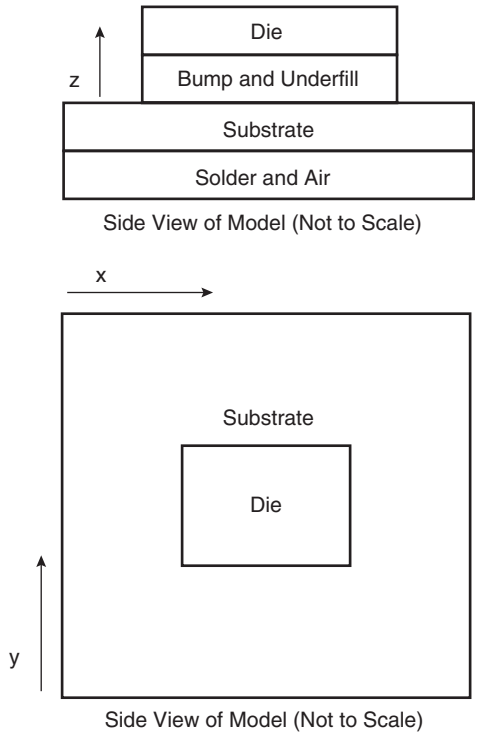
Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature – airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the PC7447 and PC7457 thermal model is shown in Figure 6-2 on page 14. Four volumes will be used to represent this device. Two of the volumes, solder ball, and air and substrate, are modeled using the package outline size of the package. The other two, die, and bump and underfill, have the same size as the die. The silicon die should be modeled 9.64 × 11 × 0.74 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 9.64 × 11 × 0.69 mm (or as a collapsed volume) with orthotropic material properties: 0.6W/(m × K) in the xy-plane and 2W/(m × K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm (PC7447) or 29 × 29 × 1.2 mm (PC7457), and this volume has 18W/(m × K) isotropic conductivity. The solder ball and air layer is modeled with the same horizontal dimensions as the substrate and is 0.9 mm thick. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034W/(m × K) in the xy-plane direction and 3.8W/(m × K) in the direction of the z-axis.

Figure 6-5. Recommended Thermal Model of PC7447 and PC7457

Conductivity	Value	Unit
Bump and Underfill		
k_x	0.6	W/(m x K)
k_y	0.6	
k_z	2	
Substrate		
k	18	
Solder Ball and Air		
k_x	0.034	
k_y	0.034	
k_z	3.8	



6.2.6 Power Consumption

Table 6-4. Power Consumption for PC7457

	Processor (CPU) Frequency				
Full-Power Mode	**600 MHz**	**1000 MHz**	**1000 MHz**	**1200 MHz**	**Unit**
Core Power Supply	1.1	1.1	1.3	1.3	
Typical(1)(2)	5.3	8.3	15.8	17.5	W
Maximum(1)(3)	7.9	11.5	22.0	24.2	W
Nap Mode					
Typical(1)(2)	1.3	1.3	5.2	5.2	W
Sleep Mode					
Typical(1)(2)	1.2	1.2	5.1	5.1	W
Deep Sleep Mode (PLL Disabled)					
Typical(1)(2)	1.1	1.1	5.0	5.0	W

Notes:
1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW
2. Typical power is an average value measured at the nominal recommended VDD (see "Recommended Operating Conditions(1)" on page 12) and 65° C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.

3. Maximum power is the average measured at nominal V_{DD} and maximum operating junction temperature (see "Recommended Operating Conditions(1)" on page 12) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

7. Electrical Characteristics

7.1 Static Characteristics

Table 7-1 provides the DC electrical characteristics for the PC7457.

Table 7-1. DC Electrical Specifications (see "Recommended Operating Conditions(1)" on page 12)

Symbol	Characteristic		Nominal Bus Voltage(1)	Min	Max	Unit
V_{IH}(2)	Input high voltage (all inputs including SYSCLK)		1.5	$GV_{DD} \times 0.65$	$GV_{DD} + 0.3$	V
V_{IH}			1.8	$OV_{DD}/GV_{DD} \times 0.65$	$OV_{DD}/GV_{DD} + 0.3$	V
V_{IH}			2.5	1.7	$OV_{DD}/GV_{DD} + 0.3$	V
V_{IL}(2)(6)	Input low voltage (all inputs including SYSCLK)		1.5	-0.3	$GV_{DD} \times 0.35$	V
V_{IL}			1.8	-0.3	$OV_{DD}/GV_{DD} \times 0.35$	V
V_{IL}			2.5	-0.3	0.7	V
I_{IN}(2)(3)	Input leakage current, $V_{IN} = GV_{DD}/OV_{DD}$		–	–	30	µA
I_{TSI}(2)(3)(4)	High-impedance (off-state) Leakage current, $V_{IN} = GV_{DD}/OV_{DD}$		–	–	30	µA
V_{OH}(6)	Output high voltage, $I_{OH} = -5$ mA		1.5	$OV_{DD}/GV_{DD} - 0.45$	–	V
V_{OH}			1.8	$OV_{DD}/GV_{DD} - 0.45$	–	V
V_{OH}			2.5	1.8	–	V
V_{OL}(6)	Output low voltage, $I_{OL} = 5$ mA		1.5	–	0.45	V
V_{OL}			1.8	–	0.45	V
V_{OL}			2.5	–	0.6	V
C_{IN}	Capacitance, $V_{IN} = 0V$, f = 1 MHz	L3 interface(5)	–	–	9.5	pF
		All other inputs(5)		–	8.0	pF

Notes:
1. Nominal voltages; see "Recommended Operating Conditions(1)" on page 12 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.
3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. Applicable to L3 bus interface only

7.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7457. After fabrication, functional parts are sorted by maximum processor core frequency as shown in section “Clock AC Specifications” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; See “Ordering Information” on page 59.

7.2.1 Clock AC Specifications

Table 7-2 provides the clock AC timing specifications as defined in Figure 7-1 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 7-2 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7457 will be a function of the AC timings of the PC7457, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 7-2.

Table 7-2. Clock AC Timing Specifications (See “Recommended Operating Conditions(1)” on page 12)

		Maximum Processor Core Frequency						
		600 MHz		867 MHz		1000 MHz		
		V_{DD} = 1.1V		V_{DD} = 1.1V		V_{DD} = 1.1V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	500	600	500	867	500	1000	MHz
f_{VCO}(1)	VCO frequency	1000	1200	1000	1733	1000	2000	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	ns
t_{KHKL}/t_{SYSCLK}(4)	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	–	–	%
	SYSCLK jitter(5)(6)	–	150	–	150	–	–	ps
	Internal PLL relock time(7)	–	100	–	100	–	–	µs

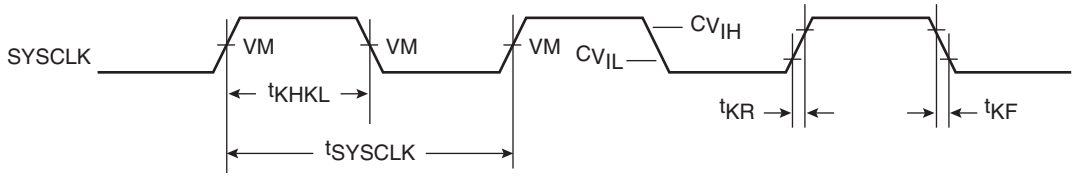
		Maximum Processor Core Frequency								
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	600	867	600	1000	600	1200	600	1267	MHz
f_{VCO}(1)	VCO frequency	1200	1733	1200	2000	1200	2400	1200	2534	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	–	1	ns

Symbol	Characteristic	Maximum Processor Core Frequency								Unit
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{KHKL}/t_{SYSCLK}[4]	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	40	60	%
	SYSCLK jitter[5][6]	–	±150	–	±150	–	±150	–	±150	ps
	Internal PLL relock time[7]	–	100	–	100	–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency and PLL (VCO) frequency don't exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in "Core Clocks and PLL Configuration" on page 47 for valid PLL_CFG[0:4] settings
2. Assumes lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4V to 1.4V.
4. Timing is guaranteed by design and characterization.
5. This represents total input jitter, short-term and long-term combined, and is guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 7-1 provides the SYSCLK input timing diagram.

Figure 7-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

7.2.2 Processor Bus AC Specifications

Table 7-3 provides the processor bus AC timing specifications for the PC7457 as defined in Figure 7-10 on page 33 and Figure 7-2 on page 23. Timing specifications for the L3 bus are provided in section "L3 Clock AC Specifications" on page 24.

Table 7-3. Processor Bus AC Timing Specifications[1] (at Recommended Operating Conditions, see page 12.)

Symbol[2]	Parameter	All Speed Grades			Unit
		V_{DD} = 1.1V	Min V_{DD} = 1.3V	Max	
	Input setup times:				
t_{AVKH}	A[0:35], AP[0:4]	2.0	1.8	–	
t_{DVKH}	D[0:63], DP[0:7]	2.0	1.8	–	
t_{IVKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1],	2.0	1.8	–	ns
t_{MVKH}[8]	BMODE[0:1], $\overline{BMODE}$[0:1], BVSEL, L3VSEL	2	1.8	–	
	Input hold times:				
t_{AXKH}	A[0:35], AP[0:4]	0	0	–	
t_{DXKH}	D[0:63], DP[0:7]	0	0	–	
t_{IXKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1]	0	0	–	ns
t_{MXKH}[8]	BMODE[0:1], $\overline{BMODE}$[0:1], BVSEL, L3VSEL	0	0	–	
	Output valid times: A[0:35], AP[0:4]				
t_{KHAV}	D[0:63], DP[0:7]	–	–	2	ns
t_{KHDV}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3],	–	–	2	
t_{KHOV}	$\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	–	–	2	
	Output hold times: A[0:35], AP[0:4]				
t_{KHAX}	D[0:63], DP[0:7]	0.5	0.5	–	ns
t_{KHDX}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3],	0.5	0.5	–	
t_{KHOX}	$\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	0.5	0.5	–	
t_{KHOE}	SYSCLK to output enable	0.5	0.5	–	ns
t_{KHOZ}	SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	–	–	3.5	ns
t_{KHTSPZ}[3][4][5]	SYSCLK to $\overline{TS}$ high impedance after precharge	–	–	1	t_{SYSCLK}
t_{KHARP}[3][5][6][7]	Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	–	–	1	t_{SYSCLK}
t_{KHARPZ}[3][5][6][7]	SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	–	–	2	t_{SYSCLK}

Notes: 1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 7-10 on page 33). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 7-3 on page 24. The nominal precharge width for $\overline{TS}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{TS}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 7-3 on page 24 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning the cycle of $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 7-2 on page 23 for sample timing.

Figure 7-2. Mode Input Timing Diagram

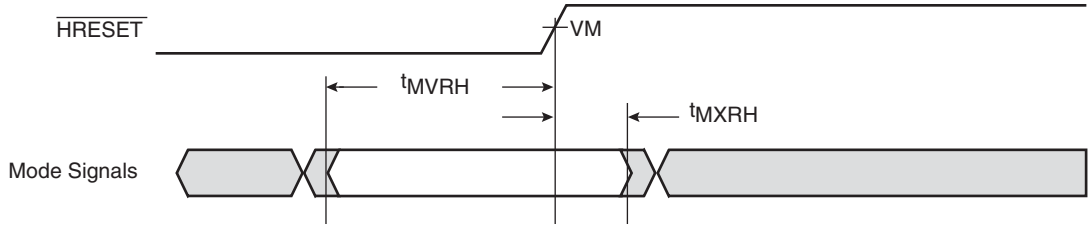
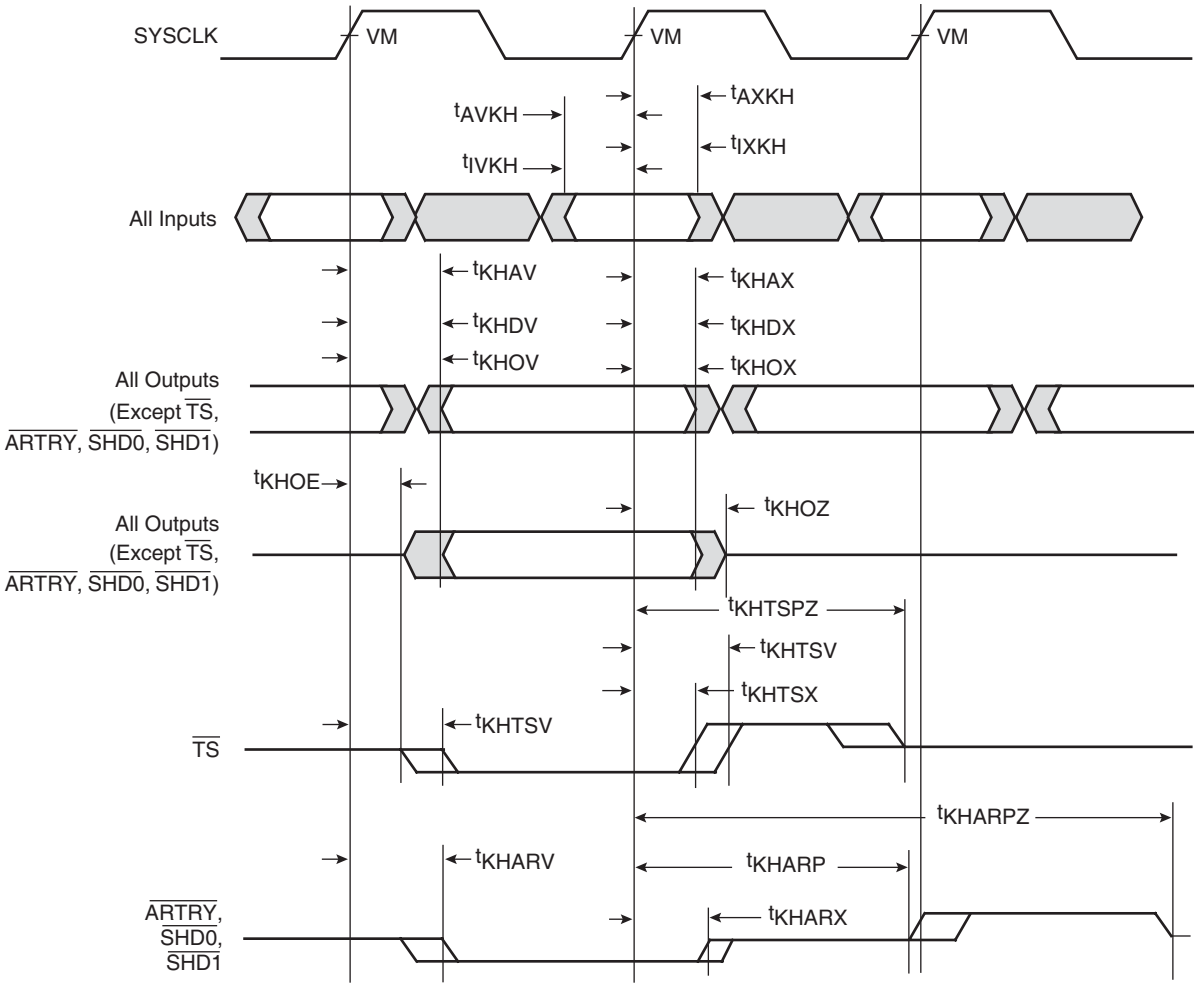


Figure 7-3 provides the input/output timing diagram for the PC7457.

Figure 7-3. Input/Output Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

7.2.3 L3 Clock AC Specifications

The L3_CLK frequency is programmed by the L3 configuration register core-to-L3 divisor ratio. See Table 15-1 on page 47 for example core and L3 frequencies at various divisors. Table 7-4 on page 25 provides the potential range of L3_CLK output AC timing specifications as defined in Figure 7-4 on page 26.

The maximum L3_CLK frequency is the core frequency divided by two. Given the high core frequencies available in the PC7457, however, most SRAM designs will be not be able to operate in this mode using current technology and, as a result, will select a greater core-to-L3 divisor to provide a longer L3_CLK period for read and write access to the L3 SRAMs. Therefore, the typical L3_CLK frequency shown in Table 7-4 is considered to be the practical maximum in a typical system. The maximum L3_CLK frequency for any application of the PC7457 will be a function of the AC timings of the PC7457, the AC timings for the SRAM, bus loading, and printed-circuit board trace length, and may be greater or less than the value given in Table 7-4.

Note that SYSCLK input jitter and L3_CLK[0:1] output jitter are already comprehended in the L3 bus AC timing specifications and do not need to be separately accounted for in an L3 AC timing analysis.

Clock skews, where applicable, do need to be accounted for in an AC timing analysis.Freescale is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 7-4. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 250 MHz or lower.

Table 7-4. L3_CLK Output AC Timing Specifications at Recommended Operating Conditions (see page 12)[6]

Symbol	Parameter	All Speed Grades						Unit
		Min	Typical	Max	Min	Typical	Max	
f_{L3_CLK}[1]	L3 clock frequency	–	200		–	250	–	MHz
t_{L3_CLK}[1]	L3 clock cycle time	–	5	–	–	4	–	ns
t_{CHCL}/t_{L3_CLK}[2]	L3 clock duty cycle	–	50	–	–	50	–	%
$t_{L3CSKW1}$[3]	L3 clock output-to-output skew (L3_CLK0 to L3_CLK1)	–	–	100	–	–	100	ps
$t_{L3CSKW2}$[4]	L3 clock output-to-output skew (L3_CLK[0:1] to L3_ECHO_CLK[1:3])	–	–	100	–	–	100	ps
	L3 clock jitter[5]	–	–	±75	–	–	±75	ps

Notes:
1. The maximum L3 clock frequency (and minimum L3 clock period) will be system dependent. See "L3 Clock AC Specifications" on page 24 for an explanation that this maximum frequency is not functionally tested at speed by Freescale. The minimum L3 clock frequency and period are f_{SYSCLK} and t_{SYSCLK}, respectively.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or Late Write SRAM. This parameter is critical to the read data signals because the processor uses the feedback loop to latch data driven from the SRAM, each of which drives data based on L3_CLK0 or L3_CLK1.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address, data and control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This is also comprehended in the AC timing specifications and need not be considered in the L3 timing analysis.
6. L3 I/O voltage mode must be configured by L3VSEL as described in Table 6-1 on page 13, and voltage supplied at GV_{DD} must match mode selected as specified in "Recommended Operating Conditions[1]" on page 12.