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Features

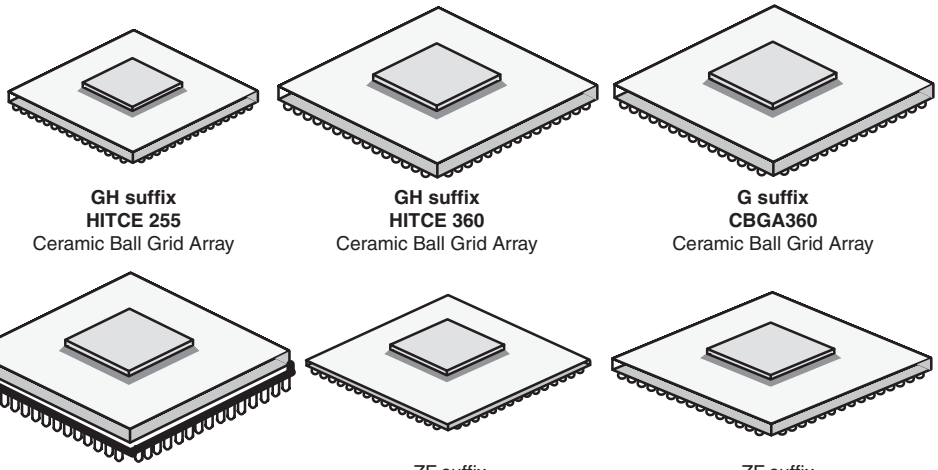
- **18.1SPECint95, Estimates 12.3 SPECfp95 at 400 MHz (PC755)**
- **15.7SPECint95, 9SPECfp95 at 350 MHz (PC745)**
- **733 MIPS at 400 MHz (PC755) at 641 MIPS at 350 MHz (PC745)**
- **Selectable Bus Clock (12 CPU Bus Dividers up to 10x)**
- **P_D Typical 6.4W at 400 MHz, Full Operating Conditions**
- **Nap, Doze and Sleep Modes for Power Savings**
- **Superscalar (3 Instructions per Clock Cycle) Two Instruction + Branch**
- **4 Beta Byte Virtual Memory, 4-GByte of Physical Memory**
- **64-bit Data and 32-bit Address Bus Interface**
- **32-KB Instruction and Data Cache**
- **Six Independent Execution Units**
- **Write-back and Write-through Operations**
- **f_{INT} max = 400 MHz (TBC)**
- **f_{BUS} max = 100 MHz**
- **Voltage I/O 2.5V/3.3V; Voltage Int 2.0V**

Description

The PC755 and PC745 PowerPC® microprocessors are high-performance, low-power, 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture, especially enhanced for embedded applications.

The PC755 and PC745 microprocessors differ only in that the PC755 features an enhanced, dedicated L2 cache interface with on-chip L2 tags. The PC755 is a drop-in replacement for the award winning PowerPC 750 microprocessor and is footprint and user software code compatible with the MPC7400 microprocessor with AltiVec technology. The PC745 is a drop-in replacement for the PowerPC 740 microprocessor and is also footprint and user software code compatible with the PowerPC 603e microprocessor. PC755/745 microprocessors provide on-chip debug support and are fully JTAG-compliant.

The PC745 microprocessor is pin compatible with the TSPC603e family.



GH suffix
HITCE 255
Ceramic Ball Grid Array

GH suffix
HITCE 360
Ceramic Ball Grid Array

G suffix
CBGA360
Ceramic Ball Grid Array

GS suffix
CI-CGA360
Ceramic Ball Grid Array with
Solder Column Interposer (SCI)

ZF suffix
PBGA255
Flip-Chip Plastic Ball Grid Array

ZF suffix
PBGA360
Flip-Chip Plastic Ball Grid Array

PowerPC 755/745 32-bit RISC Microprocessor

PC755/745

2138G–HIREL–05/06

Screening

This product is manufactured in full compliance with:

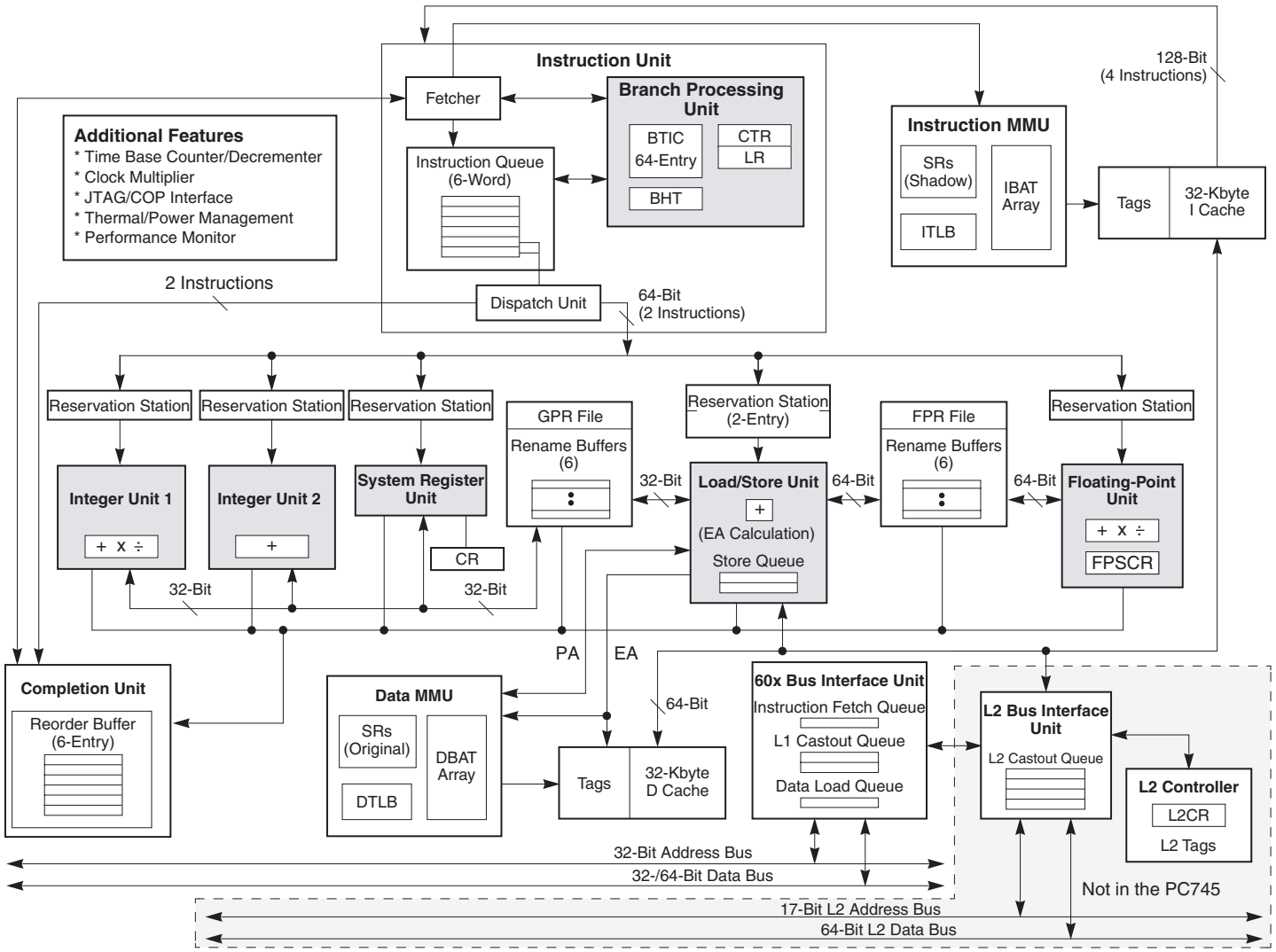
- HiTCE CBGA according to Atmel standards
- CBGA + CI-CGA + FC-PBGA up screenings based upon Atmel standards
- Full military temperature ranges (T_J = -55°C, +125°C)
- Industrial temperature ranges (T_J = -40°C, +110°C)

1. General Description

1.1 Simplified Block Diagram

The PC755 is targeted for low power systems and supports power management features such as doze, nap, sleep, and dynamic power management. The PC755 consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus.

Figure 1-1. PC755 Block Diagram



1.2 General Parameters

The following list provides a summary of the general parameters of the PC755:

Technology	0.22 µm CMOS, five-layer metal, 1 layer poly
Die size	6.61 mm x 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static Packages
PC745	Surface mount 255 Plastic Ball Grid Array (PBGA) Surface mount 255 Ceramic Ball Grid Array (Hi-TCE)
PC755	Surface mount 360 Plastic Ball Grid Array (PBGA) Surface mount 360 Ceramic Ball Grid Array (CI-CGA, CBGA, HiTCE)
Core power supply	2V ± 100 mV DC (nominal; some parts support core voltages down to 1.8V; see "Recommended Operating Conditions(1)" on page 16
I/O power supply	2.5V ± 100 mV DC or 3.3V ± 165 mV DC (input thresholds are configuration pin selectable)

1.3 Features

This section summarizes features of the PC755's implementation of the PowerPC architecture. Major features of the PC755 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry Branch History Table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 6 entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes

- Fixed Point Units (FXUs) that share 32 GPRs for Integer Operands
  - Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)-shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point Unit and a 32-entry FPR File
  - Support for IEEE-754 standard single and double precision floating point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/Store Unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and Little-endian byte addressing supported
  - Misaligned Little-endian supported
  - Level 1 Cache structure
  - 32K, 32 bytes line, 8-way set associative instruction cache (iL1)
  - 32K, 32 bytes line, 8-way set associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently used (PLRU) replacement
  - Copy-back or Write Through data cache (on a page per page basis)
  - Supports all PowerPC memory coherency modes
  - Non-Blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) Cache Interface (not implemented on PC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1-Mbyte 2-way set associative L2 cache support

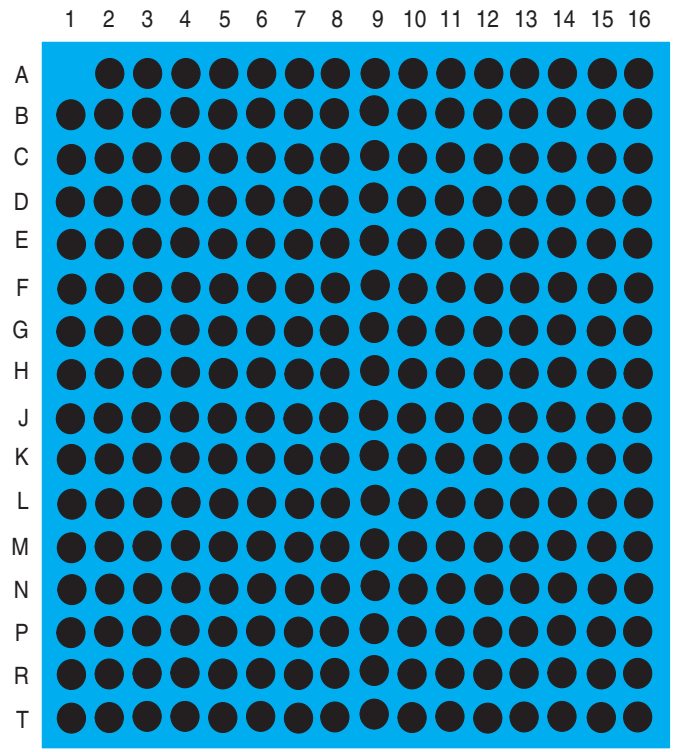
  - Copyback or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode.
  - 64 bytes (256K/512K) or 128 bytes (1M) sectored line size
  - Supports flow through (register-buffer) synchronous burst SRAMs, pipelined (register-register) synchronous burst SRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late-write synchronous burst SRAMs
  - L2 configurable to direct mapped SRAM interface or split cache/direct mapped or private memory
  - Core-to-L2 frequency divisors of 1, 1.5, 2, 2.5, and 3 supported
  - 64-bit data bus
  - Selectable interface voltages of 2.5V and 3.3V
  - Parity checking on both L2 address and data
- Memory Management Unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - 8 instruction BATs and 8 data BATs
  - 8 SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus Interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5V and 3.3V.
  - Parity checking on both address and data busses
- Power Management
  - Low-power design with thermal requirements very similar to PC740/750.
  - Selectable interface voltage of 1.8V/2.0V can reduce power in output buffers (compared to 3.3V)
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
- Integrated Thermal Management Assist Unit
  - One-ship thermal sensor and control logic
  - Thermal Management Interrupt for software regulation of junction temperature

2. Pin Assignments

Figure 2-1 (in part A) shows the pinout of the PC745, 255PBGA and HiTCE CBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Figure 2-1. Pinout of the PC745, 255 PBGA and HiTCE CBGA Packages as Viewed from the Top Surface

Part A



Not to Scale

Part B

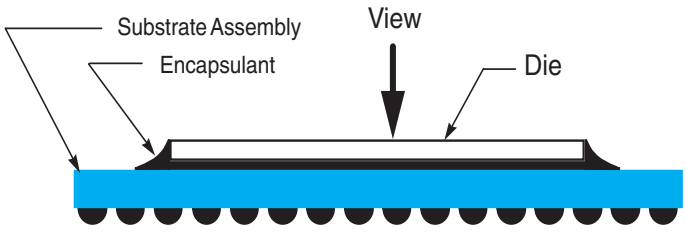
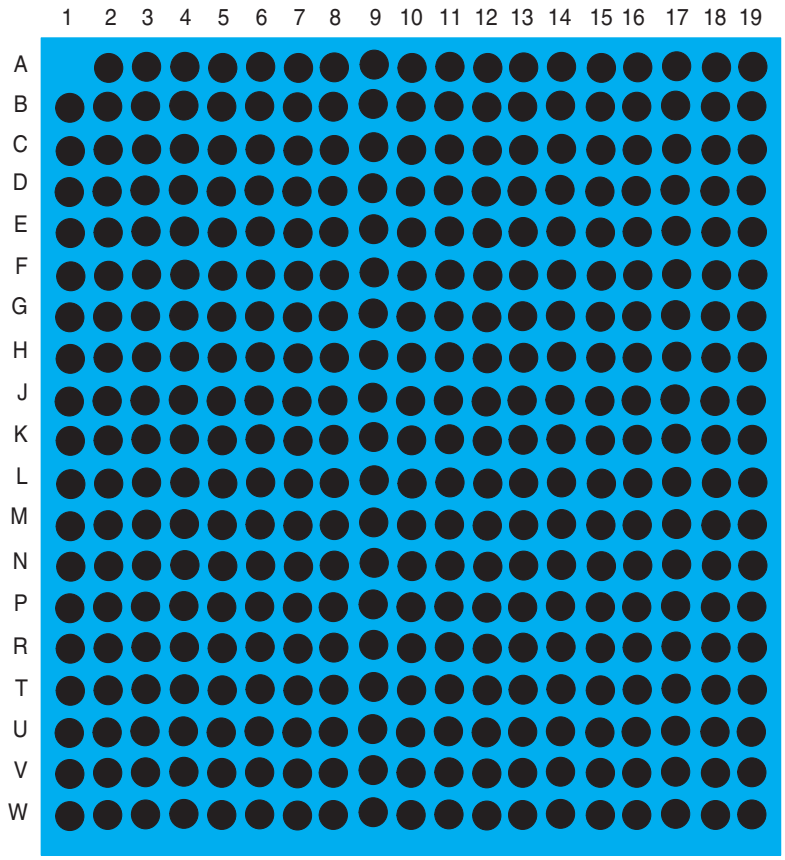


Figure 2-2 (in part A) shows the pinout of the PC755, 360 PBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

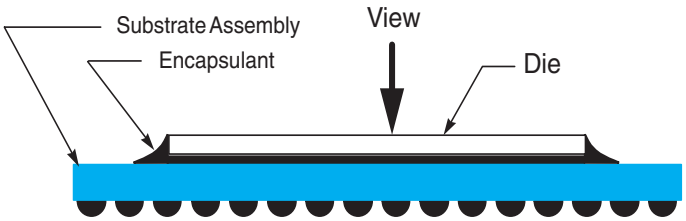
Figure 2-2. Pinout of the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages as Viewed from the Top Surface

Part A



Not to Scale

Part B



2.1 Pinout Listings

Table 2-1 provides the pinout listing for the PC745, 255 PBGA package.

Table 2-1. Pinout Listing for the PC745, 255 PBGA and HiTCE CBGA Packages

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	–	–
AACK	L2	Low	Input	–	–
ABB	K4	Low	I/O	–	–
AP[0-3]	C1, B4, B3, B2	High	I/O	–	–
ARTRY	J4	Low	I/O	–	–
AVDD	A10	–	–	2V	2V
BG	L1	Low	Input	–	–
BR	B6	Low	Output	–	–
BVSEL[3][4][5]	B1	High	Input	GND	3.3V
CI	E1	Low	Output	–	–
CKSTP_IN	D8	Low	Input	–	–
CKSTP_OUT	A6	Low	Output	–	–
CLK_OUT	D7	–	Output	–	–
DBB	J14	Low	I/O	–	–
DBG	N1	Low	Input	–	–
DBDIS	H15	Low	Input	–	–
DBWO	G4	Low	Input	–	–
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	–	–
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	–	–
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	–	–
DRTRY	G16	Low	Input	–	–
GBL	F1	Low	I/O	–	–
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12				
$\overline{\text{HRESET}}$	A7	Low	Input	–	–
INT	B15	Low	Input	–	–
L1_TSTCLK[2]	D11	High	Input	–	–
L2_TSTCLK[2]	D12	High	Input	–	–
LSSD_MODE[2]	B10	Low	Input	–	––

Table 2-1. Pinout Listing for the PC745, 255 PBGA and HiTCE CBGA Packages (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
MCP	C13	Low	Input	–	–
NC (No-Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	–	–	–	–
OVDD	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	–	–	1.8V/2.0V	3.3V
PLL_CFG[0-3]	A8, B9, A9, D9	High	Input	–	–
$\overline{\text{QACK}}$	D3	Low	Input	–	–
QREQ	J3	Low	Output	–	–
RSRV	D1	Low	Output	–	–
SMI	A16	Low	Input	–	–
SRESET	B14	Low	Input	–	–
SYSCLK	C9	–	Input	–	–
TA	H14	Low	Input	–	–
TBEN	C2	High	Input	–	–
TBST	A14	Low	I/O	–	–
TCK	C11	High	Input	–	–
TDI[5]	A11	High	Input	–	–
TDO	A12	High	Output	–	–
TEA	H13	Low	Input	–	–
TLBISYNC	C4	Low	Input	–	–
TMS[5]	B11	High	Input	–	–
$\overline{\text{TRST}}$[5]	C10	Low	Input	–	–
TS	J13	Low	I/O	–	–
TSIZ[0-2]	A13, D10, B12	High	Output	–	–
TT[0-4]	B13, A15, B16, C14, C15	High	I/O	–	–
WT	D2	Low	Output	–	–
V_{DD} 2	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	–	–	2V	2V
VOLTDET[6]	F3	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals and V_{DD} supplies power to the processor core and the PLL (after filtering to become AVDD). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 5-1 on page 15 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see "Absolute Maximum Ratings[1]" on page 14.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. Uses one of 15 existing no-connects in PC745's 255-BGA package.
5. Internal pull up on die.
6. Internally tied to GND in the PC745 255-BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

Table 2-2 provides the pinout listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8]

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	–	–
$\overline{\text{AACK}}$	N3	Low	Input	–	–
$\overline{\text{ABB}}$	L7	Low	I/O	–	–
AP[0-3]	C4, C5, C6, C7	High	I/O	–	–
$\overline{\text{ARTRY}}$	L6	Low	I/O	–	–
AVDD	A8	-	-	2V	2V
$\overline{\text{BG}}$	H1	Low	Input	–	–
$\overline{\text{BR}}$	E7	Low	Output	–	–
BVSEL[3][5][6]	W1	High	Input	GND	3.3V
$\overline{\text{CI}}$	C2	Low	Output	–	–
CKSTP_IN	B8	Low	Input	–	–
CKSTP_OUT	D7	Low	Output	–	–
CLK_OUT	E3	–	Output	–	–
$\overline{\text{DBB}}$	K5	Low	I/O	–	–
$\overline{\text{DBDIS}}$	G1	Low	Input	–	–
$\overline{\text{DBG}}$	K1	Low	Input	–	–
$\overline{\text{DBWO}}$	D1	Low	Input	–	–
DH[0-31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	–	–
DL[0-31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	–	–
DP[0-7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	–	–
$\overline{\text{DRTRY}}$	H6	Low	Input	–	–
$\overline{\text{GBL}}$	B1	Low	I/O	–	–
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	–	–	GND	GND
$\overline{\text{HRESET}}$	B6	Low	Input	–	–
$\overline{\text{INT}}$	C11	Low	Input	–	–
L1_TSTCLK[2]	F8	High	Input	–	–
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	–	–

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
L2AVDD	L13	–	–	2V	2V
$\overline{\text{L2CE}}$	P17	Low	Output	–	–
L2CLKOUTA	N15	–	Output	–	–
L2CLKOUTB	L16	–	Output	–	–
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	–	–
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	–	–
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	–	–	1.8V/2V	3.3V
L2SYNC_IN	L14	–	Input	–	–
L2SYNC_OUT	M14	–	Output	–	–
L2_TSTCLK[2]	F7	High	Input	–	–
L2VSEL[1][3][5][6]	A19	High	Input	GND	3.3V
$\overline{\text{L2WE}}$	N16	Low	Output	–	–
L2ZZ	G17	High	Output	–	–
$\overline{\text{LSSD\_MODE}}$[2]	F9	Low	Input	–	–
$\overline{\text{MCP}}$	B11	Low	Input	–	–
NC (No-Connect)	B3, B4, B5, W19, K9, K11[4], K19[4]	–	–	–	–
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	–	–	1.8V/2V	3.3V
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input	–	–
$\overline{\text{QACK}}$	B2	Low	Input	–	–
$\overline{\text{QREQ}}$	J3	Low	Output	–	–
$\overline{\text{RSRV}}$	D3	Low	Output	–	–
$\overline{\text{SMI}}$	A12	Low	Input	–	–
$\overline{\text{SRESET}}$	E10	Low	Input	–	–
SYSCLK	H9	–	Input	–	–
$\overline{\text{TA}}$	F1	Low	Input	–	–
TBEN	A2	High	Input	–	–
$\overline{\text{TBST}}$	A11	Low	I/O	–	–
TCK	B10	High	Input	–	–
TDI[6]	B7	High	Input	–	–
TDO	D9	High	Output	–	–

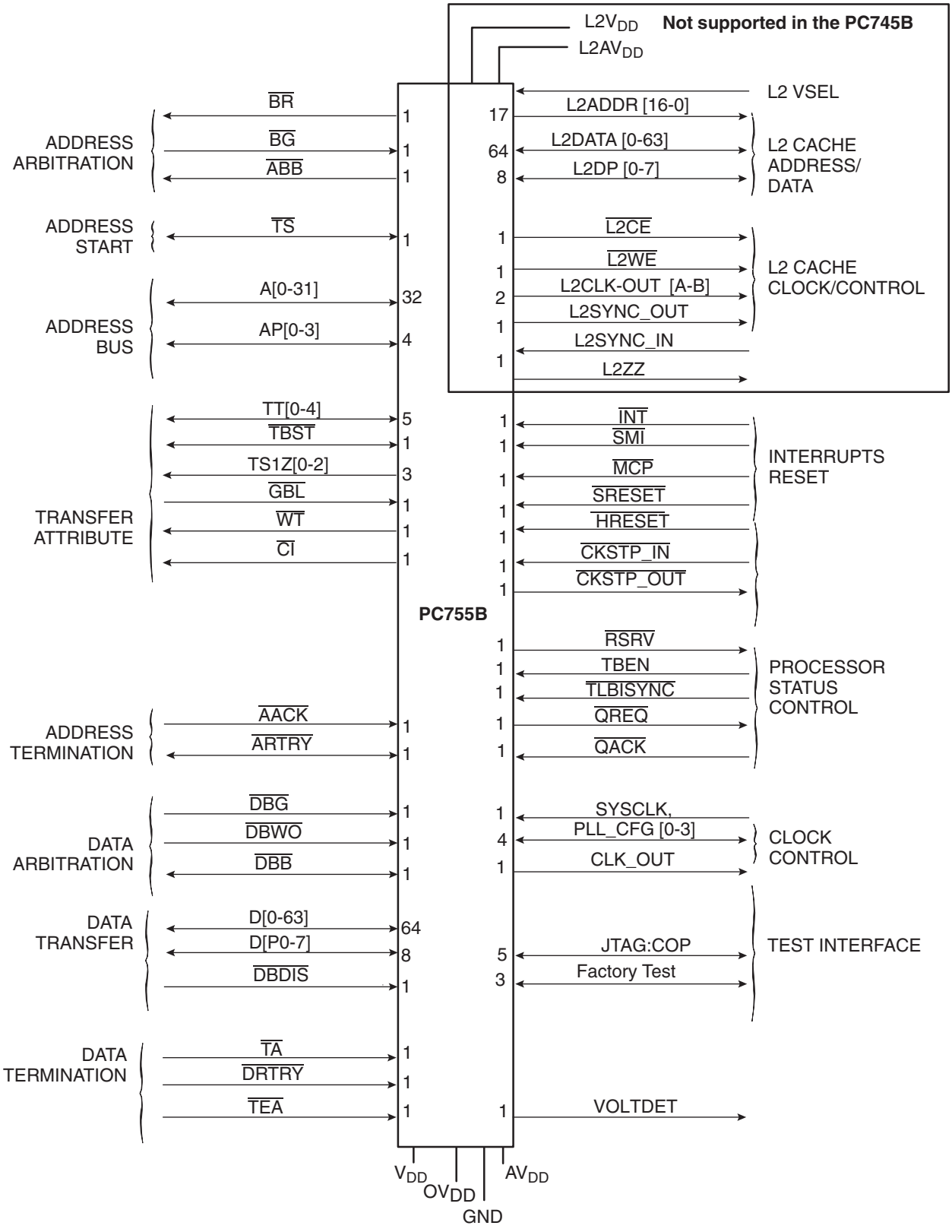
Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
$\overline{\text{TEA}}$	J1	Low	Input	–	–
$\overline{\text{TLBISYNC}}$	A3	Low	Input	–	–
TMS[6]	C8	High	Input	–	–
$\overline{\text{TRST}}$[6]	A10	Low	Input	–	–
$\overline{\text{TS}}$	K7	Low	I/O	–	–
TSIZ[0-2]	A9, B9, C9	High	Output	–	–
TT[0-4]	C10, D11, B12, C12, F11	High	I/O	–	–
$\overline{\text{WT}}$	C3	Low	Output	–	–
VDD	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	–	–	2V	2V
VOLTDET[7]	K13	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0-16], L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 5-1 on page 15 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see "Recommended Operating Conditions[1]" on page 16.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of 9 existing no-connects in PC750's 360-BGA package.
6. Internal pull up on die.
7. Internally tied to $L2OV_{DD}$ in the PC755 360-BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.
8. This is different from the PC745 255-BGA package.

3. Signal Description

Figure 3-1. PC755 Microprocessor Signal Groups



4. Detailed Specifications

This specification describes the specific requirements for the microprocessor PC755, in compliance with Atmel Grenoble standard screening.

5. Applicable Documents

1) MIL-STD-883: Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

Depending on the package, the terminal connections is shown in Table 2-1 on page 8, Table 2-2 on page 10 and Figure 3-1 on page 13.

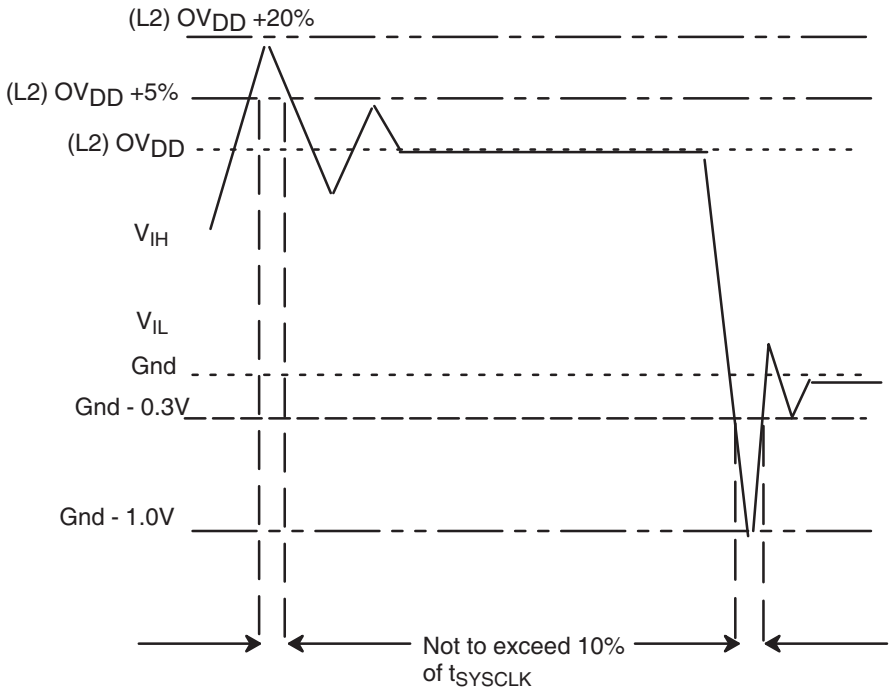
5.1.2 Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage[4]		V_{DD}	-0.3 to 2.5	V
PLL supply voltage[4]		AV_{DD}	-0.3 to 2.5	V
L2 DLL supply voltage[4]		$L2AV_{DD}$	-0.3 to 2.5	V
Processor bus supply voltage[3]		OV_{DD}	-0.3 to 3.6	V
L2 bus supply voltage[3]		$L2OV_{DD}$	-0.3 to 3.6	V
Input voltage	Processor bus[2][5]	V_{IN}	-0.3 to OV_{DD} + 0.3V	V
	L2 Bus[2][5]	V_{IN}	-0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{IN}	-0.3 to 3.6	V
Storage temperature range		T_{STG}	-55/+150	°C

Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions[1]" on page 16. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3V for up to 20 ms, or by 2.5V for up to 40 ms. Excursions beyond 3.3V or 40 ms are not supported.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0V for up to 20 ms, or by 0.7V for up to 40 ms. Excursions beyond 1.0V or 40 ms are not supported.
5. This is a DC specifications only. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5-1 on page 15.

Figure 5-1 shows the allowable undershoot and overshoot voltage on the PC755 and PC745.

Figure 5-1. Overshoot/Undershoot Voltage



The PC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC755 core voltage must always be provided at nominal 2.0V (see "Recommended Operating Conditions(1)" on page 16 for actual recommended core voltage). Voltage to the L2 I/Os and Processor Interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 5-1. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 5-1 describes the input threshold voltage setting.

Table 5-1. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5V/3.3V	1	2.5V/3.3V

Notes: 1. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, contact your local Atmel sales office.

5.1.3 Recommended Operating Conditions[1]

Characteristic		Symbol	Recommended Value				Unit
			300 MHz, 350 MHz		400 MHz		
			Min	Max	Min	Max	
Core supply voltage[3]		V_{DD}	1.80	2.10	1.90	2.10	V
PLL supply voltage[3]		AV_{DD}	1.80	2.10	1.90	2.10	V
L2 DLL supply voltage[3]		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V
Processor bus supply voltage[2][4][5]	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V
			3.135	3.465	3.135	3.465	V
L2 bus supply voltage[2][4][5]	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V
			3.135	3.465	3.135	3.465	V
Input voltage	Processor bus	V_{IN}	GND	OV_{DD}	GND	OV_{DD}	V
	L2 Bus	V_{IN}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V
	JTAG Signals	V_{IN}	GND	OV_{DD}	GND	OV_{DD}	V
Die-junction temperature	Military temperature range	T_J	-55	125	-55	125	°C
	Industrial temperature	T_J	-40	110	-40	110	°C

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support.
3. 2.0V nominal.
4. 2.5V nominal.
5. 3.3V nominal.

6. Thermal Characteristics

6.1 Package Characteristics

Table 6-1 provides the package thermal characteristics for the PC755.

Table 6-1. Package Thermal Characteristics

Characteristic	Symbol	Value			Unit
		PC755 CBGA	PC755 PBGA	PC745 PBGA	
Junction-to-ambient thermal resistance, natural convection[()(2)]	$R\theta_{JA}$	24	31	34	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board[()(3)]	$R\theta_{JMA}$	17	25	26	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board[()(3)]	$R\theta_{JMA}$	18	25	27	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board[()(3)]	$R\theta_{JMA}$	14	21	22	°C/W
Junction-to-board thermal resistance[(4)]	$R\theta_{JB}$	8	17	17	°C/W
Junction-to-case thermal resistance[(5)]	$R\theta_{JC}$	< 0.1	< 0.1	< 0.1	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R\theta_{JC}$ for the part is less than 0.1°C/W.

Note: Refer to Section 6.1.3 "Thermal Management Information" on page 19 for more details about thermal management.

6.1.1 Package Thermal Characteristics for HiTCE

Table 6-2 provides the package thermal characteristics for the PC755, HiTCE.

Table 6-2. Package Thermal Characteristics for HiTCE Package

Characteristic	Symbol	Value		Unit
		PC755 HiTCE	PC745 HiTCE	
Junction-to-bottom of balls[(1)]	$R\theta_J$	6.8	6.5	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R\theta_{JMA}$	20.7[(1)(2)]	20.9[(1)(4)]	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.0	10.2[(3)]	°C/W

Notes:
1. Simulation, no convection air flow
2. Per JEDEC JESD51-6 with the board horizontal
3. Per JEDEC JESD51-8
4. Per JEDEC JESD51-2 with the board horizontal

Table 6-3. Package Thermal Characteristics for CI-CGA

Characteristic	Symbol	Value	Unit
		PC755 CI-CGA	
Junction to board thermal resistance	$R\theta_{JB}$	8.42	°C/W

The board designer can choose between several types of heat sinks to place on the PC755. There are several commercially-available heat sinks for the PC755 provided by the following vendors.

For the exposed-die packaging technology, shown in "Recommended Operating Conditions(1)" on page 16, the intrinsic conduction thermal resistance paths are as follows:

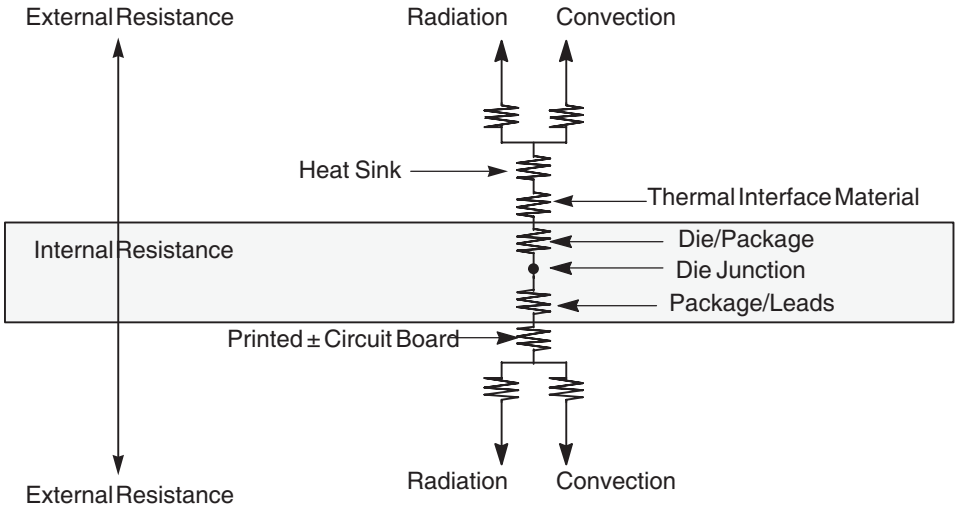
- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 6-1 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Figure 6-1. C4 Package with Head Sink Mounted to a Printed-circuit Board



Note the internal versus external package resistance.

6.1.2 Thermal Management Assistance

The PC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 6-4. More information on the use of this feature is given in the Freescale PC755 RISC Microprocessor User's manual.

Table 6-4. Thermal Sensor Specifications at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 16)

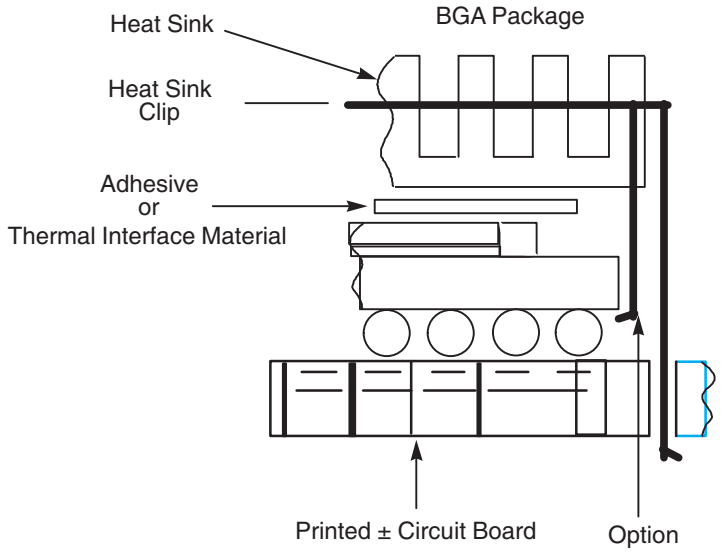
Characteristic	Min	Max	Unit
Temperature range(1)	0	127	°C
Comparator settling time(2)(3)	20	–	s
Resolution(3)	4	–	°C
Accuracy(3)	-12	+12	°C

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, "Programming the Thermal Assist Unit in the PC750 Microprocessor".
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

6.1.3 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design-the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 6-2. This spring force should not exceed 5.5 pounds of force.

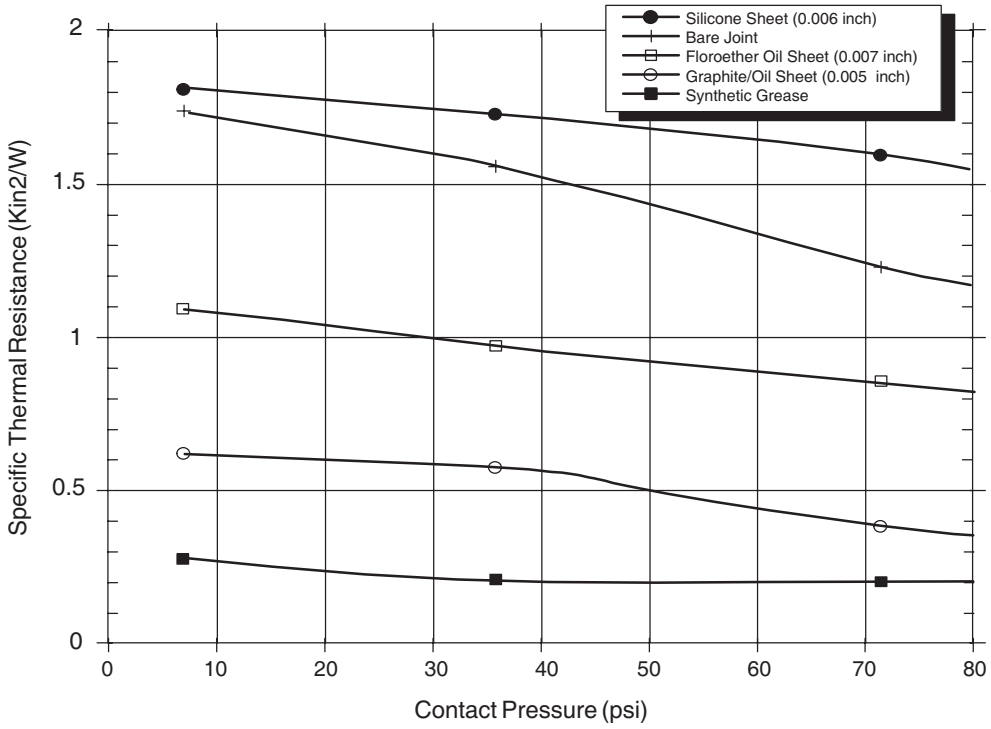
Figure 6-2. Package Exploded Cross-Sectional View with Several Heat Sink Options



Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6.1.4 Adhesives and Thermal Interface Materials

Figure 6-3. Thermal Performance of Select Thermal Interface Material



A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-3 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 6-2 on page 19). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

6.1.5 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

Where:

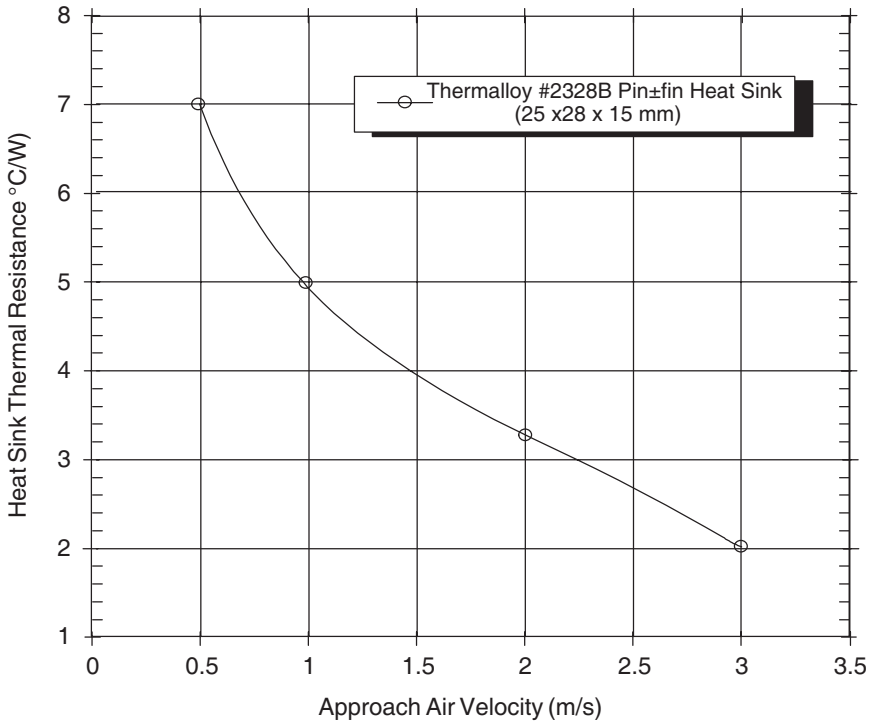
T_J is the die-junction temperature
T_A is the inlet cabinet ambient temperature
T_R is the air temperature rise within the computer cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the adhesive or interface material thermal resistance
θ_{SA} is the heat sink base-to-ambient thermal resistance
P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained less than the value specified in "Recommended Operating Conditions(1)" on page 16. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a $T_{R\ of\ 5}$°C, a CBGA package θ_{JC} = 0.03, and a power consumption (P_D) of 5.0 watts, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 6-4.

Figure 6-4. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity



Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W$

resulting in a die-junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature — airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

7. Power consideration

7.1 Power management

The PC755 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows:

- Full-power: This is the default power state of the PC755. The PC755 is fully powered and the internal functional units operate at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- Doze: All the functional units of the PC755 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the PC755 into the full-power state. The PC755 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC755 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input (MCP). A return to full-power state from a nap state takes only a few processor clock cycles.

When the processor is in nap mode, if $\overline{QACK}$ is negated, the processor is put in doze mode to support snooping.

- Sleep: Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PPL and SUSCLK. Returning the PC755 to the full-power state requires the enabling of the PPL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset, or a machine check input (MCP) signal after the time required to relock the PPL.

7.2 Power Dissipation

Table 7-1. Power Consumption for PC755

	Processor (CPU) Frequency			Unit
	300 MHz	350 MHz	400 MHz	
Full-Power Mode				
Typical[1][3][4]	3.1	3.6	5.4	W
Maximum[1][2]	4.5	6	8	W
Doze Mode				
Maximum[1][2][4]	1.8	2	2.3	W
Nap Mode				
Maximum[1][2][4]	1	1	1	W
Sleep Mode				
Maximum[1][2][4]	550	550	550	mW
Sleep Mode-PLL and DLL Disabled				
Maximum[1][2]	510	510	510	mW

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically < 10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see "Recommended Operating Conditions[1]" on page 16) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see "Recommended Operating Conditions[1]" on page 16) and 65×C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

8. Electrical Characteristics

8.1 Static Characteristics

Table 8-1. DC Electrical Specifications at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 16)

Characteristic	Nominal bus Voltage(1)	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSLCK)(2)(3)	2.5	V_{IH}	1.6	$(L2)OV_{DD}$ + 0.3	V
	3.3	V_{IH}	2	$(L2)OV_{DD}$ + 0.3	V
Input low voltage (all inputs except SYSLCK)(2)	2.5	V_{IL}	-0.3	0.6	V
	3.3	V_{IL}	-0.3	0.8	V
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V
SYSCLK input low voltage	2.5	KV_{IL}	-0.3	0.4	V
	3.3	KV_{IL}	-0.3	0.4	V
Input leakage current, (2)(3) $V_{IN} = L2OV_{DD}/OV_{DD}$		I_{in}	–	10	µA
Hi-Z (off-state) leakage current, (2)(3)(5) $V_{IN} = L2OV_{DD}/OV_{DD}$		I_{TSI}	–	10	µA
Output high voltage, I_{OH} = -6 mA	2.5	V_{OH}	1.7	–	V
	3.3	V_{OH}	2.4	–	V
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	–	0.45	V
	3.3	V_{OL}	–	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz (3)(4)		C_{in}	–	5	pF

Notes:
1. Nominal voltages; See "Recommended Operating Conditions(1)" on page 16.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).

8.2 Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in "Clock AC Specifications" on page 25 and tested for conformance to the AC specifications for that frequency. These specifications are for 275, 300, 333 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0-3] signals. Parts are sold by maximum processor core frequency.

8.2.1 Clock AC Specifications

Table 8-2 provides the clock AC timing specifications as defined in "Absolute Maximum Ratings[1]" on page 14.

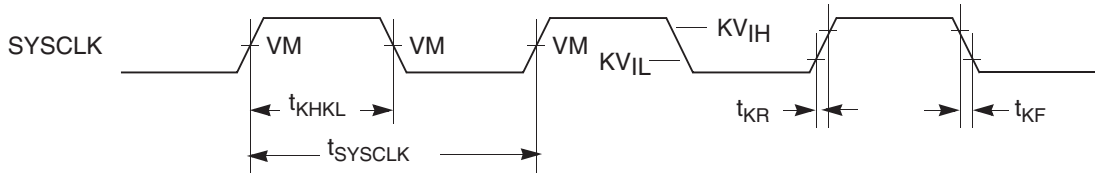
Table 8-2. Clock AC Timing Specifications at Recommended Operating Conditions (See "Recommended Operating Conditions[1]" on page 16)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit
		300 MHz		350 MHz		400 MHz		
		Min	Max	Min	Max	Min	Max	
Processor frequency[1]	f_{core}	200	300	200	350	200	400	MHz
VCO frequency[1]	f_{VCO}	400	600	400	700	400	800	MHz
SYSCLK frequency[1]	f_{SYSCLK}	25	100	25	100	25	100	MHz
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns
SYSCLK rise and fall time[2]	t_{KR} & t_{KF}	–	2	–	2	–	2	ns
	t_{KR} & t_{KF}	–	1.4	–	1.4	–	1.4	ns
SYSCLK duty cycle measured at $OV_{DD}/2$[3]	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%
SYSCLK jitter[3][4]		–	150	–	150	–	150	ps
Internal PLL relock time[3][5]		–	100	–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in Table 9-1 on page 39," for valid PLL_CFG[0-3] settings
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1v/ns is equivalent to a 2ns maximum rise/fall time measured at 0.4V and 2.4V or a rise/fall time of 1ns measured at 0.4V to 1.4V.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter – short term and long term combined and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 8-1 provides the SYSCLK input timing diagram.

Figure 8-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

8.2.1.1 *Processor Bus AC Specifications*

Table 8-3 on page 26 provides the processor bus AC timing specifications for the PC755 as defined in Figure 8-2 on page 26 and Figure 8-4 on page 28. Timing specifications for the L2 bus are provided in "L2 Clock AC Specifications" on page 28.