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Datasheet - *Preliminary Specification*

Features

- 6.6 SPECint95, 5.5 SPECfp95 at 266 MHz (Estimated)
- Superscalar 603e Core
- Integer Unit (IU), Floating-Point Unit (FPU) (User Enabled or Disabled), Load/Store Unit (LSU), System Register Unit (SRU), and a Branch Processing Unit (BPU)
- 16-Kbyte Instruction Cache
- 16-Kbyte Data Cache
- Lockable L1 Caches - Entire Cache or on a Per-way Basis up to 3 of 4 Ways
- Dynamic Power Management
- High-bandwidth Bus (32/64 bits Data Bus) to DRAM
- Supports 1-Mbyte to 1-Gbyte DRAM Memory
- 32-bit PCI Interface Operating up to 66 MHz
- PCI 2.1-compliant, 5.0V Tolerance
- Fint Max = 200 MHz
- FBus Max = 66 MHz

Description

The PC8240 combines a Power Architecture™ 603e core microprocessor with a PCI bridge. The PC8240's PCI support will allow system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces. The PC8240 also integrates a highperformance memory controller which supports various types of DRAM and ROM. The PC8240 is the first of a family of products that provides system level support for industry standard interfaces with a Power Architecture microprocessor core.

The peripheral logic integrates a PCI bridge, memory controller, DMA controller, EPIC interrupt controller, I₂O controller, and a two-wire interface controller. The 603e core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

The PC8240 contains an internal peripheral logic bus that interfaces the 603e core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade off performance for power consumption. The 603e core is clocked from a separate PLL, which is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies, while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the PC8240's memory space are passed to the processor bus for snooping purposes when snoop mode is enabled.

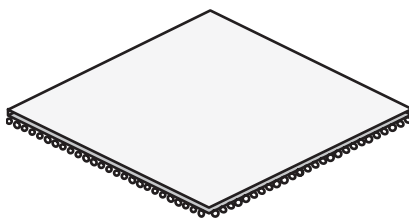
Visit our website: www.e2v.com
for the latest version of the datasheet

The PC8240's features serve a variety of embedded applications. In this way, the 603e core and peripheral logic remain general-purpose. The PC8240 can be used as either a PCI host or an agent controller.

Screening/Quality/Packaging

This product is manufactured in full compliance with:

- Upscreening based upon e2v standards
- Industrial temperature range
($T_c = -40^\circ\text{C}$, $T_c = +110^\circ\text{C}$)
($T_c = -40^\circ\text{C}$, $T_c = +125^\circ\text{C}$): ZD3 suffix
- Core power supply:
2.5 \pm 5 % V (L-Spec for 200 MHz)
- I/O power supply: 3.0V to 3.6V
- 352 Tape Ball Grid Array (TBGA)



TP suffix

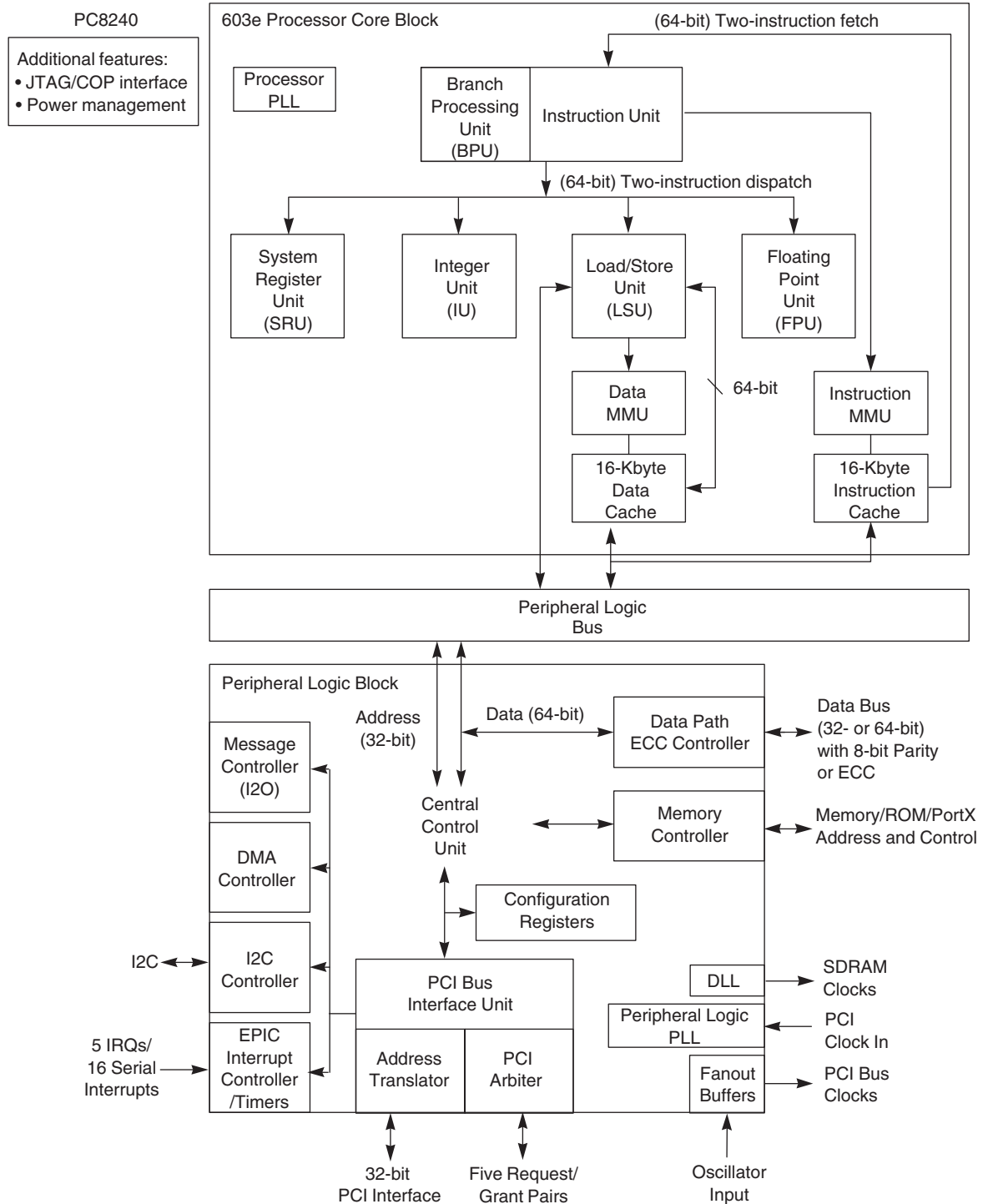
TBGA352
Tape Ball Grid Array

1. General Description

1.1 Block Diagram

The PC8240 integrated processor is comprised of a peripheral logic block and a 32-bit superscalar Power Architecture 603e core, as shown in Figure 1-1.

Figure 1-1. Block Diagram



1.2 Pinout Listing

Table 1-1 provides the pinout listing for the PC8240, 352 TBGA package.

Table 1-1. PC8240 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{C/BE}[0 - 3]$	A25 F23 K23 P25	I/O	OVdd	DRV_PCI	(6)(15)
\overline{DEVSEL}	H26	I/O	OVdd	DRV_PCI	(8)(15)
\overline{FRAME}	J24	I/O	OVdd	DRV_PCI	(8)(15)
\overline{IRDY}	K25	I/O	OVdd	DRV_PCI	(8)(15)
\overline{LOCK}	J26	Input	OVdd	–	(8)
AD[0 – 31]	C22 D22 B22 B23 D19 B24 A24 B26 A26 C26 D25 D26 E23 E25 E26 F24 L26 L25 M25 M26 N23 N25 N26 R26 R25 T26 T25 U23 U24 U26 U25 V25	I/O	OVdd	DRV_PCI	(6)(15)
PAR	G25	I/O	OVdd	DRV_PCI	(15)
$\overline{GNT}[0 - 3]$	V26 W23 W24 W25	Output	OVdd	DRV_PCI	(6)(15)
$\overline{GNT4/DA5}$	W26	Output	OVdd	DRV_PCI	(7)(15)
$\overline{REQ}[0 - 3]$	AB26 AA25 AA26 Y25	Input	OVdd	–	(6)(12)
$\overline{REQ4/DA4}$	Y26	Input	OVdd	–	(12)
\overline{PERR}	G26	I/O	OVdd	DRV_PCI	(8)(15)(18)
\overline{SERR}	F26	I/O	OVdd	DRV_PCI	(8)(15)(16)
\overline{STOP}	H25	I/O	OVdd	DRV_PCI	(8)(15)
\overline{TRDY}	K26	I/O	OVdd	DRV_PCI	(8)(15)
\overline{INTA}	AC26	Output	OVdd	DRV_PCI	(15)(16)
IDSEL	P26	Input	OVdd	–	–
Memory Interface Signals					
MDL[0 – 31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GVdd	DRV_MEM_DATA	(5)(6)(13)
MDH[0 – 31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GVdd	DRV_MEM_DATA	(6)(13)
$\overline{CAS}/DQM[0 - 7]$	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GVdd	DRV_MEM_ADDR	(6)
$\overline{RAS}/CS[0 - 7]$	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GVdd	DRV_MEM_ADDR	(6)
\overline{FOE}	H1	I/O	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{RCS0}$	N4	I/O	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{RCS1}$	N2	Output	GVdd	DRV_MEM_ADDR	–
SDMA[11 – 0]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3 W1 W2	Output	GVdd	DRV_MEM_ADDR	(6)(14)
SDMA12/SDBA1	P1	Output	GVdd	DRV_MEM_ADDR	(14)

Table 1-1. PC8240 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
SDBA0	P2	Output	GVdd	DRV_MEM_ADDR	–
PAR[0 – 7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GVdd	DRV_MEM_ADDR	(6)(13)(14)
$\overline{\text{SDRAS}}$	AD1	Output	GVdd	DRV_MEM_ADDR	(3)
$\overline{\text{SDCAS}}$	AD2	Output	GVdd	DRV_MEM_ADDR	(3)
CKE	H2	Output	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{\text{WE}}$	AA1	Output	GVdd	DRV_MEM_ADDR	–
$\overline{\text{AS}}$	Y1	Output	GVdd	DRV_MEM_ADDR	(3)(4)
EPIC Control Signals					
IRQ_0/S_INT	C19	Input	OVdd	–	–
IRQ_1/S_CLK	B21	I/O	OVdd	DRV_PCI	–
IRQ_2/S_RST	AC22	I/O	OVdd	DRV_PCI	–
IRQ_3/ $\overline{\text{S_FRAME}}$	AE24	I/O	OVdd	DRV_PCI	–
IRQ_4/ $\overline{\text{L_INT}}$	A23	I/O	OVdd	DRV_PCI	–
Two-wire Interface Control Signals					
SDA	AE20	I/O	OVdd	DRV_STD	(10)(16)
SCL	AF21	I/O	OVdd	DRV_STD	(10)(16)
Clock Out Signals					
PCI_CLK[0 – 3]	AC25 AB25 AE26 AF25	Output	GVdd	DRV_PCI_CLK	(6)
PCI_CLK4/DA3	AF26	Output	GVdd	DRV_PCI_CLK	–
PCI_SYNC_OUT	AD25	Output	GVdd	DRV_PCI_CLK	–
PCI_SYNC_IN	AB23	Input	GVdd	–	–
SDRAM_CLK[0 – 3]	D1 G1 G2 E1	Output	GVdd	DRV_MEM_ADDR	(6)
SDRAM_SYNC_OUT	C1	Output	GVdd	DRV_MEM_ADDR	–
SDRAM_SYNC_IN	H3	Input	GVdd	–	–
CKO/DA1	B15	Output	OVdd	DRV_STD	–
OSC_IN	AD21	Input	OVdd	–	–
Miscellaneous Signals					
$\overline{\text{HRST_CTRL}}$	A20	Input	OVdd	–	–
$\overline{\text{HRST_CPU}}$	A19	Input	OVdd	–	–
$\overline{\text{MCP}}$	A17	Output	OVdd	DRV_STD	(3)(4)(17)
NMI	D16	Input	OVdd	–	–
$\overline{\text{SMI}}$	A18	Input	OVdd	–	(10)
$\overline{\text{SRESET}}$	B16	Input	OVdd	–	(10)
TBEN	B14	Input	OVdd	–	(10)
$\overline{\text{QACK/DA0}}$	F2	Output	OVdd	DRV_STD	(3)(4)
$\overline{\text{CHKSTOP_IN}}$	D14	Input	OVdd	–	(10)
MAA[0 – 2]	AF2 AF1 AE1	Output	–	DRV_MEM_DATA	(3)(4)(6)

Table 1-1. PC8240 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
\overline{MIV}	A16	Output	OVdd	DRV_STD	–
PMAA[0 – 2]	AD18 AF18 AE19	Output	OVdd	DRV_STD	(3)(4)(6)(15)
Test/Configuration Signals					
PLL_CFG[0 – 4]/ DA[10 – 6]	A22 B19 A21 B18 B17	Input	OVdd	–	(4)(6)
$\overline{TEST}[0 – 1]$	AD22 B20	Input	OVdd	–	(1)(6)(9)
$\overline{TEST2}$	Y2	Input	–	–	(11)
TEST3	AF20	Input	OVdd	–	(10)
TEST4	AC18	I/O	OVdd	DRV_STD	(10)
TCK	AF22	Input	OVdd	–	(9)(12)
TDI	AF23	Input	OVdd	–	(9)(12)
TDO	AC21	Output	OVdd	DRV_PCI	–
TMS	AE22	Input	OVdd	–	(9)(12)
TRST	AE23	Input	OVdd	–	(9)(12)
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground 52 terminals	–	–	–
LVdd	AC20 AC23 D20 D23 G23 P23 Y23	Reference voltage 3.3V, 5.0V	LVdd	–	–
GVdd	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for Memory Drivers 2.5V, 3.3V	GVdd	–	–
OVdd	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3V	OVdd	–	–
Vdd	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for Core 2.5V	Vdd	–	–
LAVdd	D17	Power for DLL 2.5V	LAVdd	–	–
AVdd	C17	Power for PLL (CPU Core Logic) 2.5V	AVdd	–	–
AVdd2	AF24	Power for PLL (Peripheral Logic) 2.5V	AVdd2	–	–

Table 1-1. PC8240 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
Manufacturing Pins					
DA2	C25	I/O	OVdd	DRV_PCI	(2)
DA[11 – 13]	AD26 AF17 AF19	I/O	OVdd	DRV_PCI	(2)(6)
DA[14 – 15]	F1 J2	I/O	GVdd	DRV_MEM_ADDR	(2)(6)

- Notes:
- Place pull-up resistors of 120Ω or less on the $\overline{\text{TEST}}[0 - 1]$ pins.
 - Treat these pins as No Connects unless using debug address functionality.
 - This pin has an internal pull-up resistor which is enabled only when the PC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a "1" is read into configuration bits during reset.
 - This pin is a reset configuration pin.
 - DL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the PC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to insure that a "1" is read into configuration bits during reset.
 - Multi-pin signals such as AD[0 – 31] or DL[0 – 31] have their physical package pin numbers listed in order corresponding to the signal names. Ex: AD0 is on pin C22, AD1 is on pin D22,... AD31 is on pin V25.
 - $\overline{\text{GNT4}}$ is a reset configuration pin and has an internal pull-up resistor which is enabled only when the PC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to insure that a "1" is read into configuration bits during reset.
 - Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this PCI control pin to LVdd.
 - V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in [Table 4-1, "DC Electrical Specifications," on page 17](#).
 - Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this pin to OVdd.
 - Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this pin to GVdd.
 - This pin has an internal pull-up resistor; the value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
 - Output Valid specifications for this pin are memory interface mode dependent (Registered or Flow-through), see [Table 4-6, "Output AC Timing Specifications," on page 24](#).
 - Non-DRAM Access Output Valid specification applies to this pin during non-DRAM accesses, see specification 12b3 in [Table 4-6, "Output AC Timing Specifications," on page 24](#).
 - This pin is affected by programmable PCI_HOLD_DEL parameter, see ["PCI Signal Output Hold Timing" on page 25](#).
 - This pin is an open drain signal.
 - This pin can be programmed to be driven (default) or can be programmed to be open drain; see PMCR2 register description in the Freescale PC8240 User's Manual for details.
 - This pin is a Sustained Tri-State pin as defined by the PCI Local Bus Specification.

2. Detailed Specification

This drawing describes the specific requirements for the PC8240 processor, in compliance with e2v standard screening.

3. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.
2. MIL-PRF-38535: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

3.1 Design and Construction

3.1.1 Terminal Connections

The terminal connections are shown in [Table 1-1, "PC8240 Pinout Listing,"](#) on page 4.

3.2 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Symbol	Characteristic ⁽¹⁾	Value	Unit
Vdd	Supply Voltage – CPU Core and Peripheral Logic	–0.3 to 2.75	V
GVdd	Supply Voltage – Memory Bus Drivers	–0.3 to 3.6	V
OVdd	Supply Voltage – PCI and Standard I/O Buffers	–0.3 to 3.6	V
AVdd/AVdd2/LAVdd	Supply Voltage – PLLs and DLL	–0.3 to 2.75	V
V _{IN}	Supply Voltage – PCI Reference	–0.3 to 3.6	V
LVdd	Input Voltage ⁽²⁾	–0.3 to 5.4	V
T _{STG}	Storage Temperature Range	–55 to 150	°C

- Notes:
1. Functional and tested operating conditions are given in [Table 3-2](#). Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
 2. PCI inputs with LVdd = 5V 5% V DC may be correspondingly stressed at voltages exceeding LVdd + 0.5V DC.

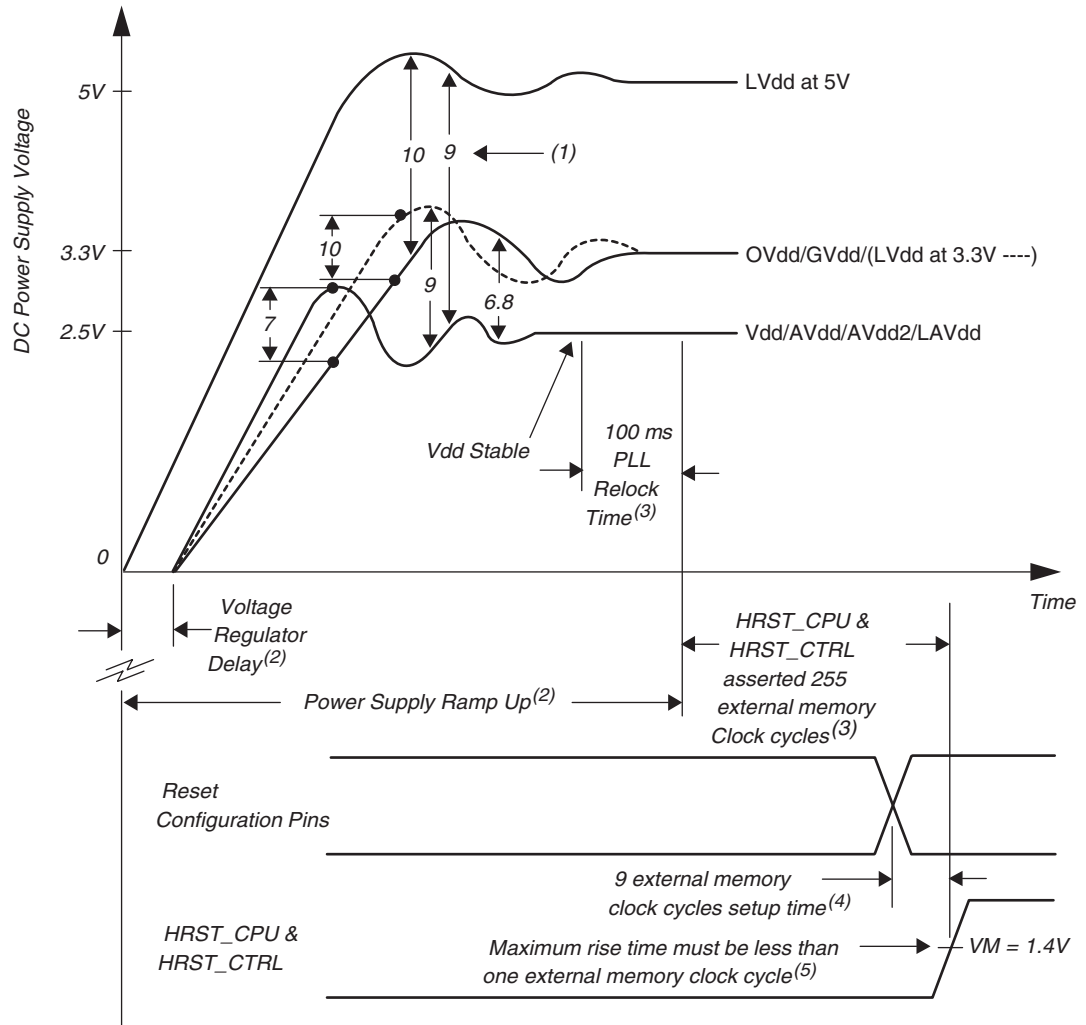
3.3 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions

Symbol	Characteristic ⁽¹⁾	Recommended Value	Unit	Notes	
Vdd	Supply Voltage	2.5 ± 5 %	V	(5)	
OVdd	I/O Buffer supply for PCI and Standard	3.3 ± 0.3	V	(5)	
GVdd	Supply Voltages for Memory Bus Drivers	3.3 ± 5 %	V	(7)	
		2.5 ± 5 %	V	(7)	
AVdd	PLL Supply Voltage – CPU Core Logic	2.5 ± 5 %	V	(5)	
AVdd2	PLL Supply Voltage – Peripheral Logic	2.5 ± 5 %	V	(6)	
LAVdd	DLL Supply Voltage	2.5 ± 5 %	V	(6)	
LVdd	PCI Reference	5 ± 5 %	V	(8)(9)	
		3.3 ± 0.3	V	(8)(9)	
V _{IN}	Input Voltage	PCI Inputs	0 to 3.6 or 5.75	V	(2)(3)
		All Other Inputs	0 to 3.6	V	(4)
T _C	Operating Temperature	–40 to 125	°C		

- Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
 2. PCI pins are designed to withstand LVdd + 0.5V DC when LVdd is connected to a 5.0V DC power supply.
 3. PCI pins are designed to withstand LVdd + 0.5V DC when LVdd is connected to a 3.3V DC power supply.
 4. Caution: Input voltage (V_{IN}) must not be greater than the supply voltage (Vdd/AVdd/AVdd2/LAVdd) by more than 2.5V at all times including during power-on reset.
 5. Caution: OVdd must not exceed Vdd/AVdd/AVdd2/LAVdd by more than 1.8V at any time including during power-on reset.
 6. Caution: Vdd/AVdd/AVdd2/LAVdd must not exceed OVdd by more than 0.6V at any time including during power-on reset.
 7. Caution: GVdd must not exceed Vdd/AVdd/AVdd2/LAVdd by more than 1.8V at any time including during power-on reset.
 8. Caution: LVdd must not exceed Vdd/AVdd/AVdd2/LAVdd by more than 5.4V at any time including during power-on reset.
 9. Caution: LVdd must not exceed OVdd by more than 3.6V at any time including during power-on reset.

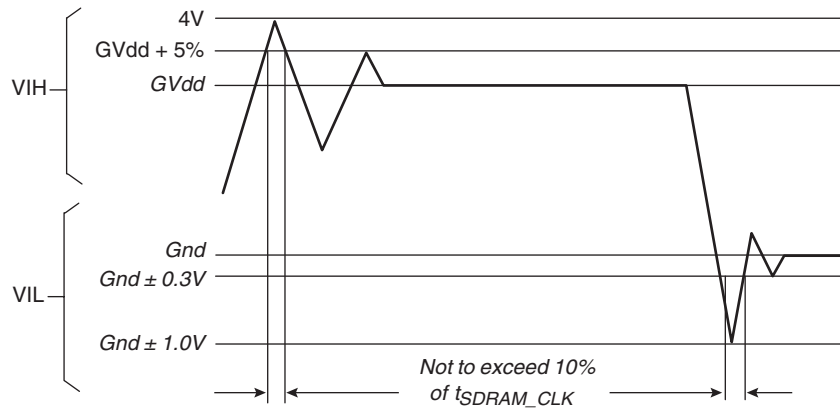
Figure 3-1. Supply Voltage Sequencing and Separation Cautions



- Notes:
1. Numbers associated with waveform separations correspond to caution numbers listed in [Table 3-2, "Recommended Operating Conditions,"](#) on page 9.
 2. Refer to ["Power Supply Voltage Sequencing"](#) on page 37 for additional information.
 3. Refer to [Table 4-4 on page 20](#) for additional information on PLL Relock and reset signal assertion timing requirements.
 4. Refer to [Table 4-5 on page 22](#) for additional information on reset configuration pin setup timing requirements.
 5. HRST_CPU/HRST_CTRL must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the non-reset state.

Figure 3-2 shows the undershoot and overshoot voltage of the memory interface of the PC8240.

Figure 3-2. Overshoot/Undershoot Voltage



3.4 Thermal Information

3.4.1 Thermal Characteristics

Table 3-3. Package Thermal Characteristics

Symbol	Characteristic	Min	Unit
θ_{JC}	Die Junction-to-Case Thermal Resistance	1.8	$^{\circ}C/W$
θ_{JB}	Die Junction-to-Board Thermal Resistance	4.8	$^{\circ}C/W$

3.4.2 Thermal Management Information

This section provides thermal management information for the tape ball grid array (TBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design, the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 3-3.

Figure 3-3. Package Exploded Cross-Sectional View with Several Heat Sink Options

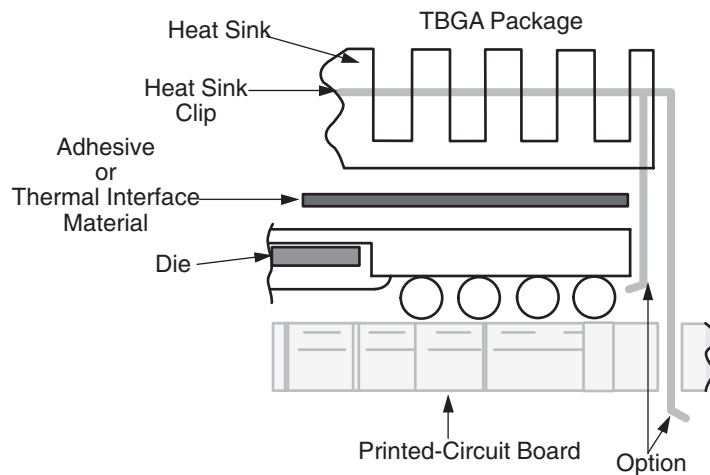
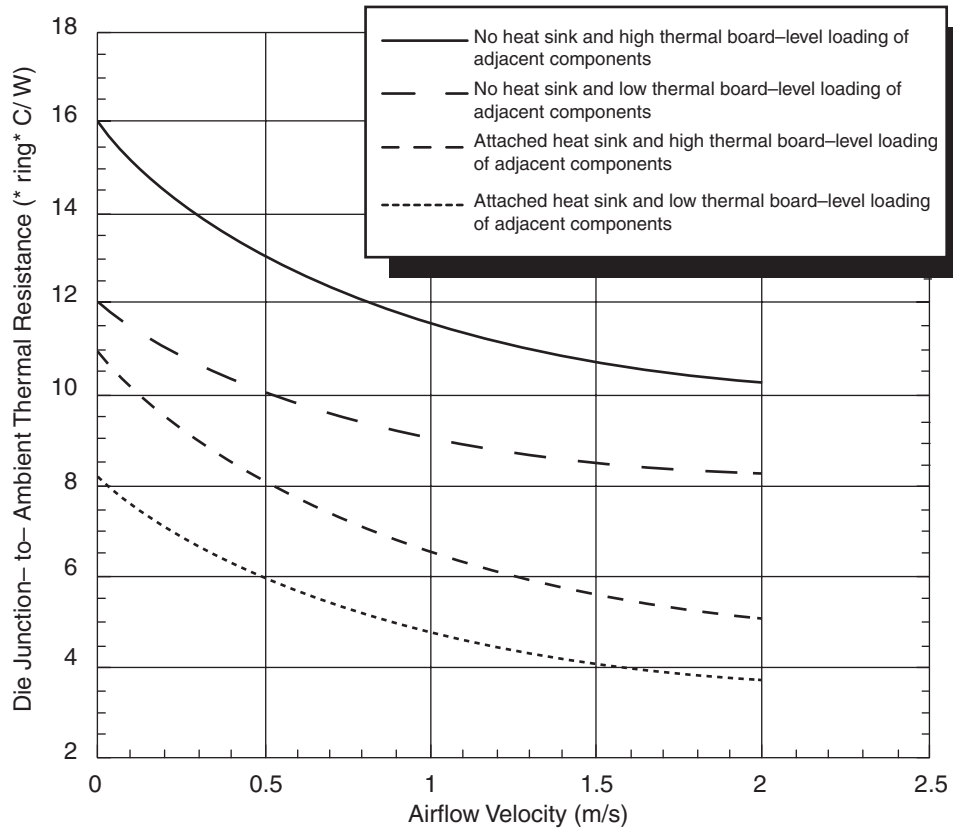


Figure 3-4 depicts the die junction-to-ambient thermal resistance for four typical cases:

1. A heat sink is not attached to the TBGA package and there exists high board-level thermal loading of adjacent components.
2. A heat sink is not attached to the TBGA package and there exists low board-level thermal loading of adjacent components.
3. A heat sink (e.g. ChipCoolers #HTS255-P) is attached to the TBGA package and there exists high board-level thermal loading of adjacent components.
4. A heat sink (e.g. ChipCoolers #HTS255-P) is attached to the TBGA package and there exists low board-level thermal loading of adjacent components.

Figure 3-4. Die Junction-to-Ambient Resistance



The board designer can choose between several types of heat sinks to place on the PC8240. There are several commercially-available heat sinks for the PC8240 provided by the following vendors:

Chip Coolers Inc. 333 Strawberry Field Rd. Warwick, RI 02887-6979	800-227-0254 (USA/Canada) 401-739-7600 Internet: www.chipcoolers.com
International Electronic Research Corporation (IERC) 135 W. Magnolia Blvd. Burbank, CA 91502	818-842-7277 Internet: www.ctscorp.com
Thermalloy 2021 W. Valley View Lane Dallas, TX 75234-8993	972-243-4321 Internet: www.thermalloy.com
Wakefield Engineering 100 Cummings Center, Suite 157H Beverly, MA 01915	781-406-3000 Internet: www.wakefield.com
Aavid Engineering 250 Apache Trail Terrell, TX 75160	972-551-7330 Internet: www.aavid.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

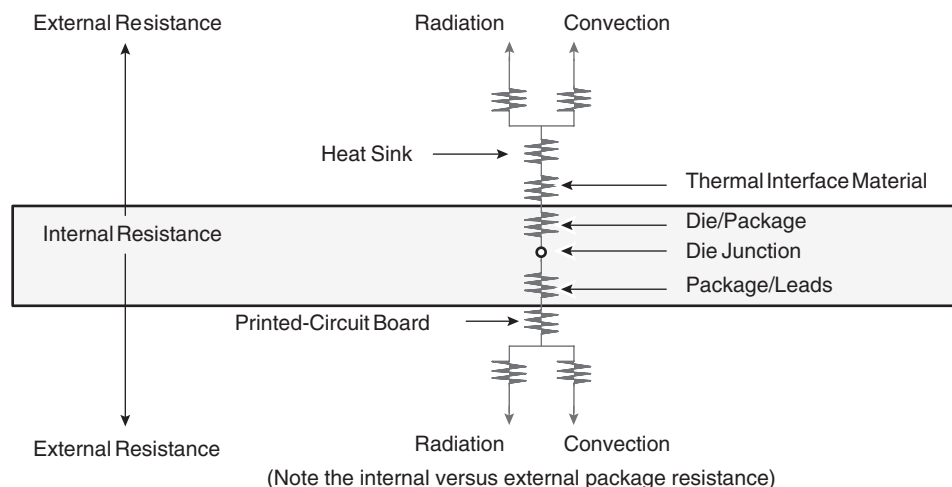
3.4.3 Internal Package Conduction Resistance

For the TBGA, cavity down, packaging technology, shown in [Figure 3-3 on page 11](#), the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance,
- The die junction-to-ball thermal resistance.

[Figure 3-5](#) depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 3-5. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



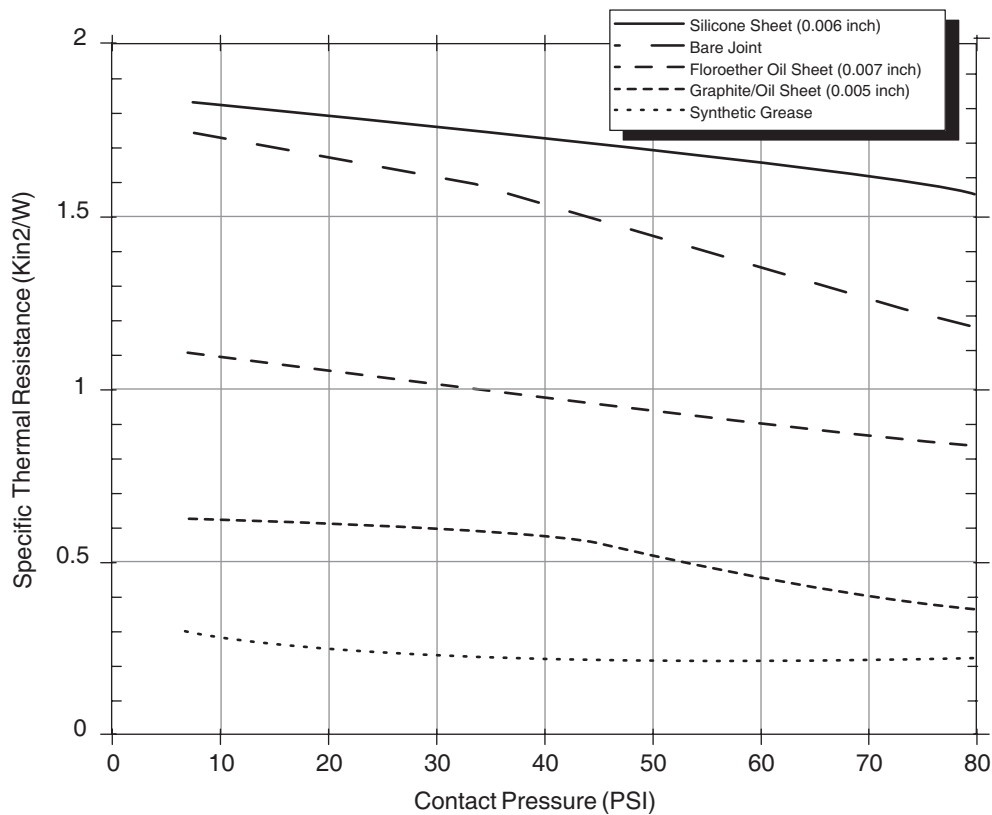
For this cavity-down, wire-bond TBGA package, heat generated on the active side of the chip is conducted through the silicon, the die attach and package spreader, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

3.4.4 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 3-6 shows the thermal performance of three thinsheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 3-5). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors, thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 3-6. Thermal Performance of Select Thermal Interface Material



The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation Dow-Corning Electronic Materials PO Box 0997 Midland, MI 48686-0997	800-248-2481 Internet: www.dow.com
Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4014	781-935-4850 Internet: www.chomerics.com
Thermagon Inc. 3256 West 25th Street Cleveland, OH 44109-1668	888-246-9050 Internet: www.thermagon.com
Loctite Corporation 1001 Trout Brook Crossing Rocky Hill, CT 06067-3910	860-571-5100 Internet: www.loctite.com

3.4.4.1 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

Where:

T_J is the die-junction temperature.

T_A is the inlet cabinet ambient temperature.

T_R is the air temperature rise within the computer cabinet.

θ_{JC} is the junction-to-case thermal resistance.

θ_{INT} is the adhesive or interface material thermal resistance.

θ_{SA} is the heat sink base-to-ambient thermal resistance.

P_D is the power dissipated by the device.

During operation the die-junction temperatures (T_J) should be maintained less than the value specified in Table. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40° C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10° C. The thermal resistance of the thermal interface material (θ_{INT}) is typically about 1° C/W. Assuming a T_A of 30° C, a T_R of 5° C, a TBGA package $\theta_{JC} = 1.8$, and a power consumption (P_D) of 5.0 watts, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30^\circ \text{ C} + 5^\circ \text{ C} + (1.8^\circ \text{ C/W} + 1.0^\circ \text{ C/W} + \theta_{SA}) \times 5.0\text{W}$$

For preliminary heat sink sizing, the heat sink base-to-ambient thermal resistance is needed from the heat sink manufacturer.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow.

The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature-airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's micro-electronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

3.5 Power Consideration

Table 3-4 provides preliminary power consumption data for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 3-4. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)				Unit	Notes
	33/66/166	33/66/200	33/100/200	66/100/200		
Typical	2.5	2.8	3.0	3.0	W	(1)(5)
Max – FP	3.0	3.4	3.6	3.6	W	(1)(2)
Max – INT	2.7	3.0	3.3	3.4	W	(1)(3)
Doze	1.8	2.0	2.2	2.2	W	(1)(4)(6)
Nap	700	700	900	900	mW	(1)(4)(6)
Sleep	500	500	500	800	mW	(1)(4)(6)

I/O Power Supplies				
Mode	Minimum	Maximum	Unit	Notes
Typ – OVdd	200	600	mW	(7)(8)
Typ – GVdd	300	900	mW	(7)(9)

- Notes:
1. The values include Vdd, AVdd, AVdd2, and LVdd but do not include I/O Supply Power, see "Power Supply Sizing" on page 38 for information on OVdd and GVdd supply power.
 2. Maximum – FP power is measured at Vdd = 2.625V with dynamic power management enabled while running an entirely cacheresident, looping, floating point multiplication instruction.
 3. Maximum – INT power is measured at Vdd = 2.625V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
 4. Power saving mode maximums are measured at Vdd = 2.625V while the device is in doze, nap, or sleep mode.
 5. Typical power is measured at Vdd = AVdd = 2.5V, OVdd = 3.3V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeroes on 64-bit boundaries to local memory are averaged.
 6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.

7. The typical minimum I/O power values were results of the PC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz.
8. The typical maximum OVdd value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes to PCI memory.
9. The typical maximum GVdd value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes on 64-bit boundaries to local memory.

Note: To calculate the power consumption at low temperature (–55°C), use a 1.25 factor.

3.6 Marking

The document where markings are defined is identified in the related reference documents. Each micro-circuit is legible and permanently marked with the following information as minimum:

- e2v Logo,
- Manufacturer’s part number, Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4. Electrical Characteristics

4.1 Static Characteristics

Table 4-1 provides the DC electrical characteristics for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9)

Table 4-1. DC Electrical Specifications

Characteristics ⁽¹⁾	Conditions ⁽⁴⁾	Symbol	Value		Unit
			Min	Max	
Input High Voltage	PCI only	V_{IH}	0.5*OVdd	LVdd	V
Input Low Voltage	PCI only	V_{IL}	–	0.3*OVdd	V
Input High Voltage	All other pins (GVdd = 3.3V)	V_{IH}	2.0	3.3	V
Input High Voltage	All other pins (GVdd = 2.5V)	V_{IH}	1.8	2.5	V
Input Low Voltage	All inputs except OSC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN Input High Voltage		CV_{IH}	0.5*OVdd	–	V
PCI_SYNC_IN Input Low Voltage		CV_{IL}	GND	0.3*OVdd	V
Input Leakage Current ⁽⁵⁾ for pins using DRV_PCI driver	0.5V V_{IN} 2.7V at LVdd = 4.75	I_L	–	70	A
Input Leakage Current ⁽⁵⁾ for pins using DRV_PCI driver	0.5V V_{IN} 5.5V at LVdd = 5.5	I_L	–	TBD	A
Input Leakage Current ⁽⁵⁾ all others	LVdd = 3.6V GVdd = 3.465	I_L	–	10	A
Output High Voltage	I_{OH} = N/A (GVdd = 3.3V) ⁽³⁾	V_{OH}	2.4	–	V
Output Low Voltage	I_{OL} = N/A (GVdd = 3.3V) ⁽³⁾	V_{OL}	–	0.4	V

Table 4-1. DC Electrical Specifications (Continued)

Characteristics ⁽¹⁾	Conditions ⁽⁴⁾	Symbol	Value		Unit
			Min	Max	
Output High Voltage	$I_{OH} = N/A$ (GVdd = 2.5V) ⁽³⁾	V_{OH}	1.85	–	V
Output Low Voltage	$I_{OL} = N/A$ (GVdd = 2.5V) ⁽³⁾	V_{OL}	–	0.6	V
Capacitance ⁽²⁾	$V_{IN} = 0V$, $f = 1$ MHz	C_{IN}	–	7.0	pF

- Notes:
1. See Table 1-1 on page 4 for pins with internal pull-up resistors.
 2. Capacitance is periodically sampled rather than 100% tested.
 3. See Table 4-2 on page 18 for the typical drive capability of a specific signal pin based upon the type of output driver associated with that pin as listed in.
 4. These specifications are for the default driver strengths indicated in Table.
 5. Leakage current is measured on input pins and on output pins in the high impedance state. The leakage current is measured for nominal OVdd/LVdd and Vdd or both OVdd/LVdd and Vdd must vary in the same direction.

Table 4-2 provides information on the characteristics of the output drivers referenced in. The values are from the PC8240 IBIS model (v1.0) and are not tested, for additional detailed information see the complete IBIS model listing at http://www.mot.com/SPS/PowerPC/teksupport/tools/IBIS/kahlua_1.ibs.txt

Table 4-2. Drive Capability of PC8240 Output Pins

Driver Type	Programmable Output Impedance (Ohms)	Supply Voltage (V)	I_{OH}	I_{OL}	Unit	Notes
DRV_STD	20	OVdd = 3.3	TBD	TBD	mA	(2)(5)
	40 (default)	OVdd = 3.3	TBD	TBD	mA	(2)(5)
DRV_PCI	25	LVdd = 3.3	11.0	20.6	mA	(1)(4)
		LVdd = 5.0	5.6	10.3	mA	(1)(4)
	50 (default)	LVdd = 3.3	5.6	10.3	mA	(1)(4)
		LVdd = 5.0	5.6	10.3	mA	(1)(4)
DRV_MEM_ADDR DRV_PCI_CLK	8 (default)	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	89.0	73.3	mA	(2)(5)
	13.3	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	55.9	46.4	mA	(2)(5)
	20	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	36.7	30.0	mA	(2)(5)
	40	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	TBD	TBD	mA	(2)(5)
DRV_MEM_DATA	20 (default)	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	36.7	30.0	mA	(2)(5)
	40	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	18.7	15.0	mA	(2)(5)

- Notes:
1. For DRV_PCI, I_{OH} read from the listing in the pull-up mode, I(Min) column, at the 0.33V label by interpolating between the 0.3V and 0.4V table entries' current values which correspond to the PCI $V_{OH} = 2.97 = 0.9 \cdot LVdd$ (LVdd = 3.3V) where Table Entry Voltage = LVdd - PCI V_{OH} .

2. For all others with OVdd or GVdd = 3.3V, I_{OH} read from the listing in the pull-up mode, I(Min) column, at the 0.9V table entry which corresponds to the V_{OH} = 2.4V where Table Entry Voltage = O/GVdd - PCI V_{OH}.
3. For GVdd = 2.5V, I_{OH} read from the listing in the pull-up mode, I(Min) column, at the TBDV table entry which corresponds to the V_{OH} = TBD V where Table Entry Voltage = GVdd - V_{OH}.
4. For DRV_PCI, I_{OL} read from the listing in the pull-down mode, I(Max) column, at 0.33V = PCI V_{OL} = 0.1*LVdd (LVdd = 3.3V) by interpolating between the 0.3V and 0.4V table entries.
5. For all others with OVdd or GVdd = 3.3V, I_{OL} read from the listing in the pull-down mode, I(Max) column, at the 0.4V table entry.
6. For GVdd = 2.5V, I_{OL} read from the listing in the pull-down mode, I(Max) column, at the TBDV table entry.

4.2 Dynamic Electrical Characteristics

This section provides the AC electrical characteristics for the PC8240. After fabrication, functional parts are sorted by maximum processor core frequency as shown in [Table 4-4, “Clock AC Timing Specifications,” on page 20](#) and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0-4] signals. Parts are sold by maximum processor core frequency; see [“Ordering Information” on page 42](#).

[Table 4-3](#) provides the operating frequency information for the PC8240.

At recommended operating conditions (see [Table 3-2 on page 9](#)) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-3. Operating frequency

Characteristic ⁽¹⁾	200 MHz		Unit
	Min	Max	
Processor Frequency (CPU)	100	200	MHz
Memory Bus Frequency	25 - 100		MHz
PCI Input Frequency	25 - 66		MHz

Note: 1. Caution: The PCI_SYNC_IN frequency and PLL_CFG[0 – 4] settings must be chosen such that the resulting peripheral logic/memory bus frequency, CPU (core) frequency, and PLL (VCO) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0 – 4] signal description in [“PLL Configuration” on page 36](#) for valid PLL_CFG[0 – 4] settings and PCI_SYNC_IN frequencies.

4.2.1 Clock AC Specifications

Table 4-4 provides the clock AC timing specifications as defined in Section.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-4. Clock AC Timing Specifications

Num	Characteristics and Conditions ⁽¹⁾	Min	Max	Unit	Notes
1a	Frequency of Operation (PCI_SYNC_IN)	25	66	MHz	
1b	PCI_SYNC_IN Cycle Time	40	15	ns	
2, 3	PCI_SYNC_IN Rise and Fall Times	–	2.0	ns	(2)
4	PCI_SYNC_IN Duty Cycle Measured at 1.4V	40	60	%	
5a	PCI_SYNC_IN Pulse Width High Measured at 1.4V	6	9	ns	(3)
5b	PCI_SYNC_IN Pulse Width Low Measured at 1.4V	6	9	ns	(3)
7	PCI_SYNC_IN Short Term Jitter (Cycle to Cycle)	–	< 500	ps	
8a	PCI_CLK[0 – 4] Skew (Pin to Pin)	0	500	ps	
8b	SDRAM_CLK[0 – 3] Skew (Pin to Pin)	TBD	TBD	ps	(8)
10	Internal PLL Relock Time	–	100	µs	(3)(4)(6)
15	DLL Lock Range with DLL_EXTEND = 0 disabled (Default)	0 (NT _{clk} - t _{loop} - t _{fix0}) 7		ns	(7)
16	DLL Lock Range with DLL_EXTEND = 1 enabled	0 (NT _{clk} - T _{clk} /2 - t _{loop} - t _{fix0}) 7		ns	(7)
17	Frequency of Operation (OSC_IN)	25	66	MHz	
18	OSC_IN Cycle Time	40	15	ns	
19	OSC_IN Rise and Fall Times	–	5	ns	(5)
20	OSC_IN Duty Cycle Measured at 1.4V	40	60	%	
21	OSC_IN Frequency Stability	–	100	ppm	
22	OSC_IN V _{IH} (Loaded)	TBD		V	
23	OSC_IN V _{IL} (Loaded)	–	TBD	V	

- Notes:
1. These specifications are for the default driver strengths indicated in Table 4-2 on page 18.
 2. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4V.
 3. Specification value at maximum frequency of operation.
 4. Relock time is guaranteed by design and characterization. Relock time is not tested.
 5. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.
 6. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
 7. DLL_EXTEND is bit 7 of the PMC2 register <72>. N is a non-zero integer (1, 2, 3, ...). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. t_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. t_{fix0} is a fixed delay inherent in the design when the DLL is at tap point 0 and the DLL is contributing no delay; t_{fix0} equals approximately 3 ns. See Figure 4-2 on page 21 for DLL locking ranges.

8. Pin to pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, i.e. the amount of variance between the internal sys-logic_clk and the SDRAM_SYNC_IN signal after the DLL is locked. While pin to pin skew between SDRAM_CLKs can be measured, the relationship between the internal sys-logic_clk and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.

Figure 4-1. PCI_SYNC-IN Input Clock Timing Diagram

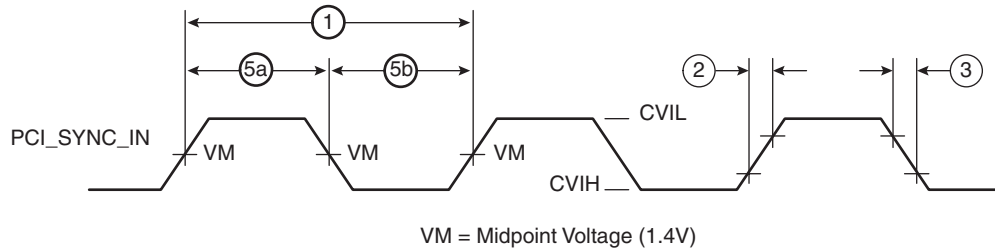
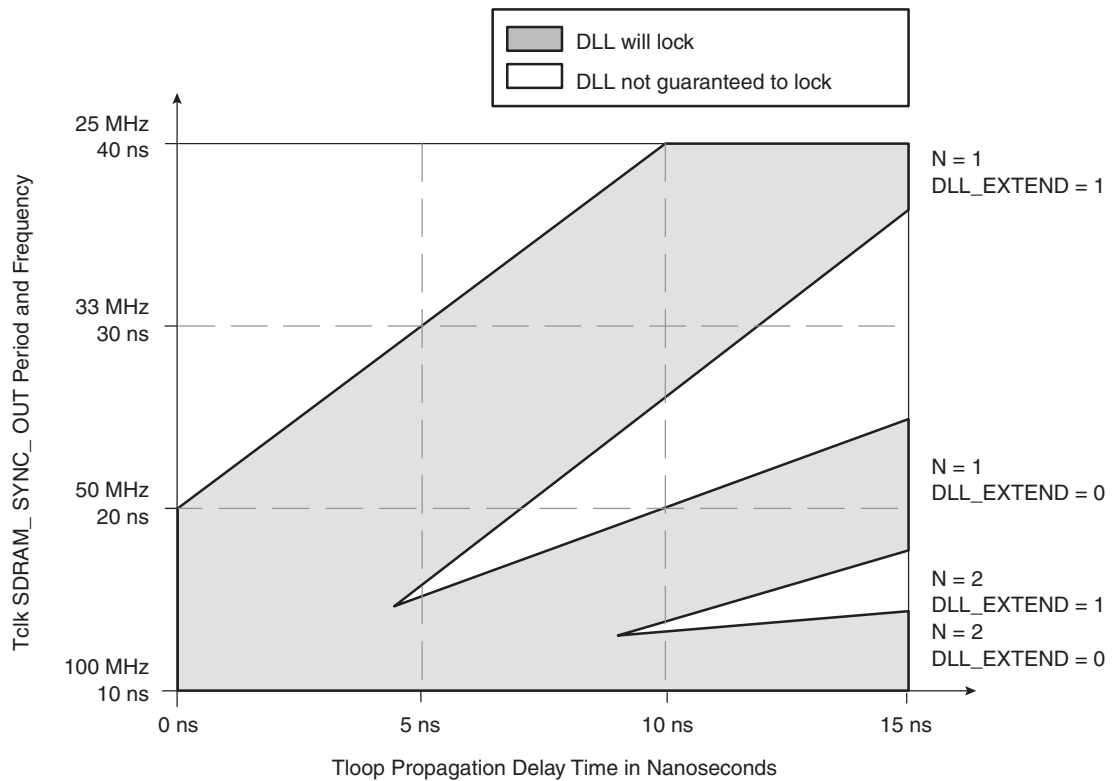


Figure 4-2. DLL Locking Range Loop Delay vs. Frequency of Operation



4.2.2 Input AC Timing Specifications

Table 4-5 provides the input AC timing specifications. See Figure 4-3 on page 22 and Figure 4-4 on page 23.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-5. Input AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
10a	PCI Input Signals Valid to PCI_SYNC_IN (Input Setup)	2.0	–	ns	(2)(3)
10b1	Memory Control and Data Input Signals in Flow Through Mode Valid to SDRAM_SYNC_IN (Input Setup)	4.0	–	ns	(1)(3)
10b2	Memory Control and Data Input Signals in Registered Mode Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10c	Epic, Misc. Debug Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10d	Two-wire Interface Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10e	Mode select Inputs Valid to HRST_CPU/HRST_CTRL (Input Setup)	9*t _{CLK}	–	ns	(1)(3)(5)
11a	PCI_SYNC_IN (SDRAM_SYNC_IN) to Inputs Invalid (Input Hold)	1.0	–	ns	(1)(2)(3)
11b	HRST_CPU/HRST_CTRL to Mode select Inputs Invalid (Input Hold)	TBD	–	ns	(1)(3)(5)

- Notes:
1. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 4-3 on page 22.
 2. All PCI signals are measured from OVdd/2 of the rising edge of PCI_SYNC_IN to 0.4*OVdd of the signal in question for 3.3V PCI signaling levels. See Figure 4-4.
 3. Input timings are measured at the pin.
 4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
 5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the HRST_CPU/HRST_CTRL signal. See Figure 4-5.

Figure 4-3. Input – Output Timing Diagram Referenced to SDRAM_SYNC_IN

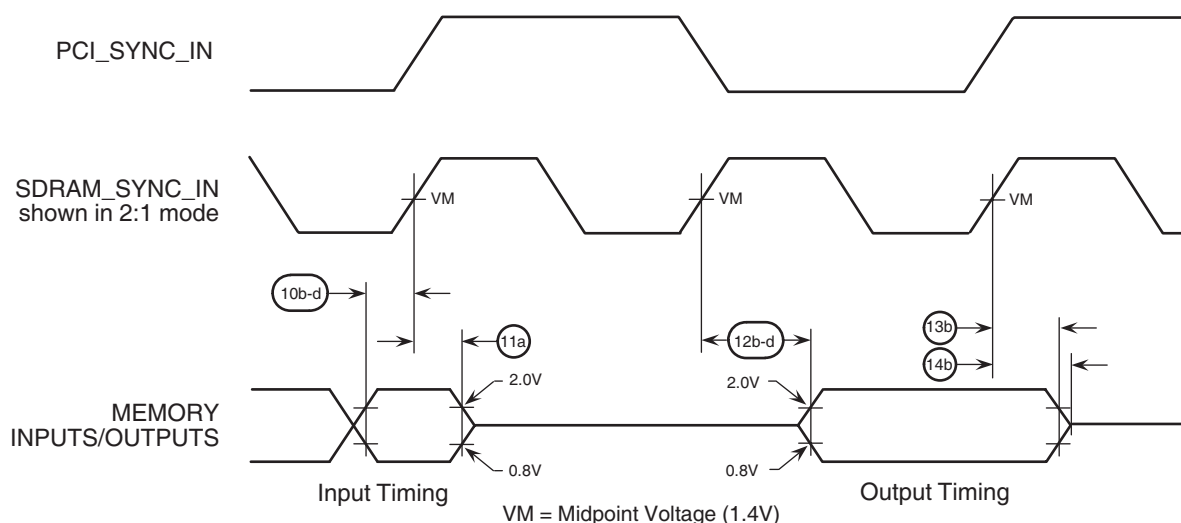


Figure 4-4. Input – Output Timing Diagram Referenced to PCI_SYNC_IN

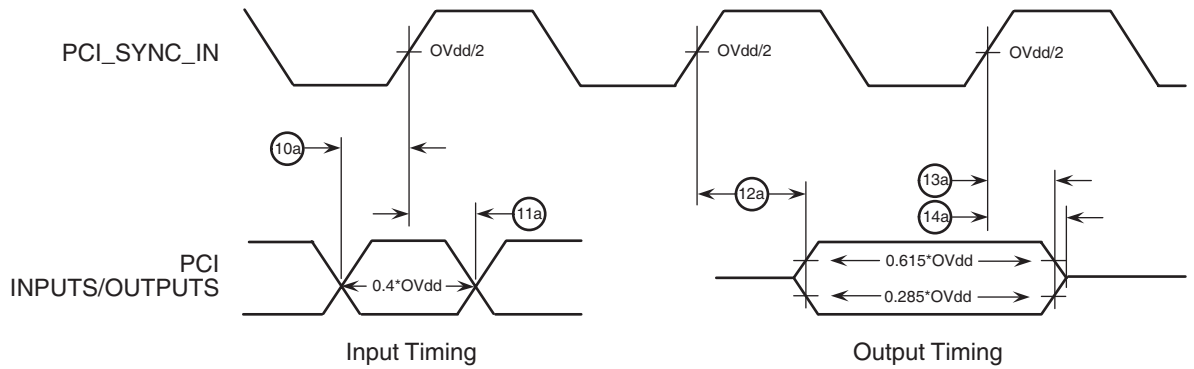
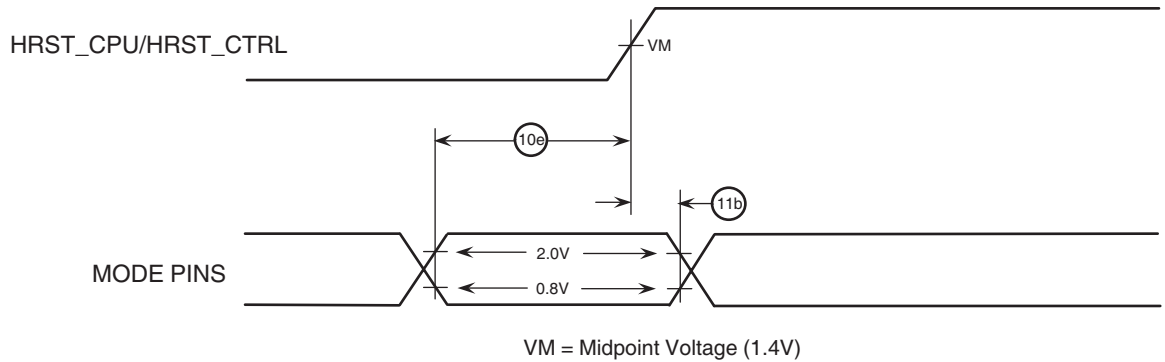


Figure 4-5. Input Timing Diagram for Mode Select Signals



4.2.3 Output AC Timing Specification

Table 4-6 provides the processor bus AC timing specifications for the PC8240. See Figure 4-3 on page 22 and Figure 4-4 on page 23.

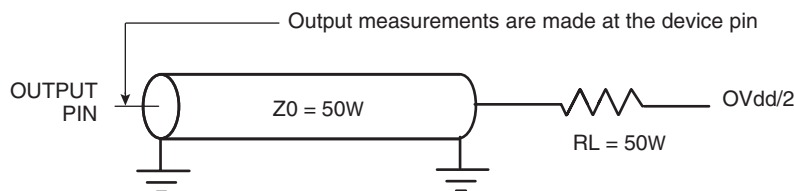
At recommended operating conditions (see Table 3-2 on page 9) with $GV_{dd} = 3.3V \pm 5\%$ and $LV_{dd} = 3.3V \pm 5\%$

Table 4-6. Output AC Timing Specifications

Num	Characteristics ⁽³⁾⁽⁶⁾	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to Output Valid, 66 MHz PCI, with \overline{MCP} pulled-down to logic 0 state. See Figure 4-7.	–	6.0	ns	(2)(4)
	PCI_SYNC_IN to Output Valid, 33 MHz PCI, with \overline{MCP} in the default logic 1 state. See Figure 4-7.	–	8.0	ns	(2)(4)
12b1	SDRAM_SYNC_IN to Output Valid (For Memory Control and Data Signals accessing DRAM in Flow Through Mode)	–	7.0	ns	(1)
12b2	SDRAM_SYNC_IN to Output Valid (For Memory Control and Data Signals accessing DRAM in Registered Mode)	–	TBD	ns	(1)
12b3	SDRAM_SYNC_IN to Output Valid (For Memory Control and Data Signals accessing non-DRAM)	–	TBD	ns	(1)
12c	SDRAM_SYNC_IN to Output Valid (For All Others)	–	7.0	ns	(1)
12d	SDRAM_SYNC_IN to Output Valid (For Two-wire Interface)	–	TBD	ns	(1)
13a	Output Hold, 66 MHz PCI, with \overline{MCP} and CKE pulled-down to logic 0 states. See Table 4-7.	0.5	–	ns	(2)(4)(5)
	Output Hold, 33 MHz PCI, with \overline{MCP} in the default logic 1 state and CKE pulled-down to logic 0 state. See Table 4-7.	2.0	–	ns	(2)(4)(5)
13b	Output Hold (For All Others)	0	–	ns	(1)
14a	PCI_SYNC_IN to Output High Impedance (For PCI)	–	TBD	ns	(2)(4)
14b	SDRAM_SYNC_IN to Output High Impedance (For All Others)	–	TBD	ns	(1)

- Notes:
1. All memory and related interface output signal specifications are specified from the $V_M = 1.4V$ of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 4-3 on page 22.
 2. All PCI signals are measured from $OV_{dd}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \cdot OV_{dd}$ or $0.615 \cdot OV_{dd}$ of the signal in question for 3.3V PCI signaling levels. See Figure 4-4 on page 23.
 3. All output timings assume a purely resistive 50Ω load (See Figure 4-6 on page 24). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
 4. PCI Bussed signals are composed of the following signals: \overline{LOCK} , \overline{IRDY} , $\overline{C/BE}[0 - 3]$, \overline{PAR} , \overline{TRDY} , \overline{FRAME} , \overline{STOP} , \overline{DEVSEL} , \overline{PERR} , \overline{SERR} , $AD[0 - 31]$, $\overline{REQ}[4 - 0]$, $\overline{GNT}[4 - 0]$, \overline{IDSEL} , \overline{INTA} .
 5. PCI hold times can be varied, see “PCI Signal Output Hold Timing” on page 25 for information on programmable PCI output hold times. The values shown for item 13a are for PCI compliance.
 6. These specifications are for the default driver strengths indicated in Table 4-2 on page 18.

Figure 4-6. AC Test Load for the PC8240



4.2.3.1 PCI Signal Output Hold Timing

In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33 MHz and 66 MHz PCI systems, the PC8240 has a programmable output hold delay for PCI signals. The initial value of the output hold delay is determined by the values on the \overline{MCP} and CKE reset configuration signals. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register.

Table 4-7 describes the bit values for the PCI_HOLD_DEL values in PMCR2.

Table 4-7. Power Management Configuration Register 2-0x72

Bit	Name	Reset value	Description
6–4	PCI_HOLD_DEL	xx0	<p>PCI output hold delay values relative to PCI_SYNC_IN. The initial values of bits 6 and 5 are determined by the reset configuration pins MCP and CKE, respectively. As these two pins have internal pull-up resistors, the default value after reset is 0b110.</p> <p>While the minimum hold times are guaranteed at shown values, changes in the actual hold time can be made by incrementing or decrementing the value in these bit fields of this register via software or hardware configuration. The increment is in approximately 400 picosecond steps. Lowering the value in the three bit field decreases the amount of output hold available.</p> <p>000 66 MHz PCI. Pull-down \overline{MCP} configuration pin with a 2K or less value resistor. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 4-4 are met for a 66 MHz PCI system. See Figure 4-7 on page 26.</p> <p>001 010 011 100 33 MHz PCI. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 4-4 are met for a 33 MHz PCI system. See Figure 4-7 on page 26.</p> <p>101 110 (Default if reset configuration pins left unconnected) 111</p>