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Introduction

DESCRIPTION

Microsemi's PD69101 is a single port, mixed-signal, high-voltage Power over Ethernet driver. The device is utilized in Ethernet switches and enables network devices to share power and data over the same cable. It enables detection of IEEE802.3af-2003 compliant PDs (Powered Devices) and IEEE802.3at High Power Devices, thus, ensuring safe power feeding and disconnection of ports with full digital control and a minimum of external components. Integrating power, analog and state of the art logic, the PD69101 device fits into a single 24-pin, plastic QFN package.

A "plug and play" device, the PD69101 executes all real time functions as specified in the IEEE802.3af-2003 ("AF") and IEEE802.3at High Power ("AT") standards, including load detection, "AF" and "AT" classification, and using Multiple Classification Attempts (MCA).

The PD69101 :

- Is designed to detect and disable disconnected ports, utilizing DC disconnection methods, as specified in the IEEE 802.3af-2003 and IEEE802.3ar-2009 standards.
- Can optionally detect legacy/pre-standard PD devices.
- Provides PD protection such as over-load, under-load, over-voltage, over-temperature and short-circuiting.
- Supports supply voltages ranging from 44 V to 57 VDC with no need for additional power supply sources.
- Is a low power device using an internal 0.34 Ω MOSFET and an external 0.5 Ω sense resistor.

The chip includes built-in internal thermal protection.

Two LEDs provide port state's indication and port type (AF/AT).

KEY FEATURES

- Fully IEEE802.3af-2003 and IEEE802.3at-2009 compliant
- Includes two-event classification
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 - 57 VDC)
- Supports 2 Pairs and 4 Pairs (Data and Spare Power Feeding)
- V_{MAIN} Out of Range Protection
- Wide temperature range: -40° to +85° C
- Over-temperature protection
- Low thermal dissipation (0.5 Ω sense resistor)
- Includes on/off command pin
- 2 x direct LEDs drive
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable AT/AF modes
- Configurable standard and legacy detection mode
- Power soft start mechanism
- On-chip thermal protection
- Voltage monitoring & protection
- Built in 3.3 VDC regulator
- Internal power on reset
- RoHS compliant
- Low Rdson FET: 0.3 Ω

IMPORTANT: For the most current data, consult MICROSEMI's website: http://www.microsemi.com

PACKAGE ORDER INFO		THERMAL DATA
T_A (°C)	Plastic 24 pin QFN 4x5	TYPICAL THERMAL RESISTANCE-JUNCTION TO AMBIENT 25° C/W
	RoHS Compliant / Pb-free / MSL1	TYPICAL THERMAL RESISTANCE-JUNCTION TO CASE 4° C/W
-40 to +85	**PD69101ILQ-TR**	Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

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POWER DISSIPATION INFORMATION

Rsense Power Dissipation: 0.5 Ω x $Iport^2$
Rds_ON Power Dissipation: 0.3 Ω x $Iport^2$

Pport_AF = 15.4W	==>	PRsense = 51 mW (320 mA) PRds_ON = 31 mW (320 mA)
Pport_AT = 30W	==>	PRsense= 180 mW (600 mA) PRds_ON = 108 mW (600 mA)

Typical PD69101 self power dissipation (including internal regulations) = 0.5 W (50 VDC)

Typical PD69101 @ 2 pairs AF application power dissipation = 0.5 W + 51 mW + 31 mW = 0.582 W

Typical PD69101 @ 2 pairs AT application power dissipation = 0.5 W + 180 mW + 108 mW = 0.788 W

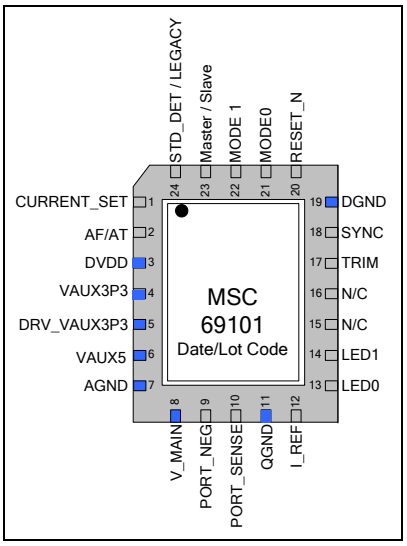
Typical 4 pairs application, with 2 x PD69101: double the power dissipation

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{MAIN})	-0.3 to 74 VDC
Port_Neg pin, LED0, LED1	-0.3 to 74 VDC
Port_Sense Pin	-0.3 to 3.6 VDC
QGND, AGND Pins	-0.3 to 0.3 VDC
VAUX5	-0.3V to 5.5V
All Other Pins	-0.3 to 3.6 VDC
Operating Ambient Temperature Range	-40 to +85°C
Maximum Operating Junction Temperature	150° C
ESD Protection at all I/O Pins	±2 KV HBM
Storage Temperature Range	-65° to +150° C

Notes:
Exceeding these ratings can cause damage to the device. Pin Port_Sense is ESD sensitive, pass 500V HBM. All voltages are with respect to ground. Currents are marked positive when flowing into a specified terminal and marked negative when flowing out of a specified terminal.

PACKAGE PIN OUT



(Top View)

RoHS / Pb-free 100% Matte Tin Finish

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ROHS AND SOLDER REFLOW INFORMATION

RoHS 6/6
Pb-free 100% Matte Tin Finish
Package Peak Temperature for Solder Reflow 260° C (+0° C, -5° C)
(40 seconds maximum exposure)

Notes: Exceeding these ratings can damage the device.

IPC/JEDEC J-STD-020C July 2004

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

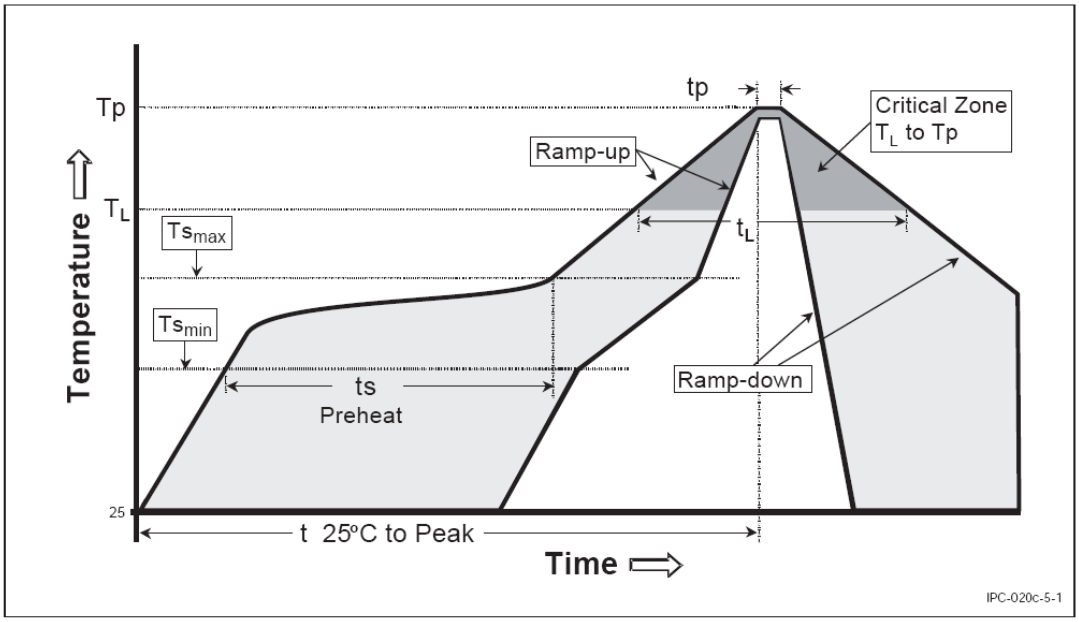

Figure 5-1 Classification Reflow Profile

Table 4-2 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.

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Electrical Characteristics

Unless otherwise specified, the following specifications apply to the operating ambient temperature, T_{AMB} -40° to +85° C.

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69101 CONTROLLER			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Input Voltage	V_{MAIN}	Supports Full IEEE802.3 functionality	44	55	57	VDC
Power Supply Current @ Operating Mode		V_{MAIN} = 55 V			10	mA
DIGITAL I/O						
Input Logic High Threshold	V_{IH}		2.2			VDC
Input Logic Low Threshold	V_{IL}				0.8	VDC
Input Hysteresis Voltage			0.4	0.6	0.8	VDC
Input High Current	I_{IH}		-10		10	uA
Input Low Current	I_{IL}		-10		10	uA
Output High Voltage	V_{OH}	For I_{OH} = -1 mA	2.4			VDC
Output Low Voltage	V_{OL}	I_{OH} = 1 mA			0.4	VDC
POE LOAD CURRENTS						
AT High Limit Mode	AT_LIM_HIGH (high current level for future use)	R_{SENSE} = 0.5 Ω 1% connected at Port_Sense pin	1.18	1.2	1.28	A
AT Medium Limit Mode	AT_LIM_MID (medium current level for future use)		847	874	919	mA
AT Low Limit Mode	AT_LIM_LOW		706	722	767	mA
AF Limit Mode	AF_LIM		410	425	448	mA
MAIN POWER SWITCHING FET						
On Resistance	R_{DSON}			0.3		Ω
Internal Thermal Protection Threshold				200		°C
LED0 AND LED1 DRIVERS						
Current Sink	I sink (from Vmain to AGND)			3	5	mA

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Dynamic Characteristics

The PD69101 utilizes three current level thresholds (I_{min}, I_{cut}, I_{lim}) and three timers (T_{min}, T_{cut}, T_{lim}).

- Loads that consume I_{lim} current for more than T_{lim} are labeled as 'short circuit state' and shutdown.
- Loads that dissipate more than I_{cut} for longer than T_{cut} are labeled as 'overloads' and are shutdown.
- If output power is below I_{min} for more than T_{min}, the PD is labeled as 'no-load' and is shutdown.

Automatic recovery from over-load and no-load conditions is attempted every T_{OVLREC} periods (typically 1 second). Output power is limited to $I_{lim,}$ which is a maximum peak current allowed at the port.

Table 1: IEEE802.3 AF Mode Parameters

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic Recovery from No-load Shutdown	T_{UDLREC} value, measured from port shutdown point (can be modified through control port)			1		Sec
Cutoff timers Accuracy	Typical accuracy of T_{cut}			2		ms
Inrush Current	I_{Inrsh}	For t=50 ms, C_{load}=180 uF max.	400		450	mA
Output Current Operating Range	I_{port}	Continuous operation after startup period.	10		375	mA
Output Power Available Operating Range	P_{port}	Continuous operation after startup period, at port output.	0.57		15.4	W
Off mode Current	I_{min1}	Must disconnect for T greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
PD Power Maintenance Request Drop-out Time Limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over-load Current Detection Range	I_{cut}	Time limited to T_{OVL}	350		400	mA
Over Load Time Limit	T_{OVL}		50		75	ms
Turn On Rise Time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn Off Time	T_{off}	From V_{port} to 2.8 Vdc			500	ms
Time Maintain Power Signature	T_{MPS}	DC modulation time for DC disconnect		49		ms

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Table 2: IEEE802.3 AT Mode Parameters

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic Recovery from No-load Shutdown	T_{UDLREC} value; measured from port shutdown point (can be modified through control port)			1		s
Cutoff Timers Accuracy	Typical accuracy of T_{cut}			2		ms
Inrush Current	I_{Inrsh}	For t = 50 ms, Cload = 180 uF max.	400		450	mA
Output Current Operating range	I_{port}	Continuous operation after startup period	10		725	mA
Output Power Available, Operating Range	P_{port}	Continuous operation after startup period at port output	0.57		36.25	W
Off Mode Current	I_{min1}	Must disconnect where T is greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
PD Power Maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over-load Current detection range	I_{cut}	Time limited to T_{OVL}			600	mA
Over-load Time Limit	T_{OVL}		50		75	ms
Turn on Rise Time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn Off Time	Toff	From V_{port} to 2.8 Vdc			500	ms
Time Maintain Power Signature	TMPS	DC modulation time for DC disconnect		49		ms

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Detailed Pinout Description

PIN	PIN NAME	PIN TYPE	DESCRIPTION
0	Exposed PAD	Analog Gnd	Exposed PAD; metal plate on the IC bottom side connected to analog ground. A high quality ground plane (about 500 mil inch over 500 mil inch) should be deployed around this pin whenever possible.
1	CURRENT_SET	Digital Input	User input to set AF / AT and maximum current limit. Use Pull-up resistors to DVDD or Pull-Down resistors to DGND to set mode of operation according to the detailed tables (page 4).
2	AF/AT	Digital Input	
3	DVDD	Power In	Regulated Input Voltage (3.3 V) for internal digital circuitry. Should be externally connected to pin 4.
4	VAUX3P3	Power In	Voltage regulation in 3.3 VDC. To be connected to pin 5. A 4.7 uF capacitor to AGND is recommended.
5	DRV_VAUX3P3	Power Out	Internal voltage regulator out 3.3 VDC. To be connected externally to pin 4.
6	VAUX5	Power	Regulated 5 VDC voltage filter. A 1 uF capacitor to AGND is recommended.
7	AGND	Power	Analog GND
8	V_MAIN	Power	Supply voltage for the internal analog circuit. Place a low ESR bypass capacitor, not less than 1 uF, as close as possible to AGND and this pin with low impedance traces.
9	PORT_NEG	Analog I/O	Negative output of the port.
10	PORT_SENSE	Analog Input	Sense resistor port input (connected to 0.5, 1% Ohm resistor to GND).
11	QGND	Power	Quiet analog ground: used for sensitive analog cells.
12	I_REF	Analog I/O	Resistor reference. Connect 30.1 K 1% resistor to QGND.
13	LED0	Open Drain I/O	Port Status Direct LED indications – see detailed table description. This is a High voltage, Open drain, Active low (SINK) output pin. Recommended to be connected to LED and Vmain through a ~18.2 Kohm (~3 mA) resistor
14	LED1	Open Drain I/O	
15	N/C	Analog I/O	Test pin; for production use only. Keep open; not connected.
16	N/C	Analog I/O	
17	TRIM	Analog Input	Zapping Input for IC production trimming. Should be connected to DVDD.
18	SYNC	Digital I/O	Synchronization open drain IO pin between master and slave, for 4-Pair applications In ALT A 2 Pair mode (Switch) this pin should be pulled down to DGND via a 4.7 Kohm resistor. In 4 Pair mode, connect the SYNC pin of Master and Slave and pull it up to the DVDD with 4.7 Kohm resistor
19	DGND	Digital I/O	Digital GND.
20	RESET_N	Digital Input	Reset input / On-Off command (Active Low).
21	MODE 0	Test I/O	Configuration Input Pins: Used to set Mode of operation and Test mode at production. Typically connected to DGND. See Table Below
22	MODE 1	Test I/O	
23	Master/Slave	Digital Input	If connected to DVDD (3.3 VDC): Master mode If connected to GND: Slave mode (4 Pair application)

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PIN	PIN NAME	PIN TYPE	DESCRIPTION
24	STD_DET / LEGACY	Digital Input	User input pin to set chip mode of operation. • "1": DVDD = IEEE802.3af compliant resistor detection only • "0": DGND = AF / AT Detection and Legacy (non-standard) line detection

Additional Pin Description and Notes

Note:

- "0" = Connect to DGND
- "1" = Connect to DVDD

CURRENT_SET and **AF/AT** pins determine the typical PD Load output current as detailed in the following coding:

AT/AF PIN	CURRENT_SET PIN	CONTINUE MAX CURRENT I CUT [MA]	TYPICAL I LIM [MA]	IEEE802.3
0	0	350	425	AF mode (standard)
1	0	600	722	AT mode (standard)
1	1	720	874	AT mode (high power)
0	1	1000	1200	AT mode (extra high power)

Configuration / Mode of Operation Coding:

MODE 0	MODE 1	MODE	DESCRIPTION
0	0	Normal operation Mode	Standard Operation POE Mode – LED0 and LED1 Outputs are used for Direct LED Drive as listed below
0	1	Serial Monitoring Mode	Standard Operation POE Mode – LED0 and LED1 are used to Continuously Streaming Out Internal Logic Signals for POE Monitoring
1	0	Test Logic Mode	Internal IC Logic Test Mode – Used in production only
1	1	JTAG Mode	Internal IC Logic Test Mode – Used in production only

LED I/Os Behavior

- LED pin is a high voltage Open Drain output pin.
- LED pin is an Active Low (SINK) pin ➔ LED is "ON" when I/O is pulled Low.

Table 3: 2 Pair Behaivor

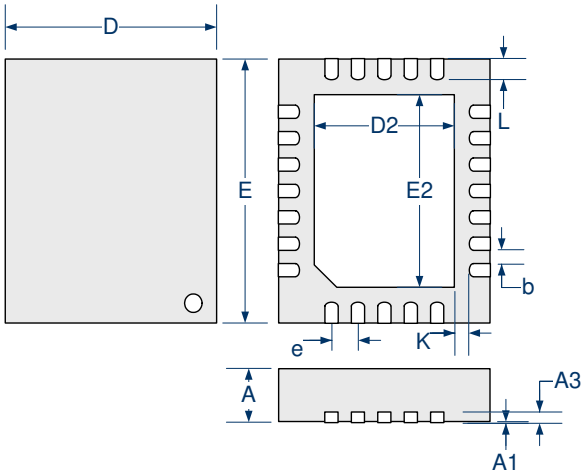
STATUS INDICATIONS	LED0	LED1	NOTES
AF Mode – Port "ON"	ON	OFF	Useful for Bicolor LED connected from LED0 to LED1
AT Mode (Class AT was detected) - Port "ON"	ON	ON	
AF Mode – Over-load or short	Blink 1 Hz	OFF	Blinking continues for ~ 2 sec
AT Mode – Over-load or short	Blink 1 Hz	Blink 1 Hz	Blinking continues for ~ 2 sec
Vmain Voltage out of range or IC over-temperature	Blink 4 Hz	OFF	Blinking continues as long as over-voltage or over-temperature state exists
AF Mode – Port "OFF"	OFF	ON	Useful for Bicolor LED connected from LED0 to LED1
AT Mode – Port "OFF"	OFF	OFF	

Table 4: 4 Pair Behavior (2 x PD69101 ICs)

STATUS INDICATIONS	LED0	LED1	NOTES
Master IC "ON and Slave IC "ON"	OFF	ON	
Only Master IC "ON (Slave IC "OFF")	ON	OFF	
Master and Slave ICs are both "OFF" due to Overload or Short	OFF	Blink 1 Hz	Blinking continues for ~ 2 sec after overload / short event
Vmain Voltage out of range or IC over-temperature	Blink 4 Hz / 1Hz	OFF	Master IC fail: blink 4 Hz Slave IC fail: blink 1 Hz Blinking continues for ~ 2 sec
Master IC "OFF" and Slave IC "OFF"	OFF	OFF	

PD69101 - Package Description

LQ **24-Pin QFN 4x5mm**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	2.50	2.75	0.098	0.108
E2	3.50	3.75	0.138	0.148
D	4.00 BSC		0.158 BSC	
E	5.00 BSC		0.197 BSC	

Note:
Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

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PD69101 - Internal Block Diagram

The PD69101 is based on two major sections (see Figure 1):

1. A Digital section which controls and monitors the logical PoE functions (state machines, timings etc.)
2. An Analog section which performs the Front End analog PoE functionality.

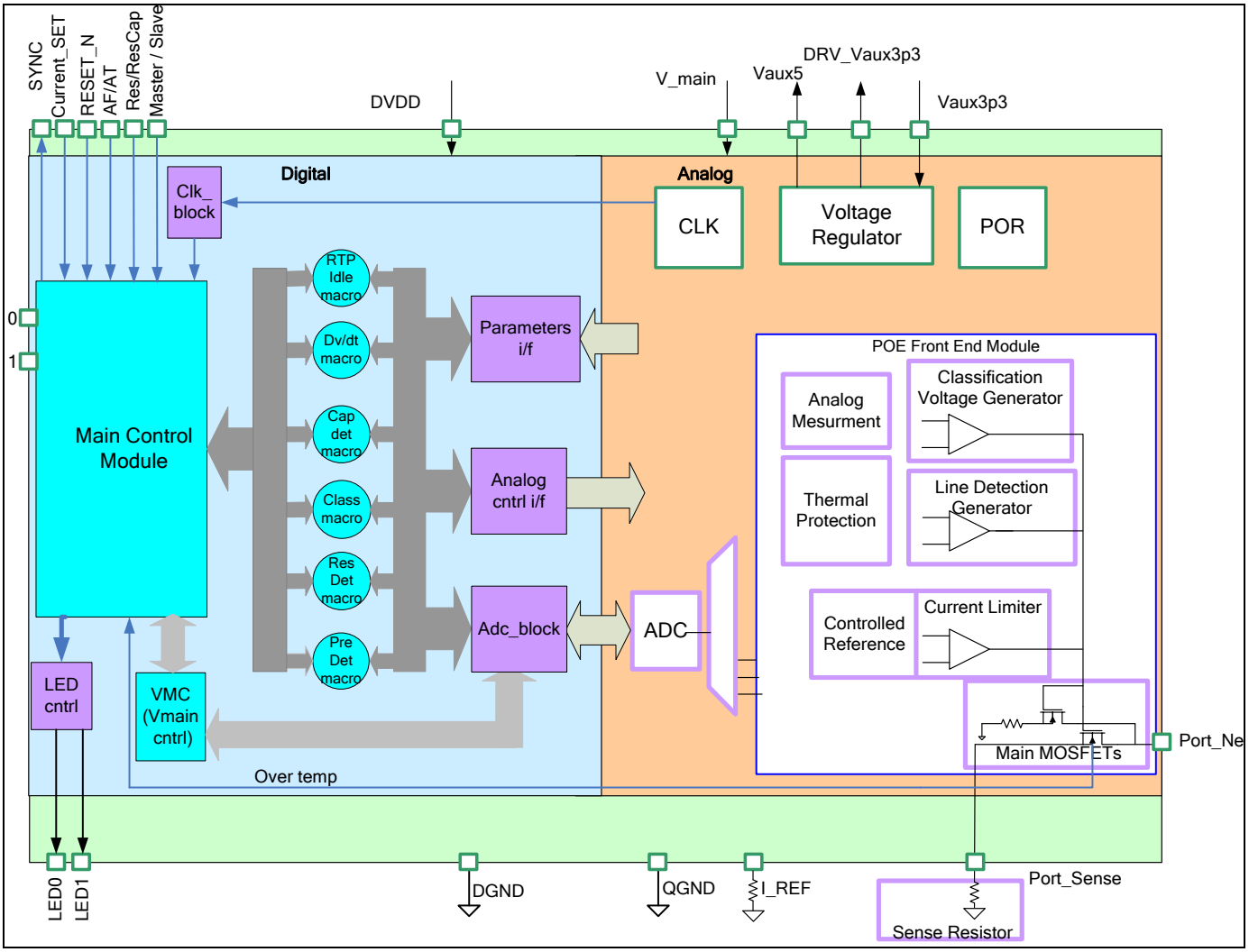

Figure 1: PD69101 Internal Block Diagram

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Logic Main Control Module

The Logic Main Control Block includes the Digital Timing Mechanisms and State Machines, synchronizing and activating the PoE functions such as:

- Real Time Protection (RTP)
- Start Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring Registers (VMC)
- LEDs Stream Out Control Indications
- ADC Interfacing
- Direct Digital Signals with Analog Block

Line Detection Generator

Upon request from the Main Control Module, four different voltage levels are generated by the Line Detection Generator, ensuring robust AF / AT Line Detection functionality.

Classification Generator

Upon request from the Main Control Module, the State Machine applies a regulated Class Event and Mark Event voltages to the ports, as required by the IEEE standard.

Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a specific value, according to pre-defined limits as set by AF/AT and Current_Set pins. In cases where the current exceeds this specific level, the system starts measuring the elapsed time. If this time period is greater than a preset threshold, the port is disconnected.

Main MOSFET

Main power switching FET, used to control PoE current into the load.

ADC

A 10-Bit Analog to Digital converter, used to convert analog signals into digital registers for the Logic Control module.

Power on Reset (POR)

This circuit monitors the internal 3.3 V voltage DC levels. If this voltage drops below specific thresholds, a reset signal is generated and the PD69101s are reset.

Voltage Regulator

The voltage regulator generates 3.3 VDC and 5 VDC for the internal circuitry. These voltages are derived from the Vmain supply.

CLK

CLK is an internal 8 MHz clock oscillator.

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Theory of Operation

The PD69101 performs IEEE802.3af, IEEE802.3at functionality as well as legacy (capacitor) and Cisco's PDs detection, as well as additional protections such as short circuit and dV/dT protection upon startup.

Line Detection

The Line Detection feature detects a valid AF or AT load, as specified in the AF / AT standard. Resistor value should range from 19 kΩ to 26.5 kΩ. Line detection is based on four different voltage levels generated over the PD (the load) as illustrated in Figure 2.

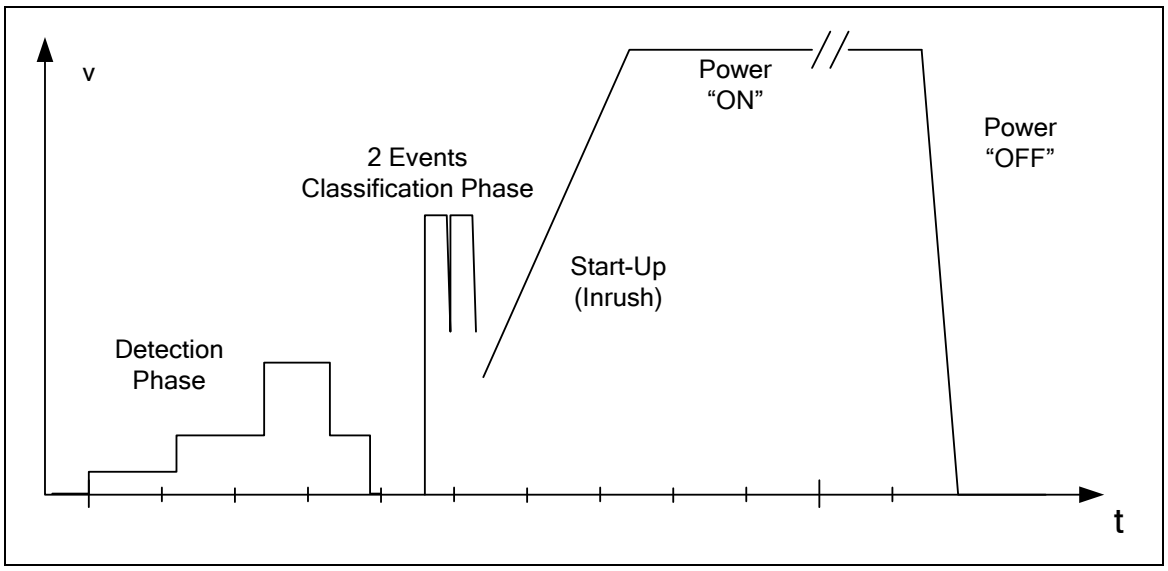

Figure 2: Typical PoE Voltage Time Diagram

Legacy (Cap) Detection

In cases where pin 24 (LEGACY) is set to "0", the PD69101's detection mechanism is configured to detect and power up LEGACY PDs, as well as AF/AT compliant PDs.

This mechanism detects and powers up CISCO Legacy PDs as well.

Classification

The classification process takes place right after the resistor detection, when the resistor detection has completed successfully. The main goal of the classification process is to detect the PD class, as specified in the IEEE802.3AF and AT standards.

In the AF mode the classification mechanism is based on a single voltage level (single finger).

In the AT mode classification mechanism is based on two voltage levels (dual finger) as defined in the IEEE802.3at-2009.

Port Start Up

Upon a successful Detection and Classification process, power is applied to the load via a controlled Start Up mechanism.

During this period current is limited to 425 mA for a typical duration of 65 mS, which enables the PD load to charge and to enter a steady state power condition.

Over-Load Detection and Port Shut Down

After power up, the PD69101 automatically initializes its internal protection mechanisms utilized to monitor and disconnect power from the load in cases where extreme conditions such as over-current or short ports terminals scenario occur, as specified in the IEEE802.3AF/AT standard.

Disconnect Detection

The PD69101 supports DC Disconnect function as per the IEEE802.3AF/AT standard.

This mechanism continuously monitors load current and disconnects power in cases where load current is below 7.5 mA (typ.) for more than 322 mS.

Over-temperature Protection

The PD69101 has internal temperature sensors that continuously monitor junction temperature and disconnect load power when the junction temperature exceeds 200° C. This mechanism protects the device from extreme events, such as high ambient

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temperature or other thermo-mechanical failures that may damage the PD69101.

V_{MAIN} Out of Range Protection

The PD69101 automatically disconnects port power when Vmain exceeds 60 VDC. This is an extremely valuable feature which protects the load if the main power source is faulty or damaged.

TYPICAL 2 PAIRS APPLICATION

This typical application Illustrates a simple “plug and play” Power Over Ethernet solution for a single Ethernet port switch or hub.

“POS” and “NEG” signals should be connected to the switch RJ45 Jack.

AF and AT modes of operations are set through AF/AT and current set pins (DGND or DVDD).

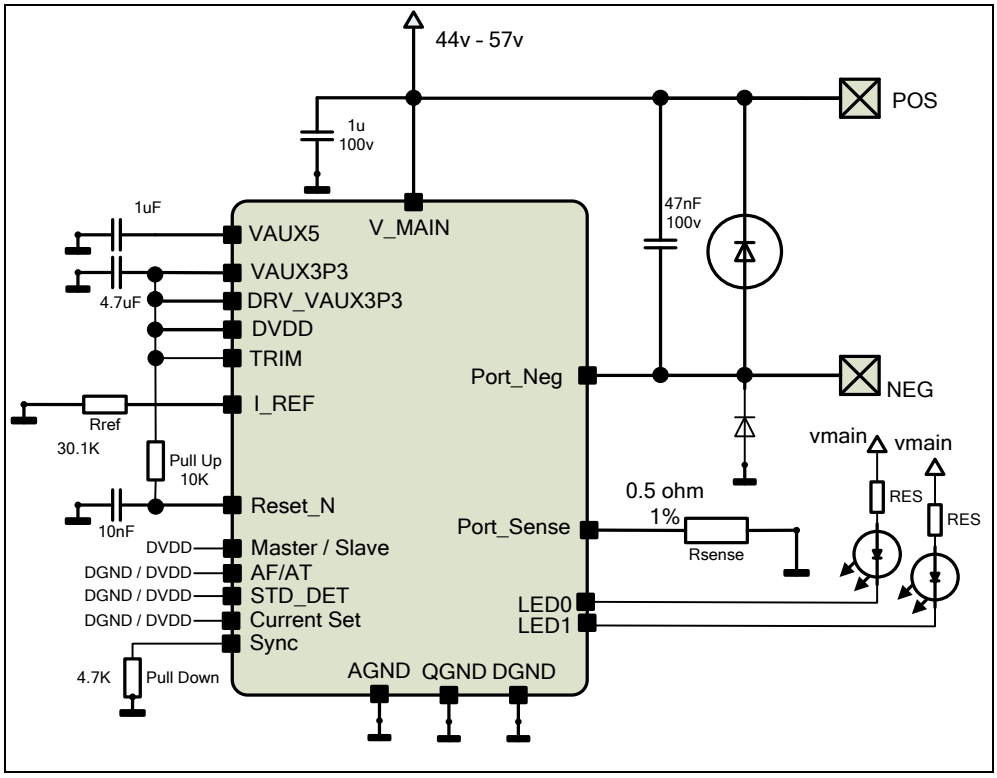

Figure 3: Typical 2 Pair Application

* For detailed application's schematics and layout recommendations, contact sales_AMSG@microsemi.com.

TYPICAL 4 PAIRS APPLICATION

This typical application Illustrates a master / slave “plug and play” Power over Ethernet solution for 4 Pairs (date and spare Wires) Ethernet port switch or hub.

“POS” and “NEG” signals are connected to the switch RJ45 jack via line transformers.

AF and AT modes of operations are set through AF/AT and current set pins (DGND or DVDD).

The SYNC pins are used to synchronize the PD69101 Master to the PD69101 Slave so that line detection, classification, power on and power off events are inline with the load.

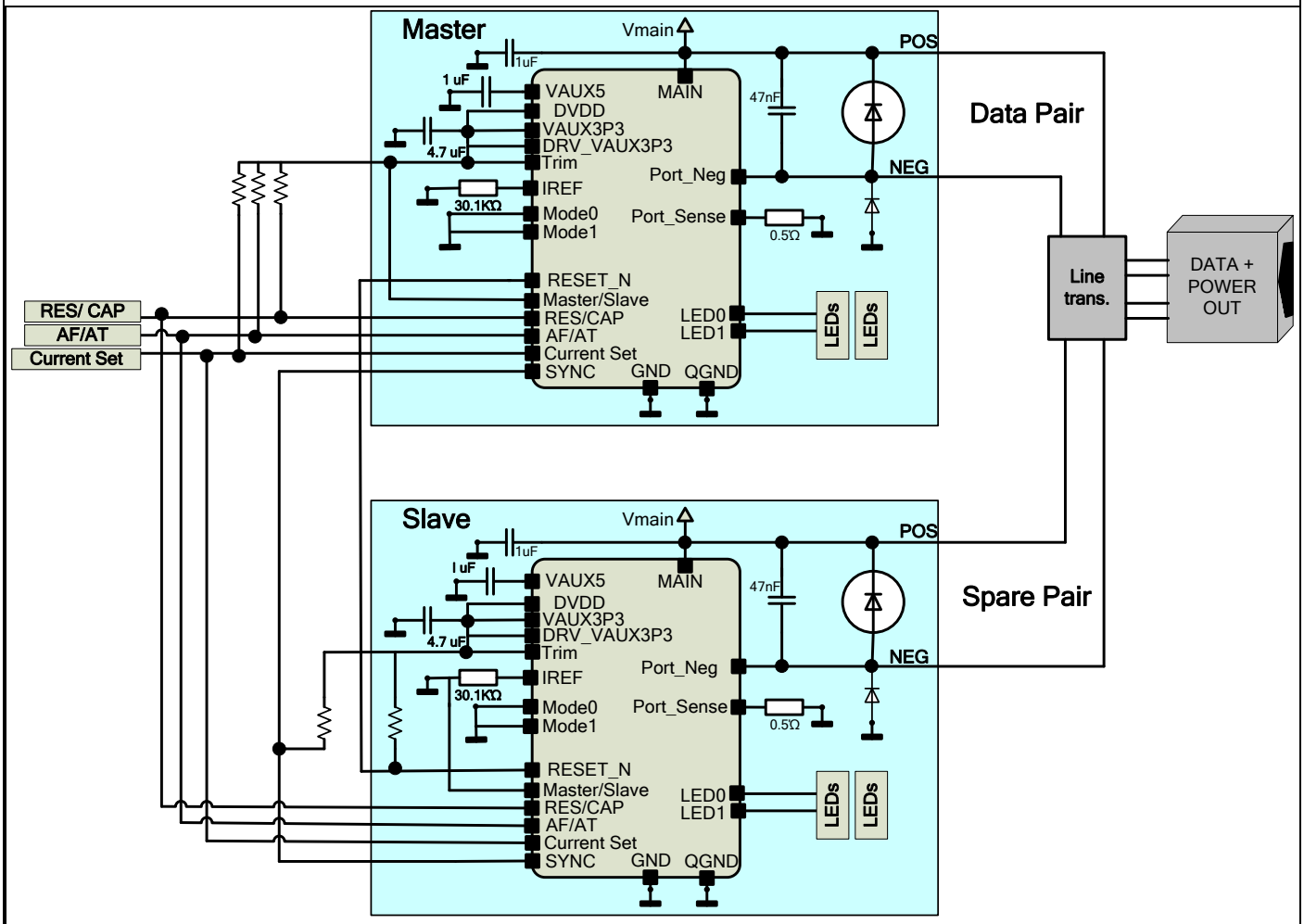

Figure 4: Typical 4 Pair Application

* For detailed application's schematics and layout recommendations, contact sales_AMSG@microsemi.com.

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4 PAIR TYPICAL TIMING DIAGRAM

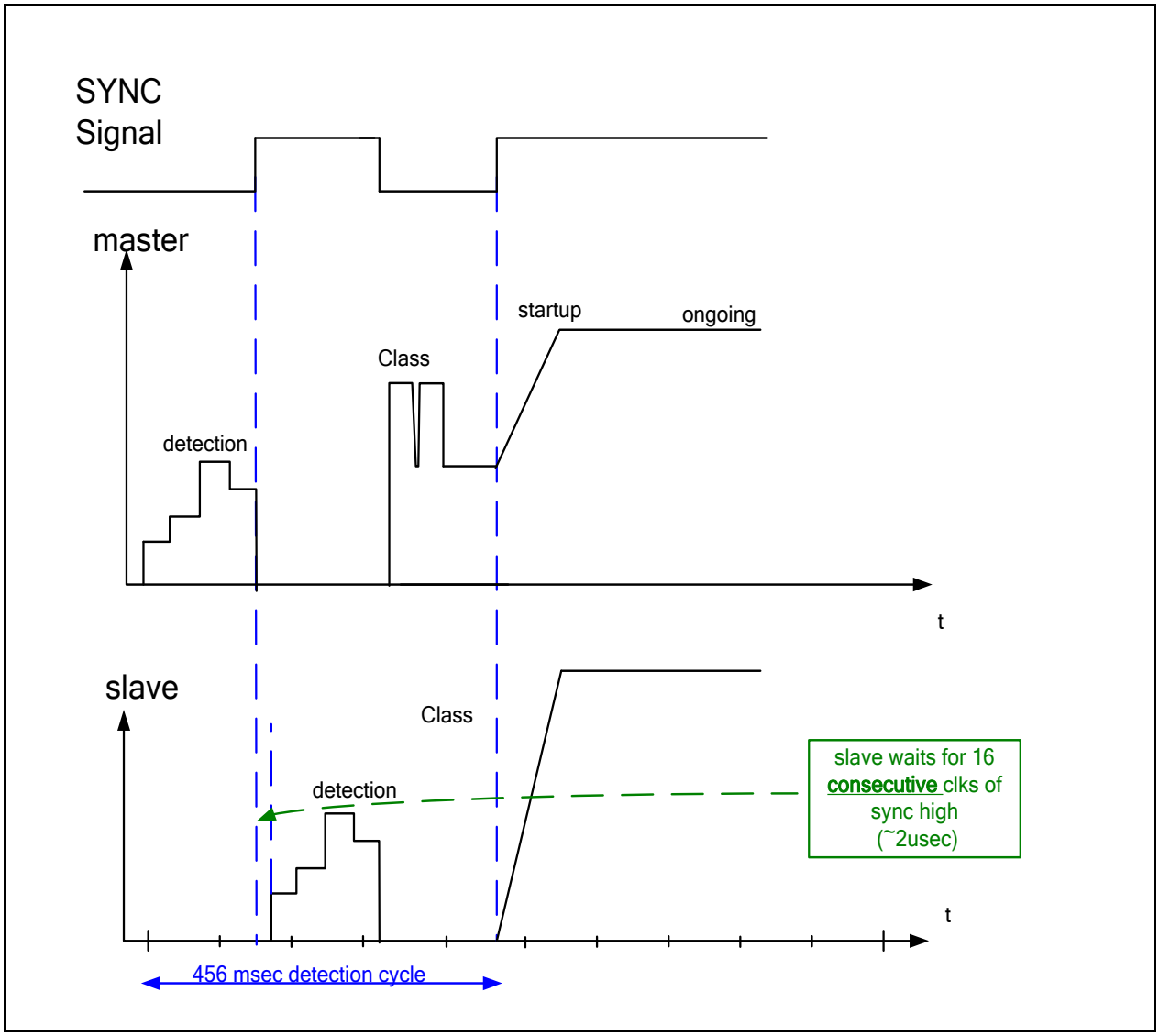

Figure 5: 4 Pair Timing Diagram

Serial Communication - Monitoring Mode

When Mode0 and Mode1 Input pins are configured to Serial Monitoring Mode ("01"), the PD69101 transmits out (continuously and repeatedly) the content of 9 internal registers:

- Data Out Stream is transmitted through LED1 (pin 14)
- Clock Out Stream is transmitted through LED0 (pin 13)
- Data stream is shifted out with a 1 MHz clock (1 µsec).
- Total transaction packet length is 116 µsec.
- The transmission is repeated every 1 msec.
- Between transactions the clock is held low, while data stream out is stable high/low.

Note: To exploit LED1 and LED0 to communicate and monitor transmissions, use a 1 KΩ pull-up resistor to the DVDD.

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Table 5: Stream Out Data Transmits 116 bits Starting from MSB to LSB

MSBYTE								LSBYTE
INTERNAL 0	INTERNAL 1	INTERNAL 2	INTERNAL 3	INTERNAL 4	VPORT	VMAIN	IPORT	PORT STATUS
13 BITS	10 BITS	23 BITS	16 BITS	16 BITS	10 BITS	10 BITS	13 BITS	5 BITS
78 internal signals used for internal tests					Port voltage measurement LSB = 58 mV V = Decimal x 58 mV	Vmain voltage measurement LSB = 58 mV V = Decimal x 58 mV	Port current measurement LSB = 238 uA I = Decimal x 238 uA	Real time port status indication See coding table below

Table 6: Port Status Coding

BINARY MSB TO LSB	DECIMAL VALUE	DESCRIPTION
00000 00001 00010	0 1 2	POE idle state
00011	3	Searching phase
00100	4	Res detection phase
00101 00110	5 6	Back off phase
00111 01000	7 8	Class phase
01001 01010 01100	9 10 12	Wait for start up
01011	11	Cap detection
01101 01110	13 14	Start up
01111 10000	15 16	On going
10001	17	UDL
10010	18	Overload or short circuit
10011 10100	19 20	Vmain out of range

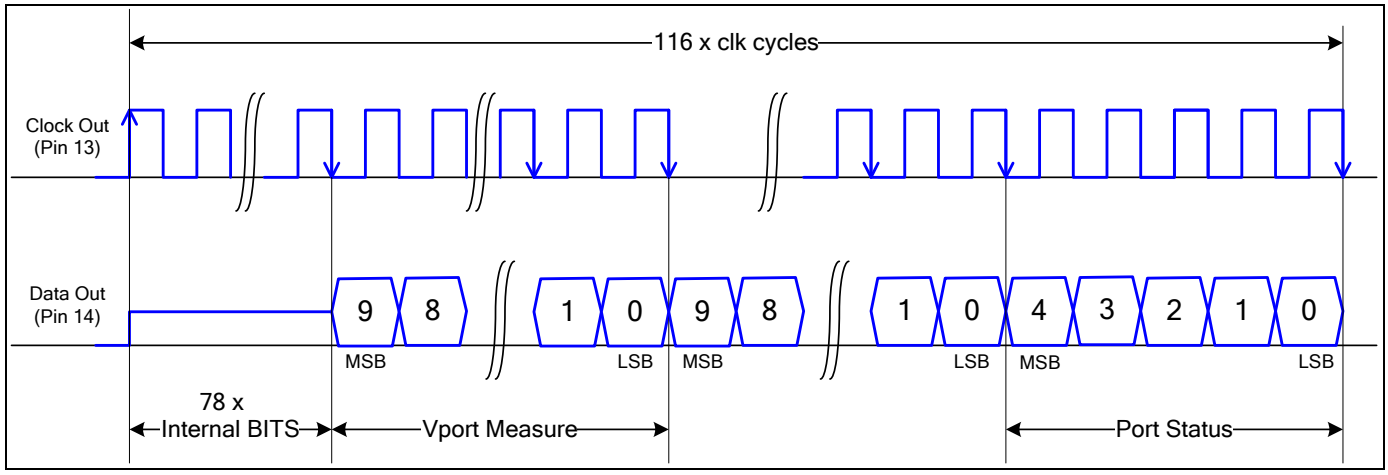

Figure 6: Data Stream Out

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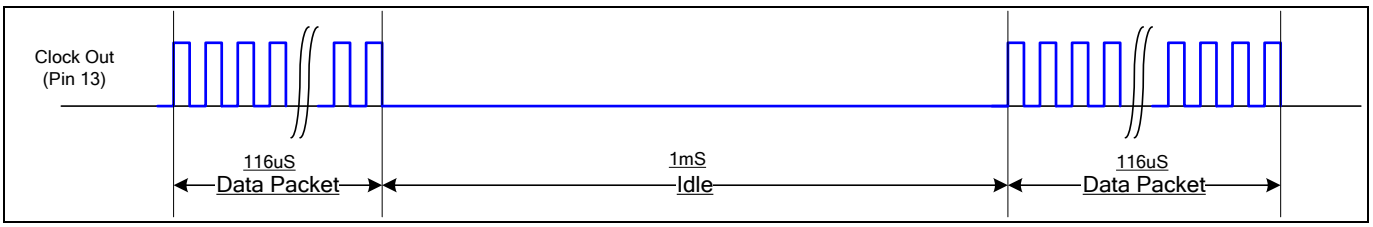

Figure 7: Multi Packet Idle Time (Between Packets)

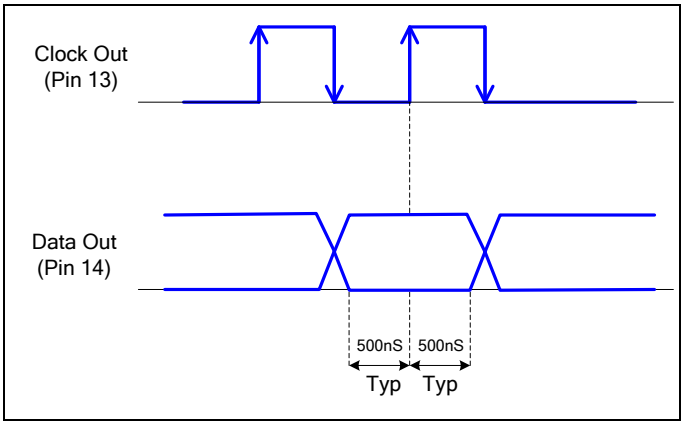

Figure 8: Data / Clock Typical Timing

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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / March 2010		Official Release
1.1 / March 2010		Added wave forms + last functionality update according to evaluation results
1.2 / June 2010		Package drawing update
1.3 / June 2010		Parameters update
1.4 / Sep 2010		Parameters update
1.5 / Dec 2010		Parameters update
1.6 / July 2013		IC marking update
1.7 / July 2013		Add TETA JC data

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