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PD69104B

4 Port PSE PoE Manager

PRODUCTION DATASHEET

Introduction

DESCRIPTION

Microsemi's PD69104B Power over Ethernet (PoE) Manager enables network devices to share power and data over a single cable. The PD69104B PoE Manager chip is employed by both Ethernet switches and Midspans. The device integrates power, analog circuitry and state of the art control logic into a single 48-pin plastic QFN package.

The PD69104B device is a 4 port, mixed-signal, high-voltage PoE Manager. The PD69104B supports 3 modes of operation:

- MSCC Extended Auto mode – this is a stand-alone mode in which the PD69104B detects IEEE802.3af-2003 compliant PDs (Powered Devices) and IEEE802.3at-2009 High Power devices, ensuring safe power feeding and disconnection of ports based on a power management algorithm while employing a minimum of external components.
- Semi Auto mode – allows the host to control which devices are powered and which are not, as well as to communicate with the PD69104B and to configure it
- Auto mode – allows turning PDs on and off automatically. Used for systems with a full power supply.

The PD69104B executes all real time functions as specified in the IEEE802.3af-2003 ("AF") and IEEE802.3at High Power ("AT") standards, including load detection, "AF" and "AT" classifications, and using Multiple Classification Attempts (MCA).

The PD69104B, supports detect legacy/pre-standard PD devices. It also provides PD real-time protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short-circuit. The PD69104B supports supply voltages between 44V and 57V with no need for additional power supply sources and has a built-in thermal protection.

The PD69104B is a low power device that uses internal MOSFETs and external 0.36Ω sense resistors.

The PD69104B is available in 48 leads, 8 mm x 8 mm QFN package.

KEY FEATURES

- Supports IEEE802.3af and IEEE802.3at, including two-event classification
- MSCC Extended Auto, Semi Auto, and Auto modes
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44V to 57V)
- Wide temperature range: -10° to +85°C
- Low power dissipation (0.36Ω sense resistor)
- Drives independent 2-pair power port
- Supports Extended PoE Protocol and Register Map
- Includes 2 selectable communication modes (I2C and UART)
- Includes Reset command pin
- Continuous monitoring port and system data
- Parameter setting using input pins
- Parameters setting from external serial EEPROM device
- Built-in Dynamic Power Management and Emergency Power Management mechanisms with 4 x Power Supply Power Good pins
- Power soft start mechanism
- On-chip thermal protection
- On-chip continual thermal monitoring
- Voltage/current and temperature monitoring/protection
- Built-in 3.3V and 5V regulators
- Internal power on reset
- MSL1, RoHS compliant

IMPORTANT: For the most current data, consult MICROSEMI's website: http://www.microsemi.com

PACKAGE ORDER INFO

T_A (°C)	Plastic 48 pin QFN 8x8 mm RoHS Compliant / Pb-free, MSL1
-10 to +85	**PD69104BILQ**

Note: Available in Tape and Reel. Append the letters "TR" to the part number. (i.e PD69104BILQ-TR)

THERMAL DATA

THERMAL RESISTANCE-JUNCTION TO AMBIENT	25° C/W
THERMAL RESISTANCE-JUNCTION TO CASE	4° C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

TYPICAL POWER DISSIPATION INFORMATION

R_{sense} Power Dissipation: 0.36Ω x I_{port}^2
R_{ds_ON} Power Dissipation: 0.3Ω x I_{port}^2
P_{port_AF} = 15.4W ==> Port Power Dissipation @ R_{sense} = 37mW (320mA)
Port Power Dissipation @ R_{ds_ON} = 31mW (320mA)
P_{port_AT} = 30W ==> Port Power Dissipation @ R_{sense} = 130mW (600mA)
Port Power Dissipation @ R_{ds_ON} = 108mW (600mA)

Using Internal 3.3V regulator

Typical PD69104B self power dissipation (including internal regulations) = 0.5W (50V)

Typical PD69104B @ 4 x Port AF application power dissipation = 0.5W + 4 x 31mW + 4 x 37mW = 0.77W

Typical PD69104B @ 4 x Port AT application power dissipation = 0.5W + 4 x 108mW + 4 x 130mW = 1.45W

Using External 3.3V regulator

Typical PD69104B self power dissipation (external 3.3V source) = 0.25W (50V)

Typical PD69104B @ 4 x Port AF application power dissipation = 0.25W + 4 x 31mW + 4 x 37mW = 0.52W

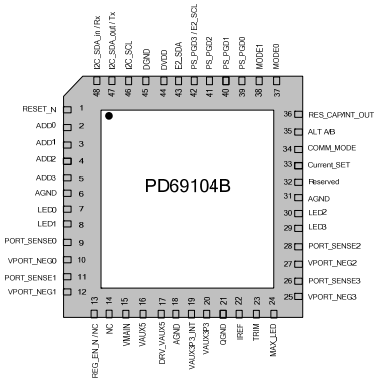
Typical PD69104B @ 4 x Port AT application power dissipation = 0.25W + 4 x 108mW + 4 x 130mW = 1.2W

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{MAIN})	-0.3V_{DC} to 74V_{DC}
Port_Neg[0..7] pins	-0.3V_{DC} to 74V_{DC}
LED pins	-0.3V_{DC} to 74V_{DC}
Port_Sense[0..7] pins	-0.3V_{DC} to 3.6V_{DC}
QGND, GND pins	-0.3V_{DC} to 0.3V_{DC}
VAUX5, DRV_VAUX5	-0.3V_{DC} to 5.5V_{DC}
All other pins	-0.3V_{DC} to 3.6V_{DC}
Operating Ambient Temperature Range	-10° to +85°C
Maximum Operating Junction Temperature	+160°C
ESD Protection at all I/O pins	± 2KV HBM
Storage Temperature Range	-65° to +150°C

Notes:
1. Exceeding these ratings can cause damage to the device. All voltages are with respect to ground. Currents are marked positive when flowing into specified terminals and marked negative when flowing out of specified terminals.

PACKAGE PIN OUT



(Top View)

RoHS / Pb-free 100% Matte Tin Finish

ROHS AND SOLDER REFLOW INFORMATION

RoHS 6/6

Pb-free 100% Matte Tin Finish

Package Peak Temperature for Solder Reflow (40 seconds maximum exposure) 260° C (+0° C, -5° C)

Notes:

Exceeding these ratings can cause damage to the device.

IPC/JEDEC J-STD-020C July 2004

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

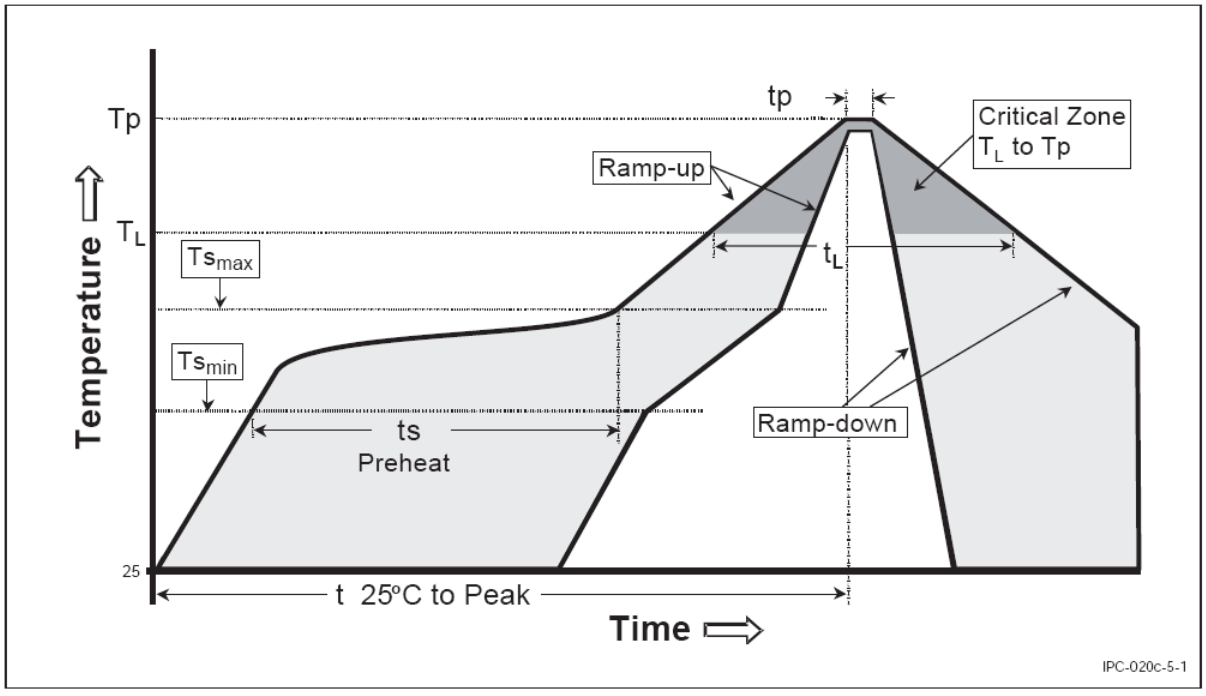


Figure 5-1 Classification Reflow Profile

Table 4-2 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.

Electrical Characteristics

Unless otherwise specified, the following specifications apply to the operating ambient temperature, -10° to +85°C.

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69104B MANAGER MIN	TYP	MAX	UNITS
POWER SUPPLY						
Input Voltage	V_{MAIN}	Supports Full IEEE802.3 functionality	44	55	57	V_{DC}
Power Supply Current @ Operating Mode	I_{MAIN}	V_{MAIN} = 55V		10		mA
5V Output Voltage	V_{AUX5}		4.5	5	5.5	V_{DC}
3.3V Output Voltage	V_{AUX3P3}		2.97	3.3	3.63	V_{DC}
3.3V Output Current		Without external NPN			5	mA
		With external NPN transistor on VAUX5			30	mA
3.3V Input Voltage	V_{AUX3P3}	REG_EN_N pin = 3.3V (internal reg. is disabled) VAUX3P3_INT=5V	3	3.3	3.6	V_{DC}
POWER ON RESET (POR)						
Threshold			2.575	2.775	2.975	V_{DC}
Hysteresis			0.2	0.25	0.3	V_{DC}
Delay			10	50	100	µS

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69104B MANAGER MIN	TYP	MAX	UNITS
DIGITAL I/O						
Input Logic High Threshold	V_{IH}		2			V_{DC}
Input Logic Low Threshold	V_{IL}				0.8	V_{DC}
Input Hysteresis Voltage			0.4	0.6	0.8	V_{DC}
Input High Current	I_{IH}		-10		10	µA
Input Low Current	I_{IL}		-10		10	µA
Output High Voltage	V_{OH}	For I_{OH} = -1 mA	2.4			V_{DC}
Output Low Voltage	V_{OL}	I_{OH} = 1 mA			0.4	V_{DC}
POE LOAD CURRENTS						
AT Limit Mode	AT_LIM_LOW	Tested With Sense resistance = 0.366 Ω (Rsense+Traces = 0.36 Ω+6mΩ=0.366 Ω) connected at port_sense pin	706	722	767	mA
	AT_LIM_HIGH		847	874	919	mA
	AT configurable		537		1200	mA
AF Limit Mode	AF_LIM		410	425	448	mA
PoE Tech High Power Port			808	850	892	mA
MAIN POWER SWITCHING FET						
On Resistance	R_{DSON}			0.3		Ω
Internal Thermal Protection Threshold				200		°C
LINE DETECTION						
Range		According to IEEE802.3 standard	19		26.5	KΩ
CLASSIFICATION						
Class Event Output Voltage		Measured between VMAIN and VPORT_NEG pins	16.5	18	19.5	V_{DC}
Mark Event Output Voltage		Measured between VMAIN and VPORT_NEG pins	7.5	8.5	9.5	V_{DC}

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69104B MANAGER MIN	TYP	MAX	UNITS
LED0 TO 3, POE_MAX DRIVERS						
Current Sink	I sink (from VMAIN to AGND)			3	5	mA
3 STATES ANALOG INPUT PINS (CURRENT SET, COMM_MODE)						
High Level input voltage			80% V_{AUX3P3}			V_{DC}
Open		Not Connected	40% V_{AUX3P3}		60% V_{AUX3P3}	V_{DC}
Low level input voltage					20% V_{AUX3P3}	V_{DC}

Dynamic Characteristics

The PD69104B utilizes three current level thresholds (I_{min}, I_{cut}, I_{lim}) and three timers (T_{min}, T_{cut}, T_{lim}).

- Loads that consume I_{lim} current for more than T_{lim} are labeled as 'short circuit state' and are shutdown.
- Loads that dissipate more than I_{cut} for longer than T_{cut} are labeled as 'overloads' and are shutdown.
- If output power is below I_{min} for more than T_{min}, the PD is labeled as 'no-load' and is shutdown.

Automatic recovery from overload and no-load conditions is attempted every T_{OVLREC} period (typically 1 second). Output power is limited to $I_{lim,}$ which is the maximum peak current allowed at the port.

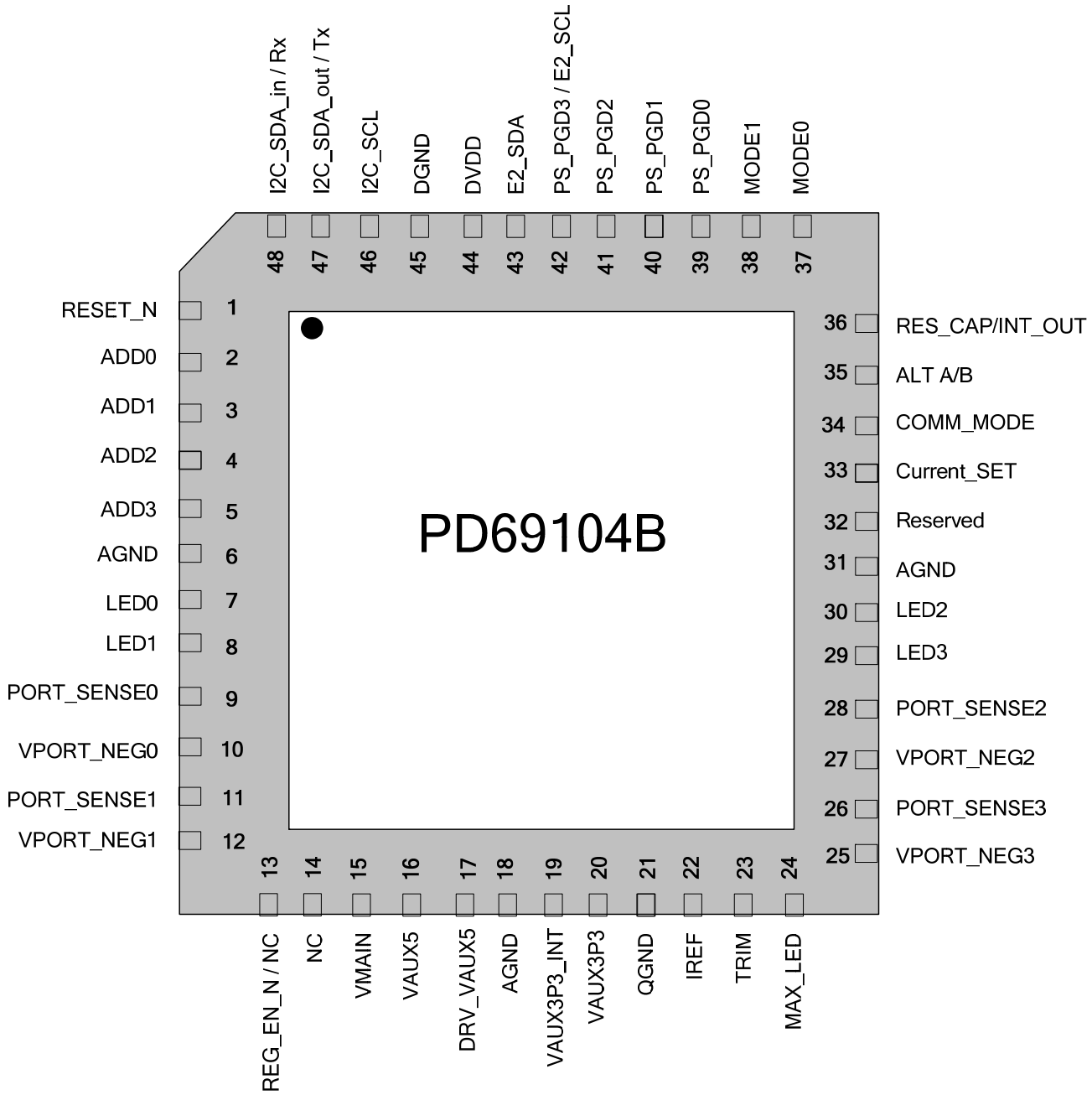
Table 1: IEEE802.3 AF Mode Parameters

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic Recovery from No-load Shutdown	T_{UDLREC} value, measured from port shutdown point (can be modified through control port)			1		Sec
Cutoff timers Accuracy	Typical accuracy of T_{cut}			2		ms
Inrush Current	I_{Inrsh}	For t = 50ms, C_{load} = 180µF max.	400		450	mA
Output Current Operating Range	I_{port}	Continuous operation after startup period	10		375	mA
Output Power Available Operating Range	P_{port}	Continuous operation after startup period, at port output	0.57		15.4	W
Off mode Current	I_{min1}	Must disconnect for T greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
PD Power Maintenance Request Drop-out Time Limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Overload Current Detection Range	I_{cut}	Time limited to T_{OVL}	350		400	mA
Overload Time Limit	T_{OVL}		50		75	ms
Turn On Rise Time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100µF capacitor parallel to 200Ω resistor)	15			µs
Turn Off Time	T_{off}	From V_{port} to 2.8V_{DC}			500	ms
Time Maintain Power Signature	T_{MPS}	DC modulation time for DC disconnect		49		ms

Table 2: IEEE802.3 AT Mode Parameters

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic Recovery from No-load Shutdown	T_{UDLREC} value; measured from port shutdown point (can be modified through control port)			1		s
Cutoff Timers Accuracy	Typical accuracy of T_{cut}			2		ms
Inrush Current	I_{Inrsh}	For t = 50ms, C_{load} = 180µF max.	400		450	mA
Output Current Operating range	I_{port}	Continuous operation after startup period	10		725	mA
Output Power Available, Operating Range	P_{port}	Continuous operation after startup period at port output	0.57		36	W
Off Mode Current	I_{min1}	Must disconnect where T is greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
PD Power Maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Overload Time Limit	T_{OVL}		50		75	ms
Turn-on Rise Time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100µF capacitor parallel to 200 Ω resistor)	15			us
Turn-off Time	T_{off}	From V_{port} to 2.8V_{DC}			500	ms
Time Maintain Power Signature	T_{MPS}	DC modulation time for DC disconnect		49		ms

Package and Pinout



Detailed Pinout Description

PIN	PIN NAME	PIN TYPE	DESCRIPTION
0.	PAD	Analog GND	Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin whenever possible (refer to PD69104B Layout Design Guidelines)
1.	RESET_N	Digital Input	Reset input – active low ('0' = reset)
2.	ADDR0	Digital Input	Address bus for setting the address of the chip. See Table 3.
3.	ADDR1	Digital Input	Address bus for setting the address of the chip. See Table 3.
4.	ADDR2	Digital Input	Address bus for setting the address of the chip. See Table 3.
5.	ADDR3	Digital Input	Address bus for setting the address of the chip. See Table 3.
6.	AGND	Power	Analog ground
7.	LED0	Analog output	Port 0 LED indication – active low ('0' = LED on) See Table 5
8.	LED1	Analog output	Port 1 LED indication – active low ('0' = LED on) See Table 5
9.	PORT_SENSE0	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
10.	VPORT_NEG0	Analog I/O	Negative port output
11.	PORT_SENSE1	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
12.	VPORT_NEG1	Analog I/O	Negative port output
13.	REG_EN_N	Analog I/O	An input pin that enables control of the $3.3V_{DC}$ internal regulator. Disables internal $3.3V_{DC}$ regulator in case external $3.3V_{DC}$ is used to supply the chip. If connected to GND – internal regulator is enabled. If connected to $3.3V_{DC}$ – internal regulator is disabled
14.	NC	Analog I/O	A test pin used only during production. Keep unconnected.
15.	VMAIN	Power	Supplies voltage for the internal analog circuitry. A 1µF (or higher) low ESR bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
16.	VAUX5	Power	Regulated $5V_{DC}$ output voltage source, needs to be connected to a filtering capacitor of 4.7µF or higher. If an external NPN is used to regulate the voltage, connect this pin to the "Emitter" (the "collector" should be connected to VMAIN).
17.	DRV_VAUX5	Power	Driven outputs for $5V_{DC}$ external regulations. In case internal regulation is used, connect to pin 16. In case an external NPN is used to regulate the voltage, connect this pin to the "Base".
18.	AGND	Power	Analog ground
19.	VAUX3P3_INT	Power	In case internal 3.3 V_{DC} regulator is used, connected to VAX3P3 (pin 20). In case external $3.3V_{DC}$ regulator is used, connect to VAUX5 (pin 16).

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20.	VAUX3P3	Power	Regulated 3.3V_{DC} output voltage source. A 4.7µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3V_{DC} regulator is used, connect it to this pin to supply the chip.
21.	QGND	Power	Quiet analog ground
22.	IREF	Analog Input	A reference resistor pin. A 30.1kΩ, 1% resistor should be connected between this pin and QGND.
23.	TRIM	Test Input	Trimming input for IC production. Should be connected to VAUX3P3.
24.	MAX_LED	Analog output	MAX LED analog output. Indicates the device has exceeded maximum power budget. See Table 5.
25.	VPORT_NEG3	Analog I/O	Negative port output
26.	PORT_SENSE3	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
27.	VPORT_NEG2	Analog I/O	Negative port output
28.	PORT_SENSE2	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
29.	LED3	Analog output	Port 3 LED indication – active low ('0' = LED on) See Table 5
30.	LED2	Analog output	Port 2 LED indication – active low ('0' = LED on) See Table 5
31.	AGND	Power	Analog ground
32.	Reserved	Analog Input	Reserved pin. Must be connected to AGND.
33.	Current_SET	Analog Input	3 state input pin, used for selecting output current and AF/AT mode. • "0" (AGND) – AF mode • "open" (N.C) – Low AT mode 600mA • "1" (V_{DD}) – High AT mode 720mA
34.	COMM_MODE	Analog Input	3 state input pin communication. Following options are available: • "0" (AGND) – UART active • "open" (N.C) – E2PROM connected • "1" (V_{DD}) – I2C active
35.	ALT A/B	Digital Input	Configuration Input Pin, used for setting PD69104B working mode. • GND – ALT B mode = Midspan mode (midsp [0:3] bits ="1") • DVDD – ALT A mode = Endspan mode (midsp [0:3] bits ="0")

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36.	RES_CAP / INT_OUT	Digital I/O	In MSCC Extended Auto mode: User input pin. Used for setting the chip legacy detection mode: • "1" (V_{DD}) – IEEE802.3af compliant resistor detection only • "0" (GND) – AF / AT Detection and Legacy (non-standard) line detection In Auto or Semi-Auto modes: Interrupt out pin. Indicates an interruption event has occurred. An external 10K pull-up resistor should be connected between this pin and DVDD.
37.	Mode0	Digital Input	Used for IC operational mode selection – see Table 4.
38.	Mode1	Digital Input	Used for IC operational mode selection – See Table 4.
39.	PS_PGD0	Digital input	Power Supply Power Good 0; Power Budget Set pin – for Fast Power Control (See Table 6)
40.	PS_PGD1	Digital input	Power Supply Power Good 1; Power Budget Set pin – for Fast Power Control (See Table 6)
41.	PS_PGD2	Digital input	Power Supply Power Good 2; Power Budget Set pin – for Fast Power Control (See Table 6)
42.	PS_PGD3 / E2_SCL	Digital I/O (open drain)	Power Supply Power good 3; Power Budget Set Pin – for initial configuration (See Table 6) *Or (refer to COMM MODE PIN)* E2_SCL: I2C Clock Out to EEPROM When working with EPROM - An external 10K pull-up resistor should be connected between this pin and DVDD.
43.	E2 SDA	Digital I/O (open drain)	EEPROM I2C data I/O pin. Used for Power Up configuration in Stand Alone Auto-Mode systems. An external 10K pull-up resistor should be connected between this pin and DVDD.
44.	DVDD	Power	Digital 3.3V_{DC} power input
45.	DGND	Power	Digital GND
46.	I2C SCL	Digital Input	I2C bus, serial clock input. An external 10K pull-up resistor should be connected between this pin and DVDD.
47.	I2C_SDA_out / Tx	Digital I/O (open drain)	I2C bus, data output / UART Tx output An external 10K pull-up resistor should be connected between this pin and DVDD.
48.	I2C_SDA_in / Rx	Digital I/O (open drain)	I2C bus, data input / UART Rx input An external 10K pull-up resistor should be connected between this pin and DVDD.

Note:

- "0" = Connect to DGND
- "1" = Connect to DVDD

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Table 3: I2C and UART Address Selection Table

CONST BITS	ADDR3 SLAVE 1 BIT	ADDR2 SLAVE 0 BIT	ADDR1 ID1 BIT	ADDR0 ID0 BIT	I2C/ UART ADDRESS
0 1 0	0	0	0	0	0100000b
0 1 0	0	0	0	1	0100001b
0 1 0	0	0	1	0	0100010b
0 1 0	0	0	1	1	0100011b
0 1 0	0	1	0	0	0100100b
0 1 0	0	1	0	1	0100101b
0 1 0	0	1	1	0	0100110b
0 1 0	0	1	1	1	0100111b
0 1 0	1	0	0	0	0101000b
0 1 0	1	0	0	1	0101001b
0 1 0	1	0	1	0	0101010b
0 1 0	1	0	1	1	0101011b
0 1 0	1	1	0	0	0101100b
0 1 0	1	1	0	1	0101101b
0 1 0	1	1	1	0	0101110b
0 1 0	1	1	1	1	0101111b

Notes:

- Address 0000000b is the global address in Extended mode operation I2C/UART (MODE<1:0>='00')
- Address 0110000b is the global address in Auto mode and Semi Auto mode operations (MODE<1:0>='01' or '11')
- All the slaves respond to the global address
- Avoid global read transactions
- Address 0001100b is used for Extended POE address (Alert Response address) in Auto mode and Semi Auto mode operations
- When reading from this Alert Response address, only slaves that assert the Int_out pin will send bytes that consist of their own addresses

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Table 4: Mode of Operation

Mode 1	Mode 0	Mode	Comm. to the IC	Functionality	Remarks
0	0	MSCC Extended Auto Mode	I2C or UART (see COMM_MODE pin)	Fully autonomous operation without a need for Host Controller (MCU) This Mode Supports Extended Registers Map. Default Operation: With No Interrupt Function (Interrupt can be enabled by communication command)	I2C or UART Protocol to Host with extended register map and PM (Power Management) support
0	1	Semi Auto mode	I2C or UART (see COMM_MODE pin)	Host should manage the ports	I2C Protocol to Host
1	0	Test mode			For internal use only
1	1	Auto mode	I2C or UART (see COMM_MODE pin)	Fully autonomous operation without a need for Host Controller. Default Operation: Interrupt Out Function – Enabled (Supported)	I2C Protocol to Host

Table 5: LED Indications

PIN	Status	LED
LED<3:0>	Port Power On	On
	Power Management event	0.4Hz Blink
	Port Over Load Port Short Circuit Port failed at Startup	0.8Hz Blink
	Vmain_Out of Range or Over Temp	All LEDs :3.3Hz Blink
	Port Off	Off
MAX_LED	Total power consumption is below Power Guard Band determined by the user	Off
	Total power consumption is above Power Guard Band but below total budget.	On
	Total power consumption is above total budget, or Power Integral is still positive	Blink

Notes:

MAX_LED:

- Both Max Power Budget and Max LED Guard Band (GB) can be configured through internal registers :
  - Max Power Budget registers: PWR_BNK0 to PWR_BNK7 (address 0x89 to 0x90)
  - Max LED Guard Band register: PoE_MAX_LED_GB (address 0x9F)
- PoE_MAX_LED_GB Register LSB = 1 watt
- Max LED reflects total power for all 4 ports
- When Total Power consumption < (Max Power - Guard Band) Max LED is OFF (below the bottom line)
- When Total Power consumption > (Max Power - Guard Band) Max LED is ON (Between the lines)

- When Total Power consumption > (Max Power) => LED is BLINKING (above top line)
- Also, when Total Power > Budget (above top line):
  - An internal Digital Power Integration Calc. machine starts integrating power
  - When this Integrated total power is larger than Budget + 12.5% (RED LINE) => lowest priority port is turned OFF
  - This specific port LED is OFF
  - Max LED will reflect the NEW Total Power status
  - If ports turn off due to PM their per port LEDs will blink (in PM frequency) and MAX_LED will turn off
  - Timing to shut down this port is proportional to the Over Power (above budget) but limited to max. of 2 sec. – see example:

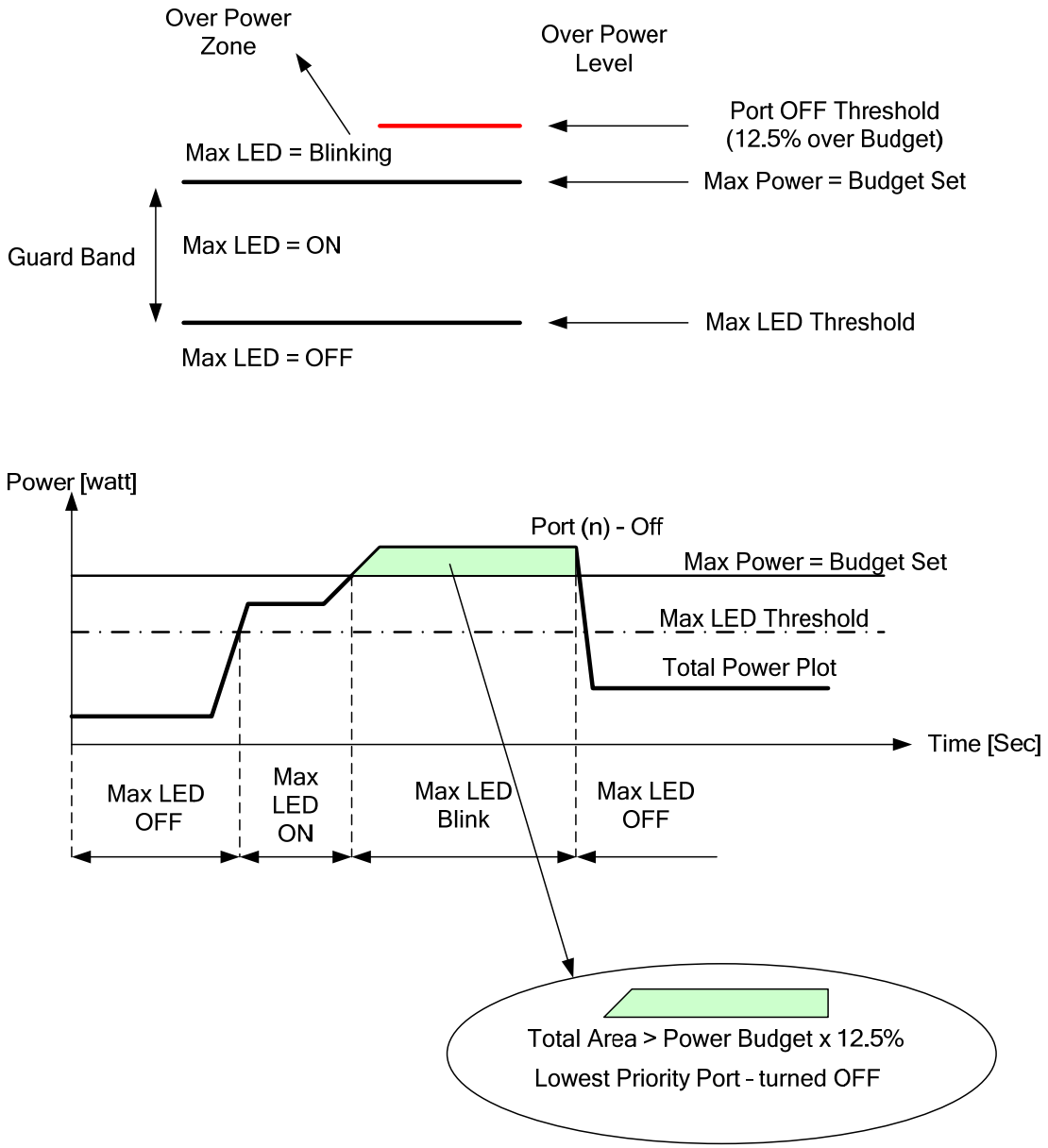

Figure 1: MAX_LED Behavior Description

- For Example:

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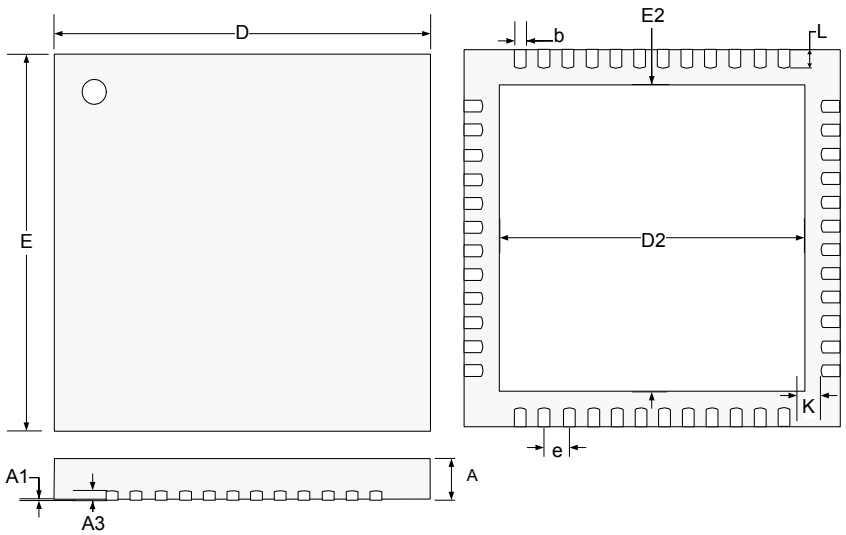
- Budget = 100w, GB = 20w
- When total power = 70w – MAX LED is OFF
- When total power = 85w – MAX LED is ON (Power Integrator is NOT activated)
- When total power = 110w – MAX LED BLINKS (Power Integrator is activated) – Port at Lowest Priority is shut off
- Timing to shut off is based on : **delta(P) x T_{off} = Power Budget x 1.125**
- In this example **10watt x T_{off} = 100watt x 0.125** T_{off} = 1.25 sec.
- If Total Power = 105 watt delta (P) = 5 Then T_{off} = 2 sec. (which is the Max Timer)

Table 6: Power Budget:

PS_PG3 / Bank Range Select	PS_PG2	PS_PG1	PS_PG0	Total Power Budget [W]	Remarks
0	0	0	0	144 (default value in AT low mode) 176 (default value in AT high mode)	Register PWR_BNK0
0	0	0	1	140 (default value)	Register PWR_BNK1
0	0	1	0	136 (default value)	Register PWR_BNK2
0	0	1	1	132 (default value)	Register PWR_BNK3
0	1	0	0	128 (default value)	Register PWR_BNK4
0	1	0	1	124 (default value)	Register PWR_BNK5
0	1	1	0	120 (default value)	Register PWR_BNK6
0	1	1	1	116 (default value)	Register PWR_BNK7
1	0	0	0	112	Constant
1	0	0	1	108	Constant
1	0	1	0	104	Constant
1	0	1	1	100	Constant
1	1	0	0	96	Constant
1	1	0	1	92	Constant
1	1	1	0	88	Constant
1	1	1	1	84	Constant

- There are 16 power levels, whereas the first 8 levels are registers that can be configured by users.
- During operation a change in one of the PG pins will change PD69104B's total power budget and may result in turning off ports.
- The power level can be set either by PS_PG0 to PS_PG3 pins or by Host via communication.

PACKAGE DRAWING



Dim	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 Ref.		0.008 Ref.	
K	0.20 Min.		0.008 Min.	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.35	6.60	0.250	0.260
E2	6.35	6.60	0.250	0.260
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note:
1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

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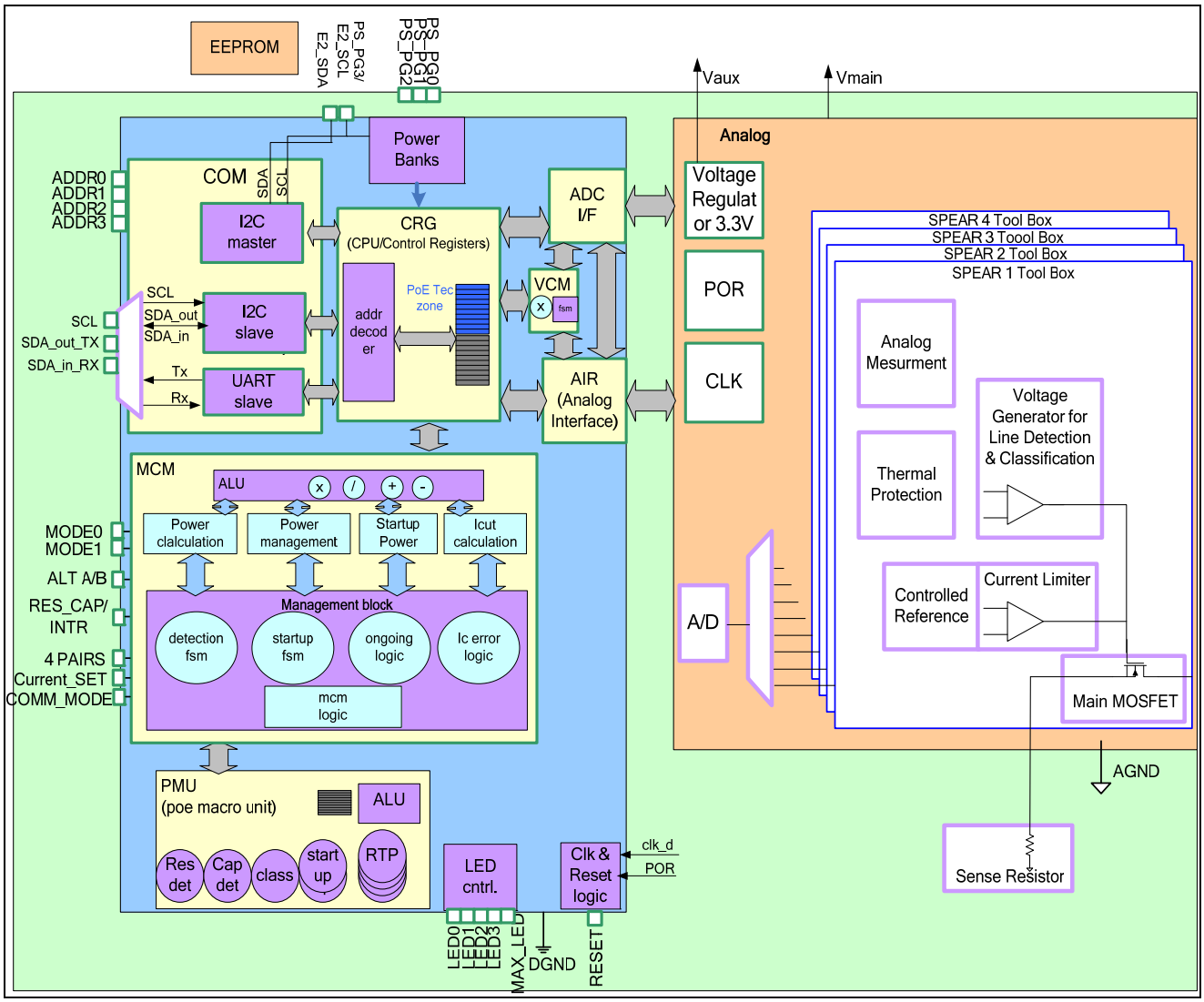
PD69104B - Internal Block Diagram



Logic Main Control Module

The Logic Main Control block includes the Digital Timing mechanisms and the State Machines, synchronizing and activating PoE functions such as:

- Real Time Protection (RTP)
- Start Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring Registers (VMC)
- LEDs Stream Out Control Indications
- ADC Interfacing
- Direct Digital Signals with Analog Block

Line Detection Generator

Upon request from the Main Control module, the Line Detection Generator creates four different voltage levels. Thus it ensures robust AF / AT Line Detection functionality.

Classification Generator

Upon request from the Main Control module, the State Machine applies regulated Class Event and Mark Event voltages to the ports, as required by the IEEE standard.

Current Limiter

This circuit continuously monitors the current of the powered ports and limits it to a specific value, according to pre-defined limits set using the Current_Set pin. In case the current exceeds this specific level, the system starts measuring the elapsed time. If this period is longer than the preset threshold, the port is disconnected.

Main MOSFET

Main power switching FET used for controlling the PoE current that streams into the load.

ADC

A 10-Bit Analog to Digital converter used for converting analog signals into digital registers.

IC main voltage monitoring:

The chip main voltage is sampled every 1mS. Each measurement is an average of 4 consecutive ADC measurements and stored in the relevant register. Main voltage measurement resolution is 5.835mV/count ±5%.

IC Thermal monitoring:

The PD69104B contain a thermal sensor that is sampled to register every 1mS so the PD69104B die temperature can be monitored at all time.

Port current/voltage monitoring:

After port is delivering power each port current/voltage is sampled every 1mS. Each measurement is an average of 4 consecutive ADC measurements and stored in the relevant register. Current measurement resolution is 122.07uA/count ±5% and voltage measurement resolution is 5.835mV/count ±5% (refer to the PD69104B user Guide register map document for more details)

Power on Reset (POR)

This element monitors the internal $3.3V_{DC}$ voltage DC levels. If this voltage drops below specific thresholds, a reset signal is generated and the PD69104B is reset.

Voltage Regulator

The voltage regulator generates $3.3V_{DC}$ and $5V_{DC}$ for the internal circuitry. These voltages are derived from the V_{main} supply.

CLK

An internal 8MHz CLK oscillator

Theory of Operation

The PD69104B meets the IEEE802.3af and IEEE802.3at functionality standards, as well as legacy (capacitor) and Cisco's PDs detection standards. Moreover, it supports additional protections such as short circuit, and dV/dT protection upon port startup.

Line Detection

The Line Detection feature detects a valid 'af' or 'at' load, as specified in the IEEE802.3 standard. The resistance value should range from 19kΩ to 26.5kΩ. Line detection is based on four different voltage levels generated over the PD (the load), as illustrated in Figure 2. The first 2 levels (low voltage level <3v) are for detecting if load up to 200KΩ is connected to the PSE; preventing from applying high voltages on the PSE when there is no-load, and eliminating potential risk to the DTE. If first detection passes next 2 levels of resistor detection are applied. If the POE detects a valid resistor signature value the detection is passed else the detection fails and moves to IDLE.

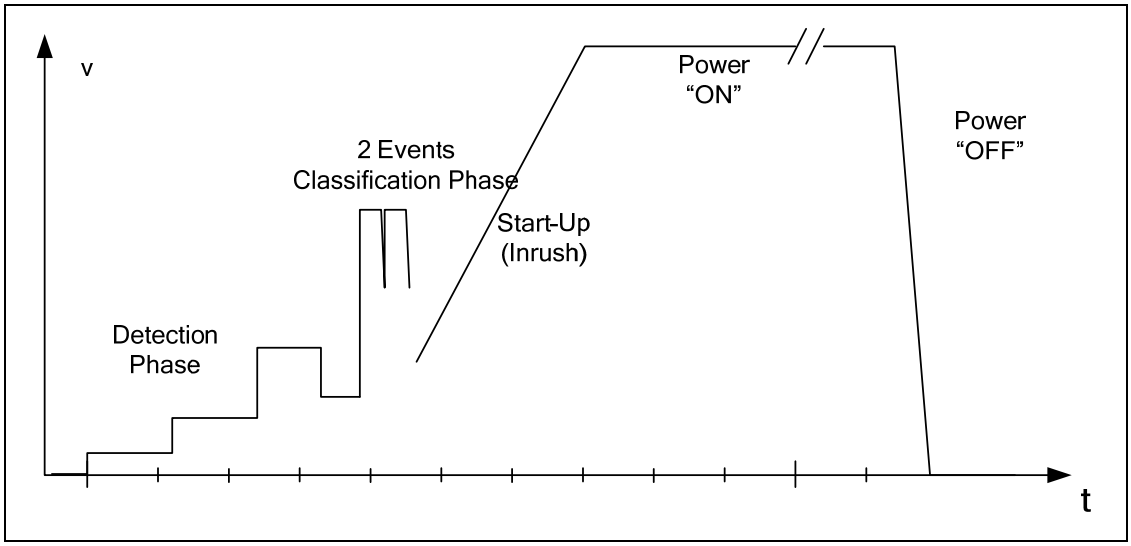


Figure 2: Typical PoE Voltage vs. Time Diagram

Legacy (Cap) Detection

In case pin 36 (RES_CAP / INT_OUT) is set to "0", the detection mechanism of the PD69104B is configured to detect and power LEGACY PDs, as well as AF/AT compliant PDs.

This mechanism also detects and powers CISCO Legacy PDs.

Classification

The classification process takes place right after the resistor detection is successfully completed. The main goal of the classification process is to detect the PD class, as specified in the IEEE802.3AF and AT standards.

In the AF mode the classification mechanism is based on a single voltage level (single finger).

In the AT mode classification mechanism is based on two voltage levels (dual finger) as defined in the IEEE802.3at-2009.

Port Start Up

Upon a successful Detection and Classification process, power is applied to the load via a controlled Start Up mechanism.

During this period current is limited to 425mA for a typical duration of 65ms. This enables the PD load to charge and to enter a steady state power condition.

Over-Load Detection and Port Shut Down

After power up, the PD69104B automatically initializes its internal protection mechanisms. These mechanisms are utilized to monitor and disconnect the power from the load in case of an extreme conditions scenario. Scenarios such as over-current or short ports

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terminals, as specified in the IEEE802.3AF/AT standard.

Disconnect Detection

The PD69104B supports the DC Disconnect function as per the IEEE802.3AF/AT standard.

This mechanism continuously monitors the load current and disconnects the power in case it drops below 7.5mA (typical) for more than 322ms.

Over-temperature Protection

The PD69104B has internal temperature sensors that continuously monitor the junction temperature and set alarm bit when exceeds 120°C or disconnect load power when it exceeds 200°C. This mechanism protects the device from extreme events, such as high ambient temperature or other thermo-mechanical failures that may damage the PD69104B.

The Alarm threshold can be set by register.

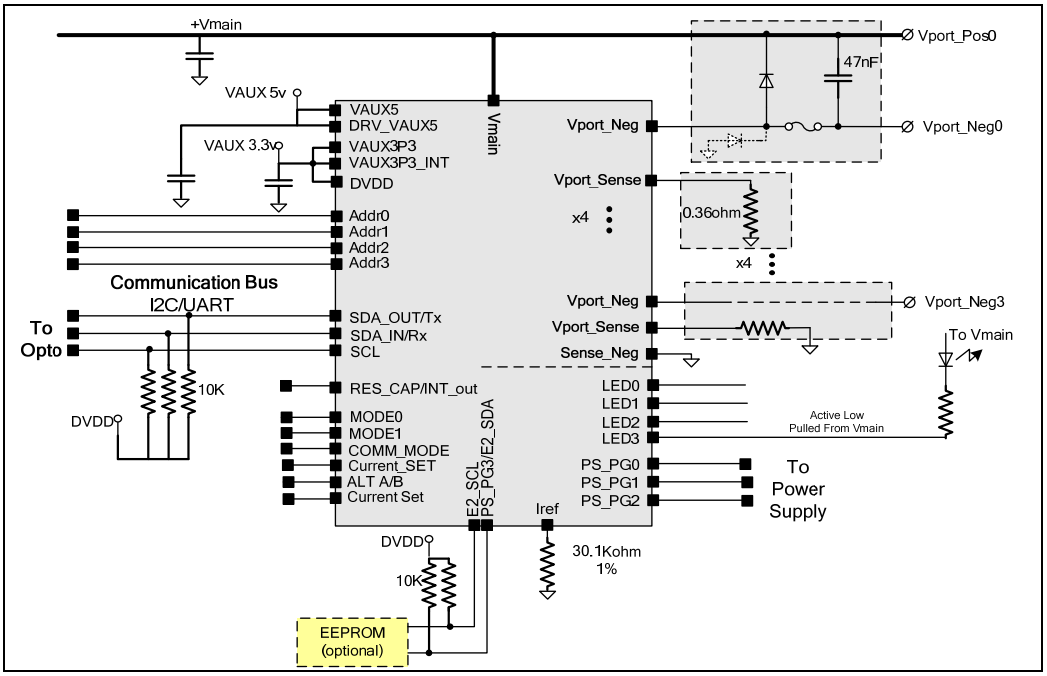
V_{MAIN} Out of Range Protection

The PD69104B automatically disconnects the ports power when V_{main} exceeds 58.5v threshold (with 180mV hysteresis) or drops below 40V threshold (with 180mV hysteresis). This extremely valuable feature protects the load in case the main power source is faulty or damaged.

TYPICAL APPLICATION

This typical application illustrates a simple “plug and play” Power over Ethernet solution for a single Ethernet port, switch or hub.

1. Plug the “POS” and “NEG” signals into the RJ45 switch jack.
2. Set the AF and AT operation modes through AF/AT and the current set pins (DGND or DVDD).



* For detailed schematics of application and layout recommendations contact sales_AMSG@microsemi.com.

Communication Function Description

The following diagram describes the I2C Communication format of the data write/read access:

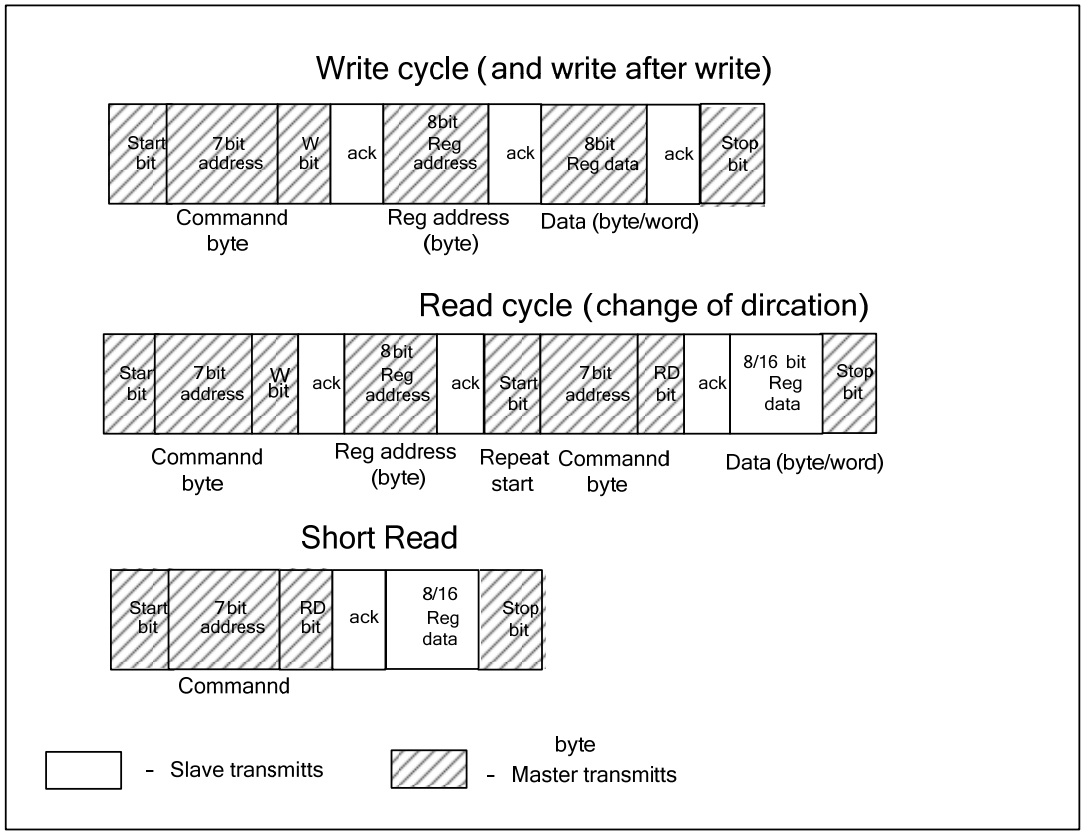


Figure 3: Packet Structure

Address Phase

This phase is common to both read and write accesses:

- Both accesses (read and write) begin with a START indication.
- The address of the slave is following the START indication. In case of a miss match, the slave ignores the rest of the access and waits for the 'STOP' indication to close the current access. However, in case the slave address matches, the next bit indicates the type of the access (read or write).
- The matched slave acknowledges the first byte.
- The following byte is the internal register address. The slave should acknowledge the byte.

Data Phase

In this phase the read and write accesses behave differently.

Write access

1. Byte of write data is transmitted to the slave; the slave acknowledges it.
2. A stop indication from the master closes the current access.

Read access

1. Another command byte is received, comprised of the slave address and the real command type (in this case read). The slave acknowledges the byte.

2. At this stage, the master is ready to continue the communication and to sample the read data; hence, the read data must be **ready** on the next rise of the clock pulse.
3. A byte of data is transmitted to the master; the master acknowledges it.

I2C High Level Layer

The following diagram describes the supported I2C high-level packet structure.

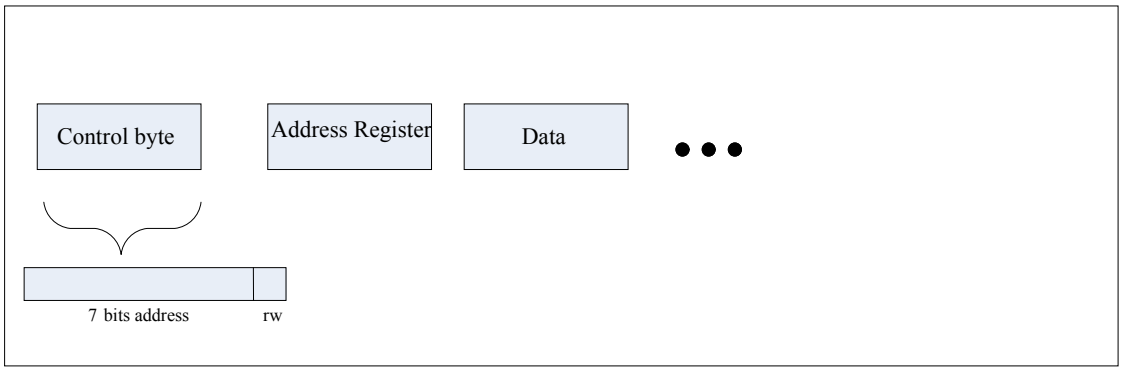


Figure 4: High Level Packet Structure

Byte/Word Read/Write Transaction

1. The first byte is the control byte that consists of the chip address and a read/write operation indication.
2. The second byte is the internal chip's address register.
3. The following bytes/words are data bytes. In case of a read operation they are read from the slave and in case of a write operation they are written to the slave.

Successive Read/Write Transaction

- The master can continue sending bytes that the slaves write, or continue receiving data from a slave during the address phase.
- The slave will continue to send/receive data bytes from/to the master until a 'stop bit' is asserted by the master.
- Each byte received by the slave (or each byte to be read from the registers) is received from the next register address (each byte address is increased by 1).

Read Byte Transaction

The slave supports a 'send byte' transaction.

1. The master begins with a start bit. The following byte consists of the chip address and a read bit.
2. If the chip address is correct the slave acknowledges the byte and immediately (at the next sck phase) sends a data byte from a constant address (addr 7'h00)
3. A send byte transaction continues with successive read transactions (address 1 address 2 and so on) until the master asserts a stop bit.

Broadcast Support

All slaves answer a general address sent by the master. In case of Auto or Semi-Auto modes the general address is **7'h30** and in case of MSCC Extended Auto mode the general address is **7'h0**.

The broadcast is for master writing only; read access is ignored in a broadcast transaction.

Time Out Mechanism

The I2C has an internal counter of 14ms. The counter resets each time the SCL rises or falls. If the SCL is "stuck" for 14ms, the I2C returns to IDLE state and transaction is ignored (the Time Out mechanism is active between the start bit and the stop bit).

I2C Timing Constraints

Table 7: Characteristics of the SDA and SCL Bus Lines for F/S-mode I2C-Bus

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	20 + 0.1C_b(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	20 + 0.1C_b(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1V_{DD}	–	0.1V_{DD}	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2V_{DD}	–	0.2V_{DD}	–	V

Notes

1. All values refer to V_{IHmin} and V_{ILmax} levels (see Electrical Characteristics, page 4).
2. A device must internally provide a hold time of at least 300ns for the SDA signal (refers to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of the SCL.
3. The maximum tHD;DAT has to be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT ³ 250ns must then be met. This is the in case the device does not stretch the LOW period of the SCL signal.
5. If the device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250ns (according to the Standard-mode I2C-bus specification) before the SCL line can be released.
6. n/a = not applicable

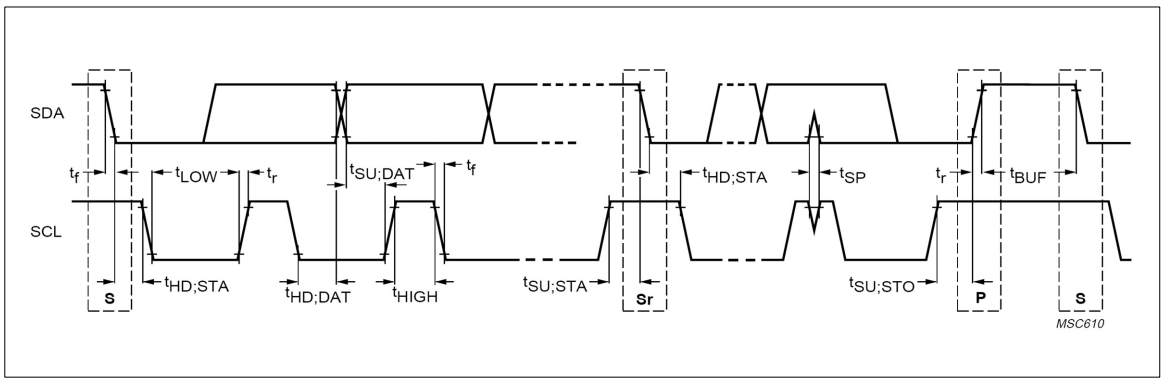


Figure 5: Definition of Timing for F/S-mode Devices on the I2C-bus

UART Communication Mode – Functional Description

The UART (Universal Asynchronous Receive Transmit) is supported by the PD69104B platform in order to allow communication between PD69104B IC's and an external host, **at Auto mode only**.
The PD69104B platform supports UART only as a slave.

Features List

- Slave mode.
- Supports 4,800 to115,200 Baud rate, auto learning mechanism
- Supports 8 bit address.
- Supports 8 bit data access.
- Supports general broadcast transmission.
- 8N1:
  - 8 bits data
  - No parity
  - 1 stop bit
- Frame transaction – header, payload and suffix.
- Time out mechanism (time out for frame and per byte).
- No successive read/write – one transaction per register (read/write).
- Half duplex implementation – Rx starts after Tx ends
- A filter for glitches cancelling on the RX pin.

The Physical Layer

The UART protocol has two data lines; the Rx, from where the PD69104B receives its data, and the Tx, throughout where data is transmitted. The UART is a byte protocol in which every byte starts with a 'start bit' and ends with a 'stop bit'.

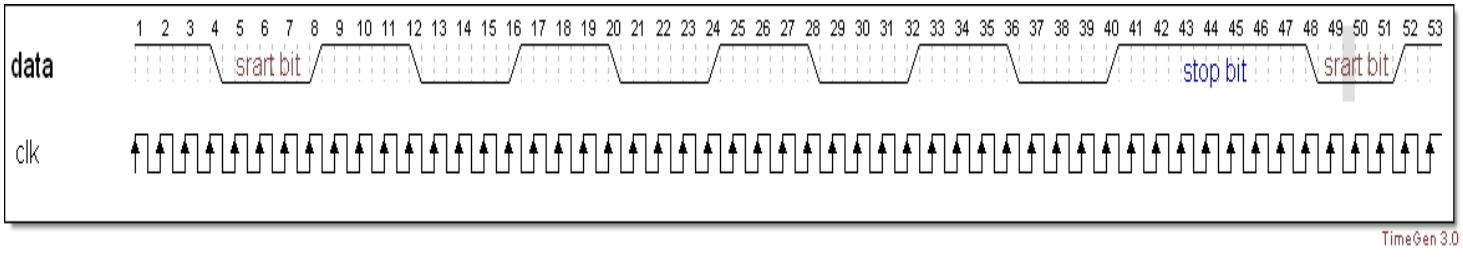


Figure 6: UART Read/Write Frame