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PD70211

PD Controller with Switching Regulator for AF/AT/UPOE/HDBaseT/4-pair PoE Applications

Description

PD70211 is an advanced PD Interface IC with integrated switching (PWM) regulator control for Powered Devices in PoE applications. It supports IEEE802.3af, IEEE802at, HDBaseT and general 2/4-pair configurations.

The PD70211 front-end includes an advanced classification block that supports 2, 3, 4, and 6 event classification. Using the SUPP_Sx pins, it also identifies which of the four pairs of the cable actually receives power and generates appropriate flags.

The IC features an internal bleeder for discharging the input capacitor of the DC/DC converter rapidly, so as to ensure fast re-detection and port power-up in case of sudden removal and re-insertion of the Ethernet cable into the RJ-45. The advanced PWM current-mode section supports synchronous Flyback and Active clamp Forward topologies, as well as Buck, Boost etc.

Features

- Supports IEEE802.3af/at, HDBaseT and other 2-pair/4-pair configurations
- Wall-adapter support (Rear Aux method)
- PD detection & programmable classification
- 2,3,4, and 6 event classification
- Integrated 0.3Ω isolating (series-pass) FET
- Inrush current limiting
- Less than 10µA offset current during detection
- Advanced PWM section
- Lead-free MLPQ-36 (6 × 6 mm) package

Applications

- HDBaseT up to 95 Watts
- IEEE802.3af and 802.3at
- Power Forwarding
- Indoor and outdoor PoE

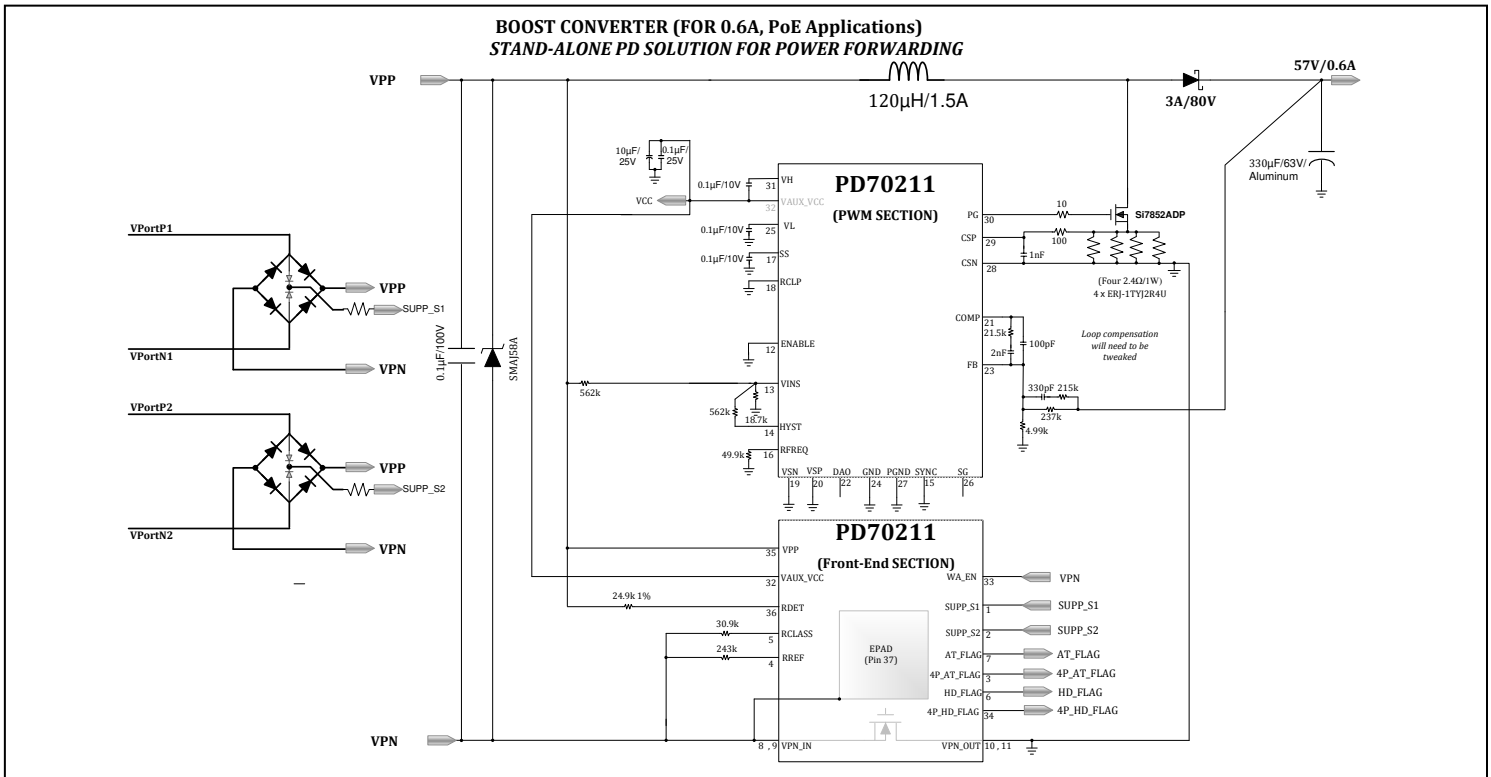

Figure 1: Typical Applications Diagram (PD70211)

Microsemi
CPG – PoE BU
One Enterprise Aliso Viejo, CA 92656 USA

Pin Configuration

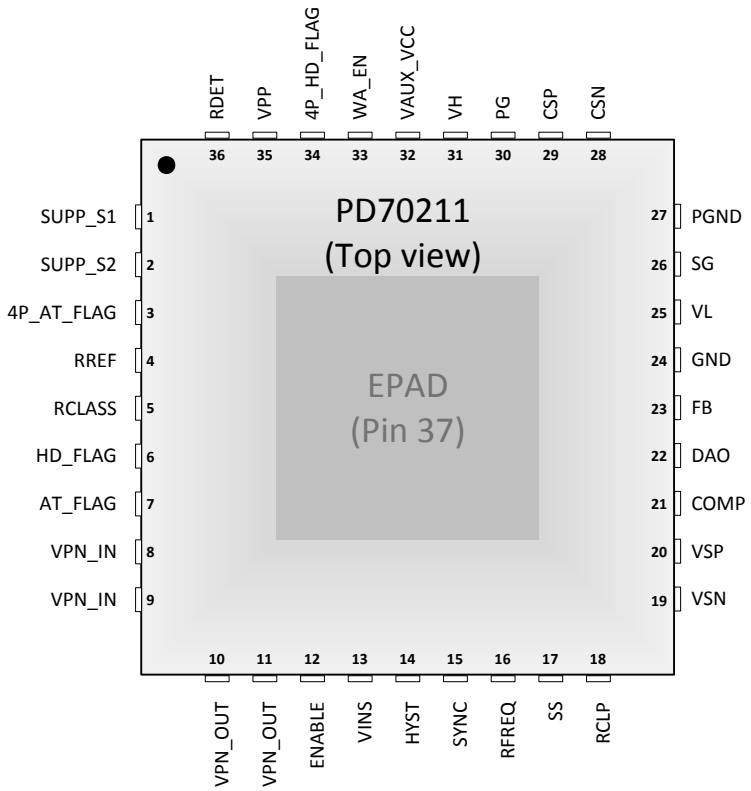

Figure 2: Pinout of PD70211 (top view)

Ordering Information

Ambient Temperature	Type	Part Marking	Tape and Reel	Package
-40°C to 85°C	RoHS compliant, Pb-free	MSCC Logo PD70211 Date/Lot Code	PD70211ILQ-TR	MLPQ-36 (6 mm × 6 mm, 0.5mm pitch)

Pin Description (PD70211)

Pin Number	Designator	Description
1	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S2 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only). Signal is referenced to VPN_IN. Place a 10k resistor in the input of this pin.
2	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S1 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only) . Signal is referenced to VPN_IN. Place a 10k resistor in the input of this pin.
3	4P_AT_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identifies each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
4	RREF	Bias current resistor. A 60.4k, 1% resistor is connected between RREF and IC ground (VPN_IN)
5	RCLASS	Sets the Class of the PD. Connect RCLASS (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4 respectively. If RCLASS is not present, the PD will draw up to 3 mA during classification, thus indicating Class 0 (default Type 1) to the PSE. Signal is referenced to VPN_IN
6	HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
7	AT_FLAG	Open Drain Output. This pin gets actively pulled low when a Type 2 PD-PSE mutually identifies each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
8, 9	VPN_IN	Lower rail of the incoming PSE voltage rail – from the negative terminal of the two OR-ed bridge rectifiers (the corresponding upper PoE rail is VPP)
10, 11	VPN_OUT	This is in effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and Power-up. It is connected to the Power ground and PWM controller IC's ground plane of the DC-DC converter section

Pin Number	Designator	Description
12	ENABLE	A logic-level input to enable the converter. We can pull it constantly up, say with a 100k resistor to VDD, to forcibly enable the converter. Provided the input supply has exceeded any applicable UVLO thresholds, of course, as set on the VINS pin or on the VCC pin. Internally, the ENABLE pin actually goes to the input of an OR-gate, the other input terminal of which is tied to "POK" – a signal provided by the front-end. If the ENABLE pin is forced high, the output of the OR-gate goes high and the converter is allowed to start (provided all UVLO's are past of course). If the ENABLE pin is held low, the internal node "POK" goes active high when the PD's front end conducts (power OK), so the OR-gate goes high once again. In this case the switching converter turns ON naturally and correctly as required by the PoE standard. However, for supporting wall-adapters, injecting power after the front-end (at the input of the converter), we can forcefully turn the converter ON without the front-end signaling "PGOOD", by *not* tying the ENABLE pin low, but by tying it high (to VDD). That will turn ON the converter irrespective of the state of the front-end (conducting or not), and whether there is any incoming PoE power or not.
13	VINS	The VINS pin is a programmable UVLO pin. The converter will turn ON provided the voltage on the VINS pin is above 1.2V (and VCC is not in UVLO, and ENABLE pin is also high – connected to VDD for example). The converter will stop switching (turn OFF) when the voltage on the VINS pin falls below 1.2V (or if ENABLE is taken low, or if VCC falls outside its operating range). Thus by connecting a voltage divider between input rail and IC ground, we can set the UVLO threshold to enable switching. However, to have a smooth startup, it is advisable to have some hysteresis too, by means of a resistor between VINS and HYST as explained below.
14	HYST	This is the output of the UVLO comparator as shown in the Block Diagram. We connect a "hysteresis resistor" from HYST pin to VINS pin to create positive feedback (and hysteresis). Initially, as the input voltage is rising, the VINS pin voltage is below 1.2V and so the output of the UVLO comparator is low, and the hysteresis resistor falls in parallel to the lower resistor of the UVLO divider placed at the VINS pin, assisting it by pulling down the VINS pin voltage further. As soon as the rising UVLO threshold is exceeded (VINS > 1.2V), the output of the UVLO comparator suddenly goes high (up to VDD) and the hysteresis resistor, effectively comes partially across the upper resistor of the UVLO divider, assisting it in the act of pulling up on the VINS pin. This feedback therefore increases the voltage on the VINS pin. And so, now the input rail has to fall to a much lower level to allow the VINS pin voltage to fall below 1.2V. That is how hysteresis is created by *positive feedback* action through the hysteresis resistor. The exact math is in the applications information of this datasheet. Note that HYST pin always toggles high or low depending on whether the voltage on the VINS pin is above or below 1.2V respectively. This can always be used to simultaneously drive an opto, to indicate when the input rail is above the programmed rising threshold and when it falls below the programmed falling threshold.
15	SYNC	Used to synchronize the LX7309 to a frequency higher than its default value as set on RFREQ pin. The synchronizing clock must be 2x the desired sync frequency, with a maximum synchronizing clock frequency of 1MHz (for 500kHz PWM frequency). The PG pin's rising edge will occur at the same instant as the rising edge of the clock being applied on the SYNC pin.

Pin Number	Designator	Description
16	RFREQ	Connect a programming resistor from this pin to IC ground (pin GND) to set the switching frequency. A typical value of the programming resistor is 49.9k, and this value will provide a frequency between 215kHz. Halving it will roughly double the frequency, whereas doubling it will halve the frequency. Note that the converter is designed to operate from 100 to 500 kHz based on this pin. Switching Frequency Equation: $$Freq = \frac{1}{(90pF \times R_{FREQ}) + 150ns}$$ where Freq is [Hz] and R_{FREQ} in [Ω] For further information refer to Setting Switching Frequency.
17	SS	This is the soft-start pin. Typically a 0.1µF cap, the "soft-start capacitor", is connected between this pin and IC ground (pin GND). The capacitor gets charged up to 1.2V by an internal resistor, and the voltage on the cap in effect forms the input voltage reference VREF of the error amplifier. But note that this capacitor serves other functions too; for example, it controls the rate of hiccupping under overcurrent fault conditions. So even if the internal reference is not being used (as in isolated topologies with a TL431 on the Secondary side), the soft-stat cap is always recommended to be in place. The actual capacitor used will be determined by the application. For further information refer to Setting Soft-Start.
18	RCLP	Low power clamp resistor. We can connect a resistor from this pin to IC ground (pin GND) to set the exact level at which pulse-skipping mode is entered at light loads. However, the usual default is to connect this pin directly to IC ground, in which case pulse-skipping mode is disabled. The method to select the threshold (and RCLP resistor value) is described in the Applications Information section of this datasheet.
19	VSN	The negative input of the internal differential-sense voltage amplifier. Note that the common-mode range of the differential voltage amplifier is 3.5V and its gain is 7. We can use this differential amplifier for implementing topologies where the "system (output) ground" is different from the IC ground. We can then step-down both output rails (output rail and its return), by equal amounts, using identical voltage dividers, to bring the voltage below 3.5V, then use differential sensing, and finally connect the output of the differential voltage amplifier (pin DAO) to FB pin.
20	VSP	The positive input of the internal differential-sense voltage amplifier. Note that it must always be connected in such a way that VSP is at a higher voltage than VSN. Also keep in mind that since the differential voltage amplifier has a gain of 7 and the output of that amp is connected to the feedback pin which compares that against a 1.2V reference, in effect, the difference between VSP and VSN stabilizes to 1.2V/7 = 0.171V in steady state. That is how we design the (identical) voltage dividers present on VSP and VSN.

Pin Number	Designator	Description
21	COMP	This is the output of the internal error amplifier, and the input of the PWM comparator. It is brought out to support isolated topologies because in such cases, there is an error amplifier already present on the Secondary side (for example a TL431 or equivalent). Therefore we want to bypass the error amplifier of the converter section. On the other hand, in non-isolated topologies, we want to use the error amplifier of the converter. We can do that directly, or through the differential voltage amplifier stage.
22	DAO	This is the output of the internal differential voltage amplifier (gain = 7). When this amplifier is used, we connect DAO to the feedback pin (FB). We have part of the compensation network between the two pins, and this network is typical of any Type 3 error amplifier input, with or without a differential amplifier present.
23	FB	This is the feedback pin of the IC. It is internally compared to a 1.2V reference. If the internal error amplifier is not used and the COMP pin is being used to inject the error signal (as in isolated topologies), the FB pin can be either tied high (to VDD), or connected to COMP.
24	GND	This is the IC ground. In more detail this is the analog (quiet) ground of the IC. Pin 20 is the Power ground (PGND). Typically, we can connect the analog ground and PGND together on a copper island on the component side, and then connect that through several vias very close to the chip on to a large ground plane which extends up to the lower side of the current sense resistor. All chip decoupling can then be very simply with respect to the copper island on the component side.
25	VL	This is created by an internal LDO and basically provides a housekeeping rail for the IC itself, which is 5V with respect to the IC ground. A 1µF ceramic cap placed close to this pin, connected to IC ground is recommended for proper decoupling. This pin can also provide up to 5mA for external circuitry if required, thermal aspects (IC dissipation) being considered.
26	SG	Secondary Gate driver. We can use this to drive a synchronous FET or an active clamp FET. It is derived from VCC (~ 12V), and has a 10Ω limiting resistor. So it can be used to drive a Gate-drive transformer directly. It is usually complementary to the Primary Gate driver pin (PG). But there is a typical 110ns blanking time between the two to prevent cross-conduction. SG is held firmly low in pulse-skip mode (if allowed). It is also low during soft-start. It allows forced PWM (continuous conduction) mode by allowing negative inductor currents. It does not support diode-emulation mode (discontinuous conduction mode). However, in pulse-skip mode, since SG stays OFF, the converter automatically lapses into discontinuous conduction mode through the body-diode of the synchronous FET. We can leave this pin floating if unused.
27	PGND	Power ground (for internal SG and PG drivers). This is also best for VCC decoupling, and the Primary-side current sense resistor's lower terminal. We can also combine GND an PGND on to a single large ground plane. Note that Power ground plane is firmly connected to VPN_OUT, which is the Drain side of the PD's low-side pass-FET (it stands for Negative Port Voltage Out).

Pin Number	Designator	Description
28	CSN	The negative input of the internal current-sense voltage amplifier. Note that the common-mode range of the differential current-sense amplifier is 2V and its gain is 5. We can use this for high-side current sensing up to 2V. It is then placed on the (steady) output side of a Buck inductor, and the max output voltage is 1.8V for using this type of sensing. Ensure that CSN is at a lower voltage compared to the positive input of the current-sense amplifier (CSP). Current sensing can also be implemented in a more basic fashion for "low-side" sensing, with a resistor in the return (ground) of the Buck. In that case CSN is shown connected to IC ground. However, to avoid noise from ground bounce, it is best to route this on the PCB in Kelvin manner to the lower end of the sense resistor. This is important because the peak operating voltage on the sense resistor is only 200mV and PCB-related noise can cause jitter in the switching waveform in current-mode control.
29	CSP	The positive input of the internal current-sense voltage amplifier. See discussion for Pin 28 (CSN) above. Note that the output of the current-sense amplifier is amplified 5 times. So a 0.2V current-sense voltage translates to a 1V swing at the input of the PWM comparator. Higher voltages lead to hiccup mode protection.
30	PG	This stands for Primary Gate driver. We can use this to drive the main FET, and it has a 5 or 10Ω limiting drive resistor switched between a voltage close to VCC rail and the IC ground. For guaranteeing proper shutdown during OFF time, it is necessary to add a 470k resistor from PG to VINS, as shown in Figure 1.
31	VH	Internal rail of -5V with respect to VCC, brought out only for decoupling purposes. Connect a 0.1µF ceramic cap very close, from this pin to VAUX_VCC pin.
32	VAUX_VCC	Auxiliary voltage rail from front-end to the VCC (supply) input of the PWM section. The front-end provides a few mA of startup current for the PWM controller (at typically 10.5V). Signal is referenced to VPN_OUT and is activated once front end power up sequence is end. After initial startup of PWM section, a bias winding can be connected to this pin through a diode, to sustain the PWM section.
33	WA_EN	While this input is low (referenced to VPN_IN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature. Place 100nF/10V capacitor from WA_EN to VPN_IN pins, locate it close to device. When WA_EN is not used, connect it to VPN_IN. For further information, refer to External source connected to PD device output.
34	4P_HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
35	VPP	Upper rail of the incoming PSE voltage rail – from the positive terminal of the two OR-ed bridge rectifiers (the corresponding lower PoE rail is VPN_IN)
36	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25KΩ (or 24.9K), 1% resistor is connected between this pin and VPP
37	EPAD	Connected on PCB plane to VPN_IN

Functional Block Diagram

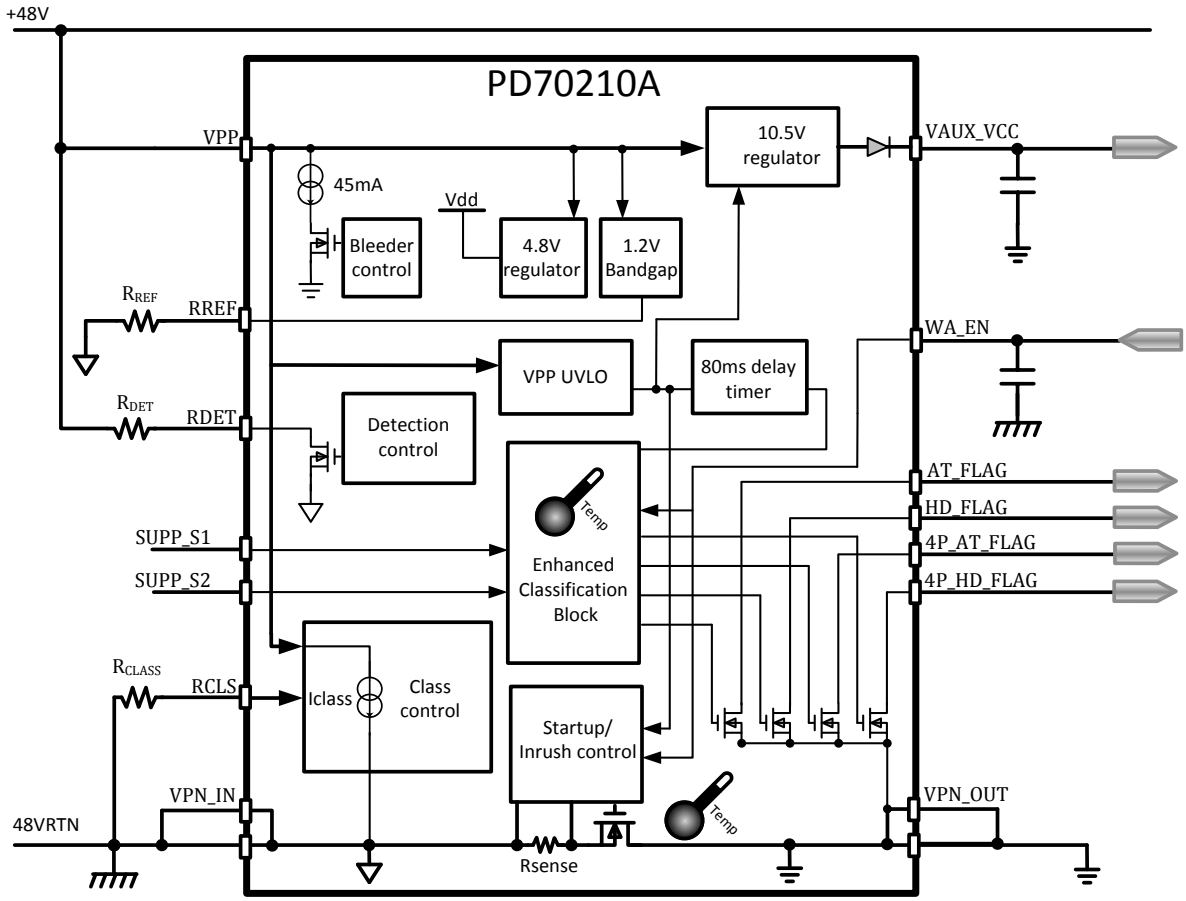

Figure 3: Block Diagram (PD70211 front-end section)

PD70211 (PWM section)

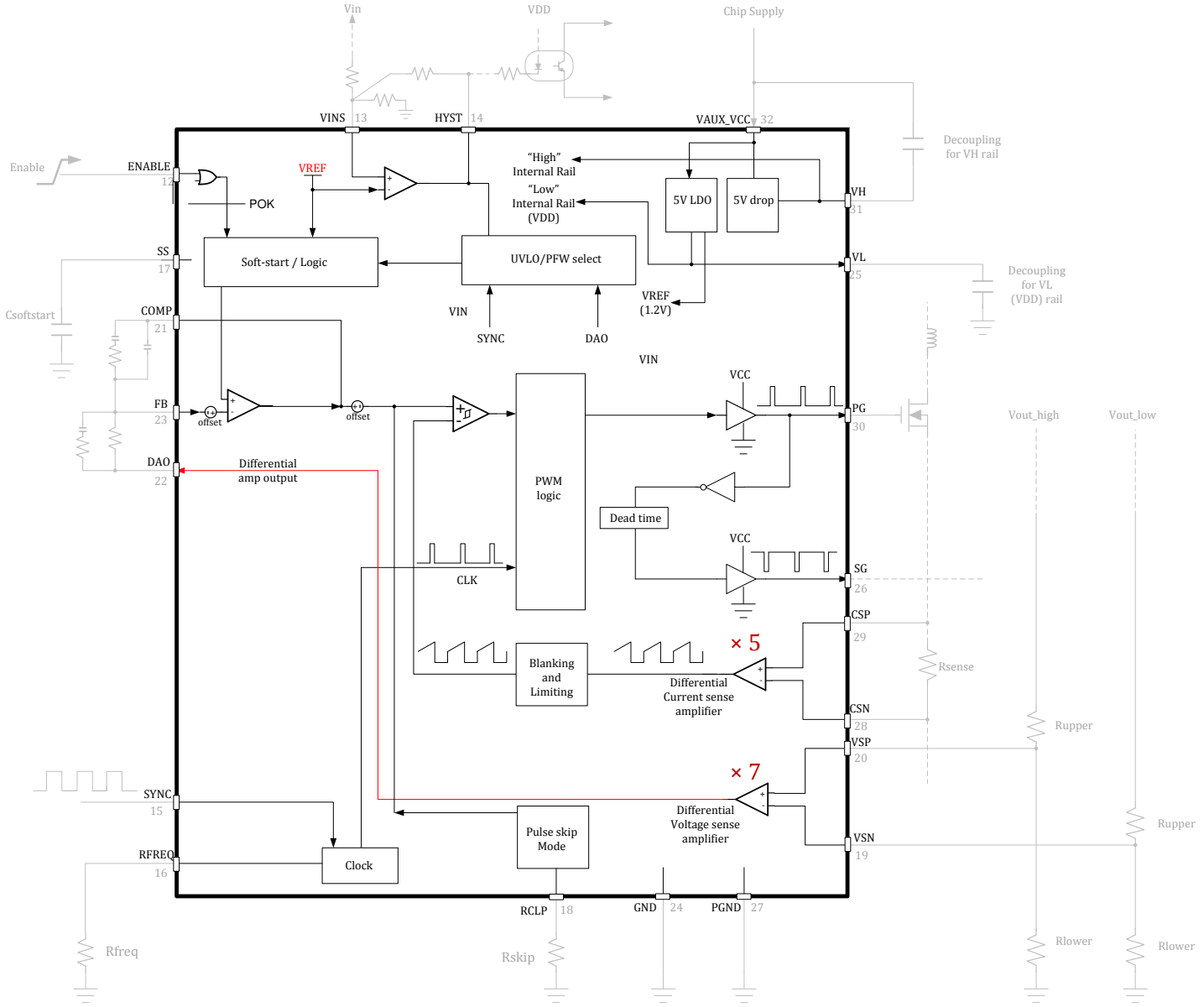

Figure 4: Block Diagram (PD70211 PWM section)

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability. Voltages are with respect to IC ground (VPN_IN).

		Min	Max	Units
VPP, VPN_OUT, RDET		-0.3	74	V
AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG		-0.3	20	V
SUPP_S1, SUPP_S2		0	V_{VPP} + 1.5	V
RREF, RCLS, WA_EN		-0.3	5	V
VAUX_VCC		-0.3	20	V
PG, SG		-0.3	20	V
VL		-0.3	6	V
VH (with respect to VAUX_VCC)		0.3	-6	V
ENABLE				
All other pins		-0.3	VL+0.3	V
Junction Temperature		-40	150	°C
Lead Soldering Temperature (40s, reflow)			260	°C
Storage Temperature		-65	150	°C
ESD rating	HBM		±1.5*	kV
	MM		±50	V
	CDM		±500	V

*Pins VPP, VAUX/VCC , RREF pass ±1kV HBM only.

Operating Ratings (Front-End Section)

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics. voltages are with respect to IC ground (VPN_IN).

	Min	Max	Units
VPP	0	57	V
Ambient Temperature*	-40	85	°C
Detection Range	1.1	10.1	V
Mark event range	4.9	10.1	V
Class event range	13.7	20.9	V

* Corresponding Max Operating Junction Temperature is 125°C.

Operating Ratings (PWM Section)

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics. Voltages are with respect to IC ground.

	Min	Max	Units
VCC	7.8	20	V
Fsw (adjustable frequency range)	100	500	kHz
Max Duty Cycle		44.5	%
f_{sw_synch} (synchronization frequency range)	200	1000	kHz

Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		22.3		°C/W
θ_{JP}		3		°C/W
θ_{JC}		4		°C/W

Note: The θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics (Front-End Section)

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated, are either by design or by production testing at 25°C ambient. Voltages are with respect to IC ground (VPN_IN).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage						
I_{IN}	IC input current with I_{CLASS} off	VPP=55V		1	3	mA
Detection phase						
V_{DET}	Detection range		1.1		10.1	V
R_{DET_TH}	R_{DET} disconnect threshold		10.1		12.8	V
$R_{DS\_DET\_ON}$	On-resistance of internal FET during detection				50	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$R_{DS\_DET\_OFF}$	Off-resistance of internal FET after detection		**2**			MΩ
I_{OFFSET_DET}	Input offset current	1.1V ≤ VPP ≤ 10.1V, T_J ≤ 85°C			5	µA
$V_{R\_DET\_ON}$	R_{DET} reconnection threshold when VPP goes low		2.8	3.0	4.85	V
Classification phase						
V_{CLS_ON}	Classification sink turn-on threshold		11.4		13.7	V
V_{CLS_OFF}	Classification sink turn-off threshold		20.9		23.9	V
$V_{HYS\_CLS\_ON}$	Hysteresis of V_{CLS_ON} threshold			1		V
V_{MARK_TH}	Mark detection threshold (VPP falling)		10.1		11.4	V
I_{MARK}	Current sink in Mark event region		0.25		4	mA
I_{CLASS_CLIM}	Current limit of class current		50	68	80	mA
I_{CLASS}	Classification current sink	R_{CLASS} = not present (Class 0)			3	mA
		R_{CLASS} = 133 Ω (Class 1)	9.5	10.5	11.5	
		R_{CLASS} = 69.8 Ω (Class 2)	17.5	18.5	19.5	
		R_{CLASS} = 45.3 Ω (Class 3)	26.5	28.0	29.5	
		R_{CLASS} = 30.9 Ω (Class 4)	38.0	40.0	42.0	
Isolation FET						
R_{DSON}	On resistance	Total resistance between VPN_IN to VPN_OUT; I_{LOAD} < 600mA, -40°C <T_A < 85°C			0.3	Ω
I_{CLIM_INRUSH}	Inrush current limit		105	240	325	mA
OCP	Overcurrent protection		2.2			A

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILOAD	Continuous operation load				2	A
Undervoltage Lockout						
$UVLO_{ON}$	Threshold that marks start of Inrush phase		36		42	V
$UVLO_{OFF}$	Threshold where pass-FET turns off as VPP collapses		30.5		34.5	V
DC-DC Input Cap Discharger						
I_{CAP_DIS}	Discharge current	7V ≤ VPP ≤ 30V	22.8		60	mA
t_{dis}	Discharge time	C_{DC_DC} ≤ 264 µF (by design, not tested)			500	ms
$timer_{dis}$	Discharge timer	Time for which discharge circuit is activated	430			ms
References, Rails and Logic						
V_{AUX}	Auxiliary voltage	0mA < I_{AUX} < 4mA	9.8	10.5	12.0	V
I_{AUX}	Max continuous current from V_{AUX}		4			mA
I_{AUX_CLIM}	Aux current limit		10		32	mA
V_{REF}	Bandgap reference voltage		1.17	1.2	1.23	V
t_{FLAG_LO}	Low level flag	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG, I_{FLAG}= 3mA			0.4	V
I_{FLAG}	Flag Current driving capability	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	5			mA
t_{FLAG}	Delay timer between start of inrush and flags declared	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	80			ms
V_{SUPP_HI}	SUPP_Sx high voltage threshold	For SUPP_S1 and SUPP_S2	25		35	V

Wall Adapter			Min	Typ	Max	Units
V_{IH}	Input high logic		2.4			V
V_{IL}	Input low logic				0.8	V

Truth Table for Status of Flags

Number of Fingers "N" (N-Event classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi Z	Hi Z	Hi Z	Hi Z
2	H	L	0V	Hi Z	Hi Z	Hi Z
2	L	H	0V	Hi Z	Hi Z	Hi Z
2	H	H	0V	Hi Z	0V	Hi Z
3	L	H	0V	0V	Hi Z	Hi Z
3	H	L	0V	0V	Hi Z	
3	H	H	0V	0V	0V	Hi Z
4	X	X	0V	0V	0V	Hi Z
5	RESERVED FOR FUTURE					
6	X	X	0V	0V	0V	0V

Electrical Characteristics (PWM Section)

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated, are either by design or by production testing at 25°C ambient. Voltages are with respect to IC ground (VPN_IN).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Current						
$V_{CC\_UVLO\_UP}$	UVLO threshold with input rising	V_{CC} rise time $\geq$ 0.5 ms	8.85	9.15	9.5	V
$V_{CC\_UVLO\_DN}$	UVLO threshold with input falling	V_{CC} rise time $\geq$ 0.5 ms	7	7.3	7.6	V
I_{VCC_SD}	IC input current (no switching)	V_{ENABLE} = Low, or V_{VCC} < $V_{CC\_UVLO\_UP}$		1	2000	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{VCC_Q}	IC input current (switching, no load on SG, PG, VDD)	V_{ENABLE} = High, and $V_{VCC} > V_{CC\_UVLO\_UP}$, fsw = 500kHz			3	mA
Input UVLO/PFW						
VINS_TH	Threshold on VINS pin	Rising or falling	1.171	1.200	1.229	V
V_{HYST_HIGH}	Hysteresis pin high voltage	$I_{HYST\_SOURCING}$ = 1mA	2.8			V
V_{HYST_LOW}	Hysteresis pin low voltage	$I_{HYST\_SINKING}$ = 3mA			0.4	V
LDOs						
VL		I_{VDD_EXT} < 5mA (current out of pin)	4.75	5	5.25	V
VH	VH rail (with respect to VCC)			-5V		V
Soft Start						
I_{SS_CH}	Current out of SS pin during charging phase	RFREQ=33.3k, V_{SS}=0.5V	32	36	40	µA
I_{SS_DISCH}	Current into SS pin during discharging phase	RFREQ=33.3k, V_{SS}=0.5V		10		% of I_{SS_CH}
V_{SS_CH}	Soft start charge completed threshold	By design only	90		95	% of VREF
V_{SS_DISCH}	Soft start discharge completed threshold			50		mV
R_{SS_DISCH}	Soft-start pin discharge FET resistance			50		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DISCH}	Soft-start discharge FET on-time			32		Switch cycles
Switching Frequency and Synchronization						
f_{sw_range}	Switching frequency accuracy	RFREQ=33.2k	285	315	345	kHz
f_{sync_max}	Max synchronization frequency		1			MHz
V_{SYNC_HI}	SYNC pin high threshold		2.4			V
V_{SYNC_LO}	SYNC pin low threshold				0.8	V
t_{sync}	Minimum pulse width of SYNC pulse		100			ns
D_{sync_max}	Max SYNC pulse duty cycle				90	%
Error Amplifier						
VREF	Reference voltage		1.171	1.200	1.229	V
$Gain_{DC\_OPL}$	DC Open-loop gain	Rload=100k	70	100		dB
AV_{UGBW}	Unity Gain Bandwidth	Cload=10pF (By design only)	2	5		MHz
I_{COMP_OUT}	Output sourcing current	$0.2V \leq V_{COMP} \leq 1.3V$	110		620	µA
I_{COMP_IN}	Output sinking current	$0.2V \leq V_{COMP} \leq 1.3V$	145		495	µA
$V_{EA\_CMR\_MAX}$	Max of input common-mode range		2			V
V_{CLAMP}	COMP pin high clamp		1.8	2.1	2.6	V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PWM Comparator						
V_{OFFSET}	Inserted offset in inverted input		200		300	mV
V_{RCLP}	Voltage set on RCLP pin by external resistor to GND		0		1	V
Current Sense Amplifier						
$Gain_{CSA}$	DC Gain		4.75	5	5.25	V
I_{AUX}	Max continuous current from V_{AUX}		4			mA
$V_{CSA\_CMR\_MAX}$	Max input common-mode range		2			V
t_{BLANK}	Blanking time		50		100	ns
V_{ILIM}	Current limit threshold on output of current sense amplifier	Where PWM pulses start to get truncated	1.1	1.2	1.3	V
$V_{ILIMHICCUP}$	Current Limit threshold on output of current sense amplifier capability	Where PWM pulses start to get omotted in hiccup mode	1.7	1.8	1.9	V
Differential Voltage Amplifier						
$Gain_{DA}$	DC gain of differential voltage amp		6.68	7.0	7.14	
AV_{UGBW_DA}	Unity Gain Bandwidth of differential voltage amp			5		MHz
$V_{DA\_CMR\_MAX}$	Max of input common-mode range		3.5			V
Drivers						
R_{PG_HI}	Drive resistance when PG is high			10		Ω
R_{PG_LO}	Drive resistance when PG is low			5		Ω
t_{PG_MIN}	Minimum on-time of PG				120	ns
D_{MAX}	PG max duty cycle		44.5		50	%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{SG_HI}	Drive resistance when SG is high			10		Ω
R_{SG_LO}	Drive resistance when SG is low			10		Ω
t_{DEAD}	Deadtime	PG low to SG high or PG high to SG low	60	110	190	ns
Logic Levels on VINS and ENABLE						
V_{HI}	Input high threshold		2			V
V_{LO}	Input low threshold				0.8	V
Thermal Protection						
T_{SD}	Thermal shutdown (rising)			157		°C
T_{HYST}	Thermal shutdown hysteresis			15	30	°C

Thermal Protection

PD70211 is protected from excessive internal temperatures that may occur during various operating procedures. Two temperature sensors are located on the chip, monitoring the temperatures of the following:

- Isolating Switch (pass-FET)
- Classification Current Sink

Each of the over temperature sensor activates a protection mechanism that will disconnect the Isolation (pass) FET or the classification circuit respectively. This protects the device from being permanently damaged or even from long-term degradation.

Truth Table for Status of Flags

Number of Fingers "N" (N-Event Classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi Z	Hi Z	Hi Z	Hi Z
2	H	L	0V	Hi Z	Hi Z	Hi Z
2	L	H	0V	Hi Z	Hi Z	Hi Z
2	H	H	0V	Hi Z	0V	Hi Z
3	L	H	0V	0V	Hi Z	Hi Z
3	H	L	0V	0V	Hi Z	
3	H	H	0V	0V	0V	Hi Z
4	X	X	0V	0V	0V	Hi Z
5	RESERVED FOR FUTURE					
6	X	X	0V	0V	0V	0V

Wall Adapter mode

PD70211 support wall adapter functionality, i.e. by setting WA_EN pin high it will give priority to the wall adapter jack to supply the load.

WA_EN pin is used while connecting a wall-adapter voltage between VPP and VPN_OUT by means of an OR-ing diode.

While WA_EN, Wall-adapter enable pin, is held low (referenced to VPN_IN), the front-end works as a normal PD.

When WA_EN is raised high (referenced to VPN_IN) three internal operations are forced:

- The Isolation FET is turned OFF.
- All output flags AT_FLAG, HD_FLAG, 4P_AT_FLAG and 4P_HD_FLAG are activated (low state).
- Vaux output voltage is turned ON.

While activating WA_EN pin, the wall-adapter will supply input voltage for the DC-DC converter.

Having WA_EN at high state does not disable detection and classification modes.

Applications Information

Peripheral devices

- An 100nF/100V capacitor should be placed between device VPP and VPNI pins, and located as close as possible to the device.
- An 58V TVS should be placed between device VPP and VPNI pins.
- An 10K ohm resistor should be placed on SUPP_S1 and SUPP_S2 lines between diode bridge and PD70211 device.
- When WA_EN is used, an 100nF/10V Capacitor should be placed between WA_EN and VPNI pin close to PD70211 device.
- When not used, WA_EN should be connected to VPNI pin.

Setting Switching Frequency

A resistor, RFREQ, is connected from RFREQ pin to IC ground. Based on that, we get the following frequency

$$Freq = \frac{1}{(90pF \times R_{FREQ}) + 150ns}$$

where Freq is [Hz] and Rfreq in Ω

For example, by setting RFREQ=49900Ω, we get

$$Freq = \frac{1}{(90pF \times 49900\Omega) + 150ns} = \sim 215000Hz$$

We can set any frequency between 100 to 500 kHz. Note that when synchronizing, the default frequency (as set by RFREQ) must be lower than the synchronization clock. In case the synchronization breaks, the converter will lapse back to the default value. When synchronizing, we can increase the frequency to 1MHz.

Setting Soft-Start

A capacitor is connected between SS pin and IC ground. The current charging the capacitor is

$$I_{SS\_CHG} = \frac{1.2V}{RFREQ} \text{ (in seconds)}$$

For example, if RFREQ=49.9k, we get

$$I_{SS\_CHG} = \frac{1.2V}{49.9\times10^{3}} \text{ (in Amperes)} = 2.4\times10^{-5} \Rightarrow 24\mu A$$

So, charging a 0.1µF ceramic cap on the soft-start pin from 0 to 1.2V will take

$$t_{SS} = \frac{C\times\Delta V}{I_{SS\_CHG}} \text{ (in seconds)} = \frac{0.1\mu\times1.2}{24\mu} \text{ (in seconds)} = \frac{0.12}{24} \text{ (in seconds)} = 5\times10^{-3} \text{(in seconds)} \Rightarrow 5ms$$

This is the soft-start time in this case.

Setting Pulse-skip Mode threshold

If a programming resistor RCLP is placed between RCLP pin and IC ground, the clamping voltage level is given by

$$V_{CLP} = \frac{0.3\times RCLP}{RFREQ} \text{ (in Volts)}$$

For example, if RCLP = RFREQ, say both are 49.9k, then the converter will enter pulse skipping when the output of the current sense amplifier drops to 0.3V. Note that the gain with this current amplifier is 5, so in terms of the voltage on the sense resistor (input of the current amp), we get 0.3V/5 = 0.06V. Since we usually design the converter so that its peak is around 0.2V (the peak of Rsense voltage before it starts to current limit), we are getting a ratio of 0.06V/0.2V = 0.3. In other words, the converter will enter pulse-skipping when the output current is 30% of the max designed output current.

Setting UVLO/Hysteresis thresholds

Note: *A 470k resistor from PG pin to VINS pin is required for guaranteeing proper termination of Gate drive pulse during UVLO.*

Suppose we have a divider connected to input at the VINS pin. Suppose we call the resistors R_{UPPER} and R_{LOWER}. We also have a hysteresis resistor, R_{HYST}, from the output of the UVLO comparator, which provides positive feedback on to the VINS pin, as explained in the Pin Description section. So, when the input voltage is rising, in

effect the hysteresis resistor is in parallel to the lower resistor R_{LOWER}. When the voltage on the VINS pin rises above 1.2V, the UVLO comparator flips and the hysteresis resistor appears connected to 5V (output of the UVLO comparator). The equivalent configurations are shown in Figure 5. After solving the equations, the following example indicates the set thresholds. The values are as used in Figure 3.

$R_{UPPER} = 270k; R_{LOWER} = 8.66k; R_{HYST} = 270k$

Part 1: (VINS less than 1.2V)

Equivalent lower resistor is a parallel combination of R_{LOWER} and R_{HYST}

$$R_{LOWER\_EQUIV} = \frac{R_{LOWER} \times R_{HYST}}{R_{LOWER} + R_{HYST}} = \frac{8.66k \times 270k}{8.66k + 270k} = 8.391k$$

The rising voltage threshold is

$$V_{UVLO\_UP} = VREF \times \frac{R_{UPPER} + R_{LOWER\_EQUIV}}{R_{LOWER\_EQUIV}} = 1.2V \times \frac{270k + 8.391k}{8.391k} = 39.8V$$

Part 2: (VINS greater than 1.2V)

$$V_{UVLO\_DN} = VREF \times \frac{R_{UPPER}}{R_{LOWER}} - (VDD - VREF) \times \frac{R_{UPPER}}{R_{HYST}} + VREF$$

$$1.2V \times \frac{270k}{8.66k} - (3.8V) \times \frac{270k}{270k} + 1.2 = 34.8V$$

So with the selected resistors, we get a rising threshold of 39.8V, and a falling threshold of 34.8V.

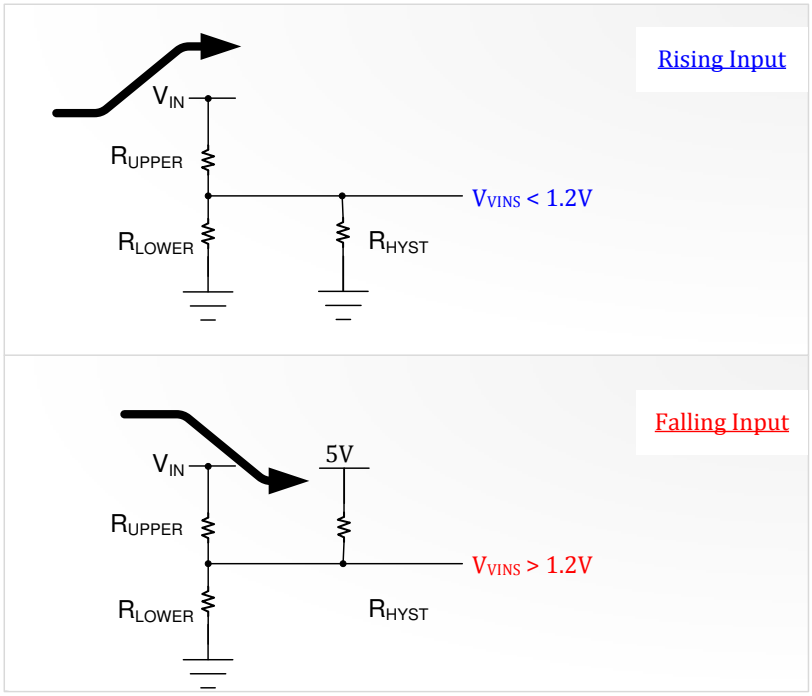

Figure 5: Equivalent Diagrams for UVLO and Hysteresis

Setting the Voltage Divider for Output Rails

Generically, we can state the equation to be

$$V_{OUT} = V_X \times \frac{R_{UP} + R_{LOW}}{R_{LOW}}$$

Where R_{UP} is the name we have given to the upper resistor (connected to output rail) and R_{LOW} is the name we have given here to the resistor connected to lower rail (usually IC ground). However, there are so many topologies, we have in effect thress cases in all the typical schematics presented so far.

a) Non-isolated topologies with simple divider connected directly to FB pin. For this use V_X = 1.2V.

b) Isolated topologies with divider to another reference (such as TL431 with an internal reference of 2.5V). For this use V_X = 2.5V.

c) Non-isolated topologies with a differential divider connected to differential voltage amplifier of the LX7309 . Here we use the same divider equation provided above, but using V_X = 0.171V (that is 1.2V divided down by the gain of the diff-amp, i.e. by 7). We need two identical dividers.

Selecting the Sense Resistor

In a Buck topology, the center of the switch current ramp equals the output current. To that we need to add about 30% for the peak current "I_{PEAK+}" because of the rising ramp caused by the inductor. That is a factor of 1.3. We also need to include some headroom for proper transient response at max load. Since the peak voltage on the sense resistor is 0.2V, to leave headroom, we should plan that the switch current peak stays at around 0.18V max at max load. This means that:

$$I_{PEAK} = 1.3 \times I_O, \text{ So}$$

$$R_{SENSE} = \frac{0.18}{1.3 \times I_O} = \frac{0.138}{I_O}$$

$$R_{SENSE} = \frac{0.138}{I_O} \text{ (Buck)}$$

Assuming we have designed the converter to operate up to 44% max duty cycle, we can quickly estimate the peak current as follows.

For example, if we have a Buck application for 5A output, irrespective of the input and output voltage conditions (as long as they are not violating the min and max duty cycle limits of the converter), and assuming we have selected inductance appropriately, we should pick a sense resistor of

$$R_{SENSE} = \frac{0.138}{5A} = 0.028\,\Omega$$

We may need to put an adjust resistor in parallel (such as the "22Ω" placeholder) we have shown in all the typical application schematics.

For a Forward converter (Buck with a transformer), instead of the load current I_{OR} in the above equation, use the reflected load current of I_O/n, where n is the turns ratio (number of Primary-side turns divided by number of Secondary-side turns). You will also need to lower the sense resistance further (by means of the adjust resistor), to account for the magnetization current component on the switch side. So roughly:

$$R_{SENSE} \approx \frac{0.138}{I_0} \times \frac{N_P}{N_S} \quad \text{(Forward)}$$

For a Boost or Buck-Boost, we have to account for the fact that the peak current is not just 1.3 times max load current, but is actually

$$I_{PEAK} = 1.3 \times \frac{I_0}{1-D} \text{ (where D can be as high as 44\%)}$$

So we should use the following equation for sense resistor

$$R_{SENSE} = \frac{0.18 \times (1-D)}{1.3 \times I_0} = \frac{0.101}{1.3 \times I_0} = \frac{1}{13 \times I_0}$$

$$R_{SENSE} = \frac{0.077}{I_0} \text{ (Boost, Buck-Boost)}$$

For example, if the max load current is 5A, the sense resistor value to use is

$$R_{SENSE} = \frac{0.077}{5A} = 0.015\,\Omega$$

As we can see, this is roughly half of what we got for the Buck (same load current).

For a Flyback topology (Buck-Boost with a transformer), we have to use the reflected output current. So we get:

$$R_{SENSE} \approx \frac{0.077}{I_0} \times \frac{N_P}{N_S} \text{ (Flyback)}$$

Operation with an External DC Source

PD applications utilizing PD70211 IC may be operated with an external power source (DC wall adaptor). There are two cases of providing power with an external source, the cases are presented in.

Figure 6 and **Figure 7.**

- External source connected to application's low voltage supply rails. External source voltage level is dependent on DCDC output characteristics. Described in
- Figure **6**
- External source connected to PD device output connection toward the application (VPP to VPN_{OUT}). External source voltage level is dependent on DCDC input requirements. Described in Figure 7

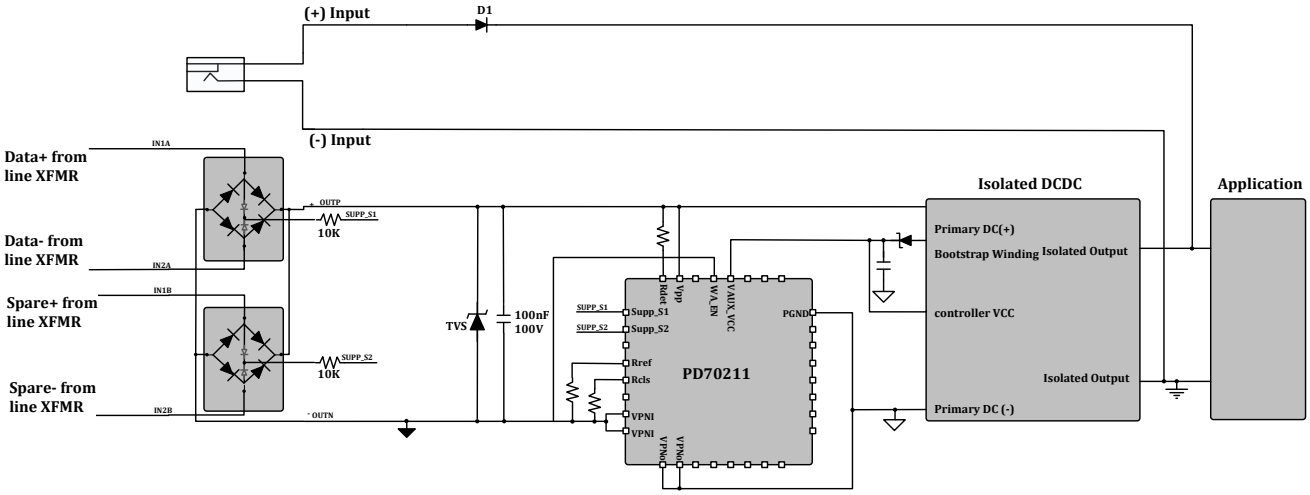

Figure 6: External Power Input connected to Application supply Rails