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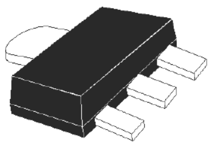
PD85004

RF power transistor the LdmoST plastic family

Features

- Excellent thermal stability
- Common source configuration
- Broadband performances
  P_{OUT} = 4 W with 17 dB gain @ 870 MHz
- Plastic package
- ESD protection
- Supplied in tape and reel
- In compliance with the 2002/95/EC european directive



SOT-89

Description

The PD85004 is a common source N-channel, enhancement-mode lateral field-effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 13.6 V in common source mode at frequencies of up to 1 GHz.

PD85004's superior gain and efficiency makes it an ideal solution for mobile radio.

Figure 1. Pin connection

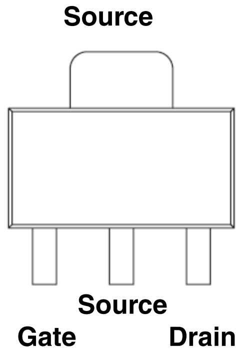


Table 1. Device summary

Order code	Marking	Package	Packaging
PD85004	8504	SOT-89	Tape and reel

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	-0.5 to +15	V
I_D	Drain current	2	A
P_{DISS}	Power dissipation	6	W
T_J	Max. operating junction temperature	150	°C
T_{STG}	Storage temperature	-65 to +150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	21	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 4. Static

Symbol	Test conditions			Min	Typ	Max	Unit
I_{DSS}	V_{GS} = 0 V	V_{DS} = 25 V				1	µA
I_{GSS}	V_{GS} = 5 V	V_{DS} = 0 V				1	µA
$V_{GS(Q)}$	V_{DS} = 13.6 V	I_D = 50 mA			3.9		V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 0.25 A			0.27		V
C_{ISS}	V_{GS} = 0 V	V_{DS} = 13.6 V	f = 1 MHz		16		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 13.6 V	f = 1 MHz		14		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 13.6 V	f = 1 MHz		1.1		pF

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 13.6 V, I_{DQ} = 50 mA, P_{IN} = 0.1 W, f = 870 MHz	4	5		W
G_{PS}	V_{DD} = 13.6 V, I_{DQ} = 50 mA, P_{OUT} = 4 W, f = 870 MHz	15	17		dB
N_D	V_{DD} = 13.6 V, I_{DQ} = 50 mA, P_{OUT} = 4 W, f = 870 MHz	60	65		%
Load mismatch	V_{DD} = 13.6 V, I_{DQ} = 50 mA, P_{OUT} = 4 W, f = 870 MHz All phase angles	20:1			VSWR

2.3 ESD protection characteristics

Table 6. ESD protection characteristics

Test conditions	Class
Human body model	2
Machine model	M3

2.4 Moisture sensitivity level

Table 7. Moisture sensitivity level

Test methodology	Rating
J-STD-020B	MSL 3

3 Impedances

Figure 2. Impedances

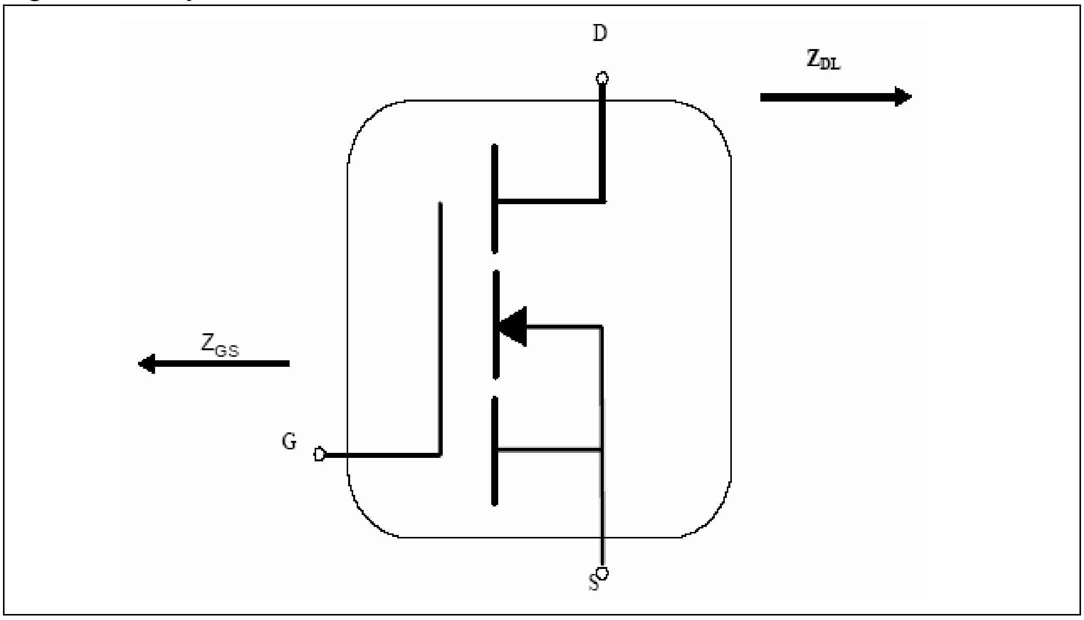


Table 8. Broadband impedances

F(MHz)	Z_{GS}	Z_{DL}
860	2.46+ j 6.63	8.38+ j 2,83
880	2.59+ j 6.83	8.08+ j 3.46
900	2.63+ j 6.97	7.77 + j 4.10
920	2.57+ j 7.09	7.50+ j 4.77
940	2.42+ j 7.17	7.15+ j 5.37
960	2.27+ j 7.34	6.95+ j 6.07

4 DC curves

Figure 3. DC output characteristics

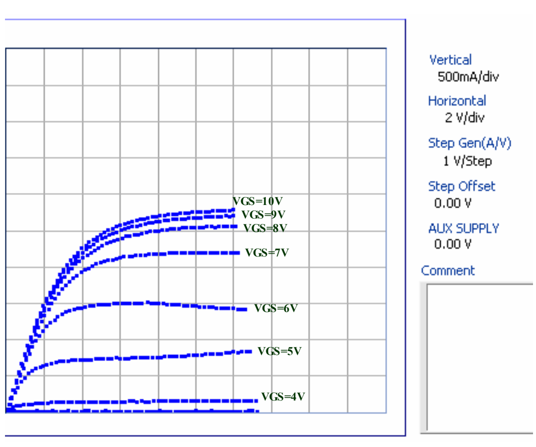


Figure 4. ID vs V_{GS}

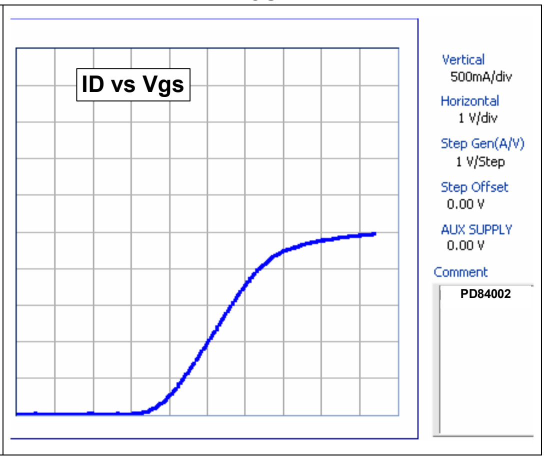
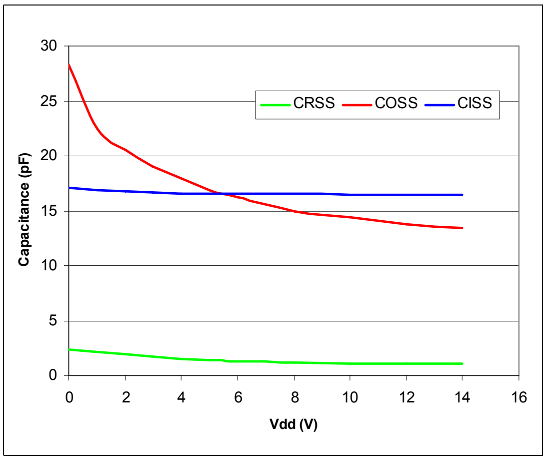


Figure 5. Capacitances vs drain voltage



5 RF curves

Figure 6. Output power and drain efficiency vs frequency 13.6 V / 50 mA / Pin = 19 dBm

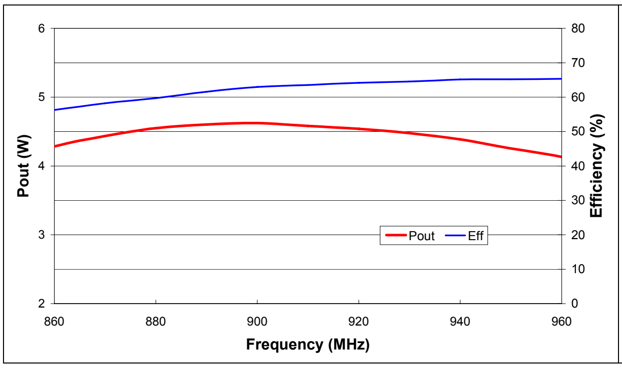


Figure 7. Gain vs frequency 13.6 V / 50 mA

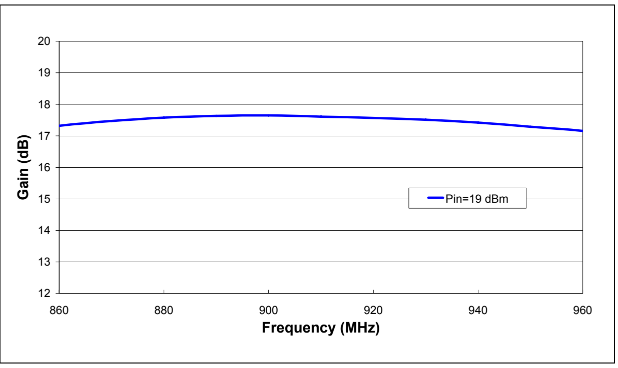


Figure 8. Input return loss vs frequency 13.6 V / 50 mA

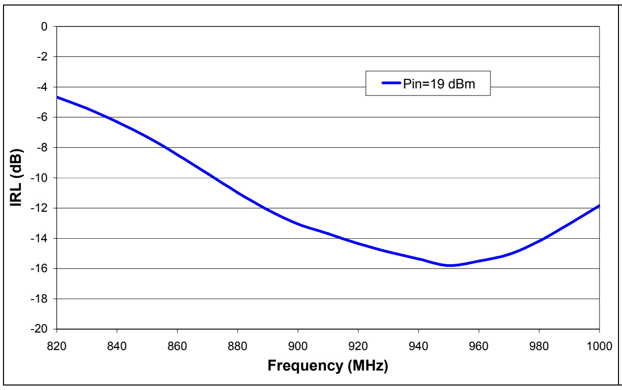


Figure 9. Gain vs output power 13.6 V / 50 mA

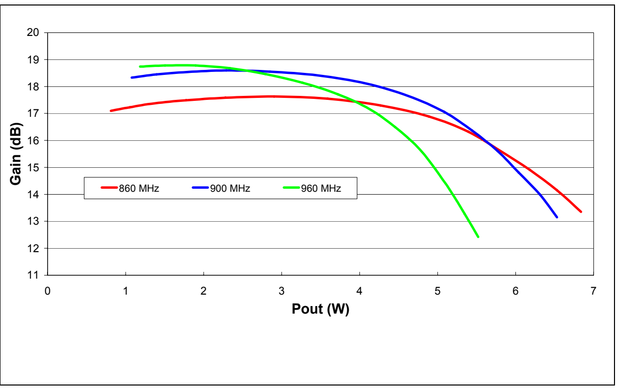


Figure 10. Drain current vs output power 13.6 V / 50 mA

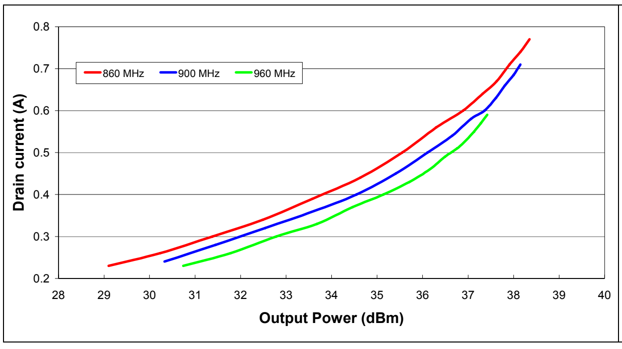


Figure 11. Output power vs input power 13.6 V / 50 mA

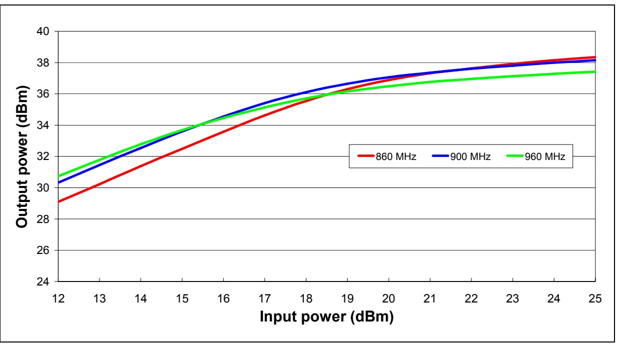
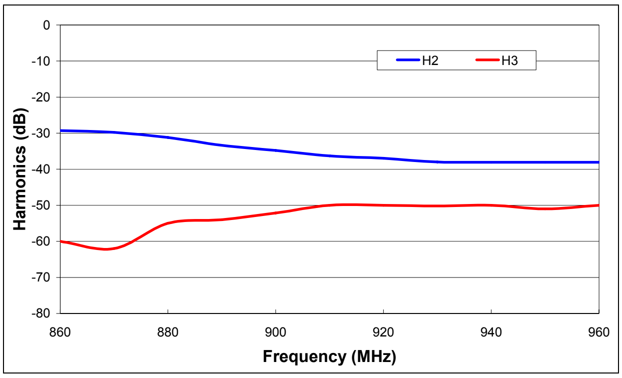


Figure 12. Harmonics vs frequency 13.6 V / 50 mA



6 Schematic and BOM

Figure 13. Schematic

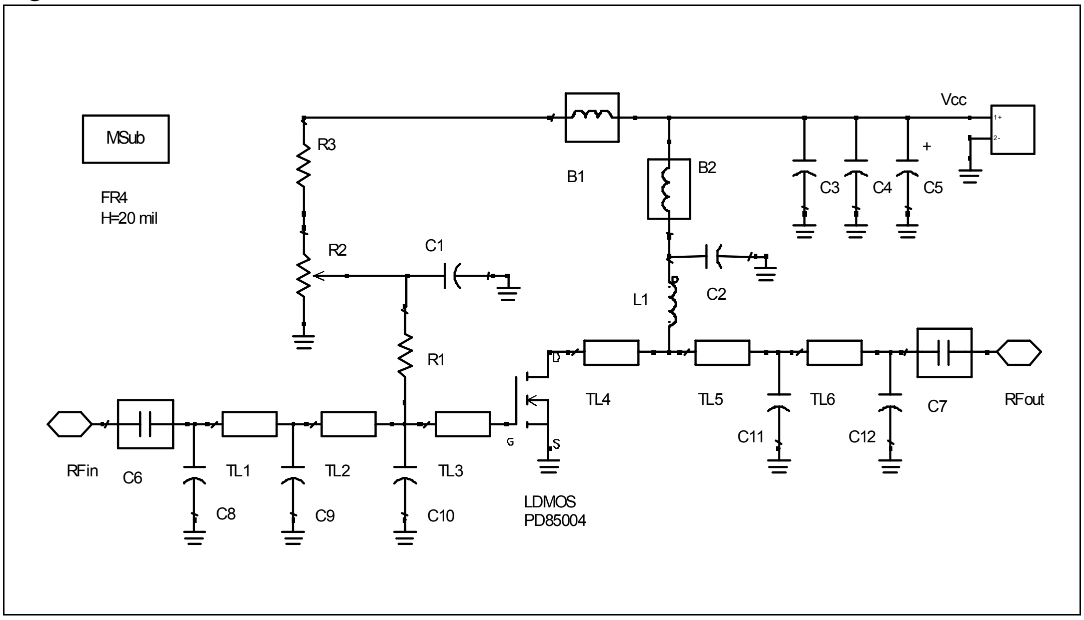
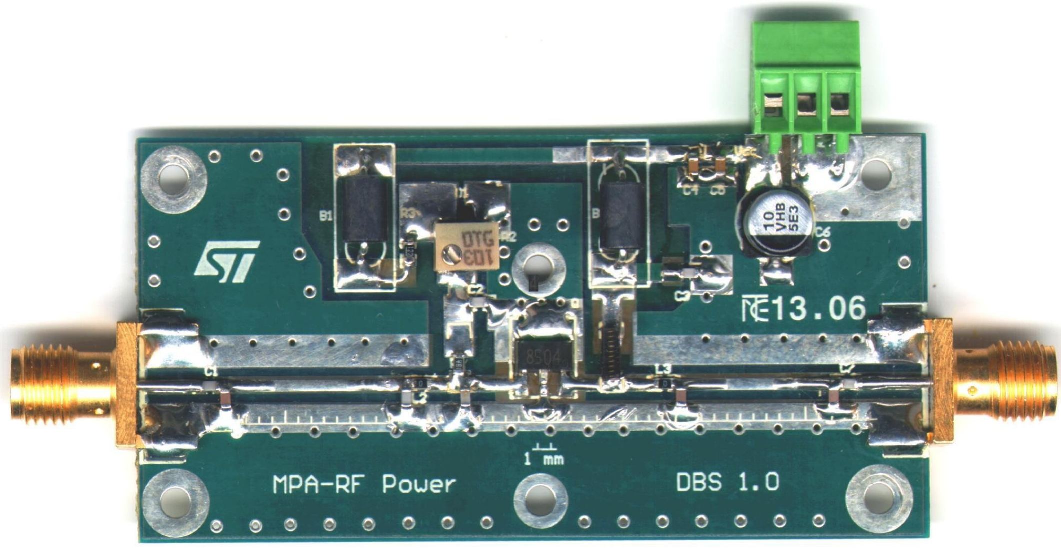


Table 9. **Components part list**

Component ID	Description	Value	Case size	Manufacturer	Part code
B1	Ferrite bead			Panasonic	EXCELDRC35C
B2	Ferrite bead			Panasonic	EXCELDRC35C
C1, C2	Capacitor	120 pF	0603	Murata	GRM39-C0G121J50D500
C3	Capacitor	1 nF	0603	Murata	GRM39-X7R102K50C560
C4	Capacitor	10 nF	0603	Murata	GRM39-X7R103K50C560
C5	Capacitor	10 uF	SMT	Panasonic	EEVHB1V100P
C6, C7	Capacitor	39 pF	0603	Murata	GRM39-C0G390J50D500
C8	Capacitor	3.3 pF	0603	Murata	GRM39-C0G3R3C50Z500
C9	Capacitor	12 pF	0603	Murata	GRM39-C0G120J50D500
C10	Capacitor	22 pF	0603	Murata	GRM39-C0G220J50D500
C11	Capacitor	6,8 pF	0603	Murata	GRM39-C0G6R8D50Z500
C12	Capacitor	1,5 pF	0603	Murata	GRM39-C0G1R5C50Z500
L1	Inductor	12.55 nH		Coilcraft	1606-10
R1	Resistor	150 Ω	0603	Tyco electronics	
R2	Potentiometer	10 KΩ		Bourns electronics	3214W-1-103E
R3	Resistor	1 K	0603	Tyco electronics	01623440-1
TL1	Transmission Line	W= 0.92 mm	L = 13.6 mm		
TL2		W=0.92 mm	L = 3.5 mm		
TL3		W=0.92 mm	L = 4.2 mm		
TL4		W=0.92 mm	L = 3.8 mm		
TL5		W=0.92 mm	L = 4.2 mm		
TL6		W=0.92 mm	L = 11.3 mm		
RF in, RF out	SMA-CONN	50 Ω	60 mils	JOHNSON	142-0701-801
PD85004	LDMOS			STMicroelectronics	PD85004
Board	FR-4 THk = 0.020" 2 OZ Cu both sides				

7 Demonstration board photo

Figure 14. Demonstration board photo



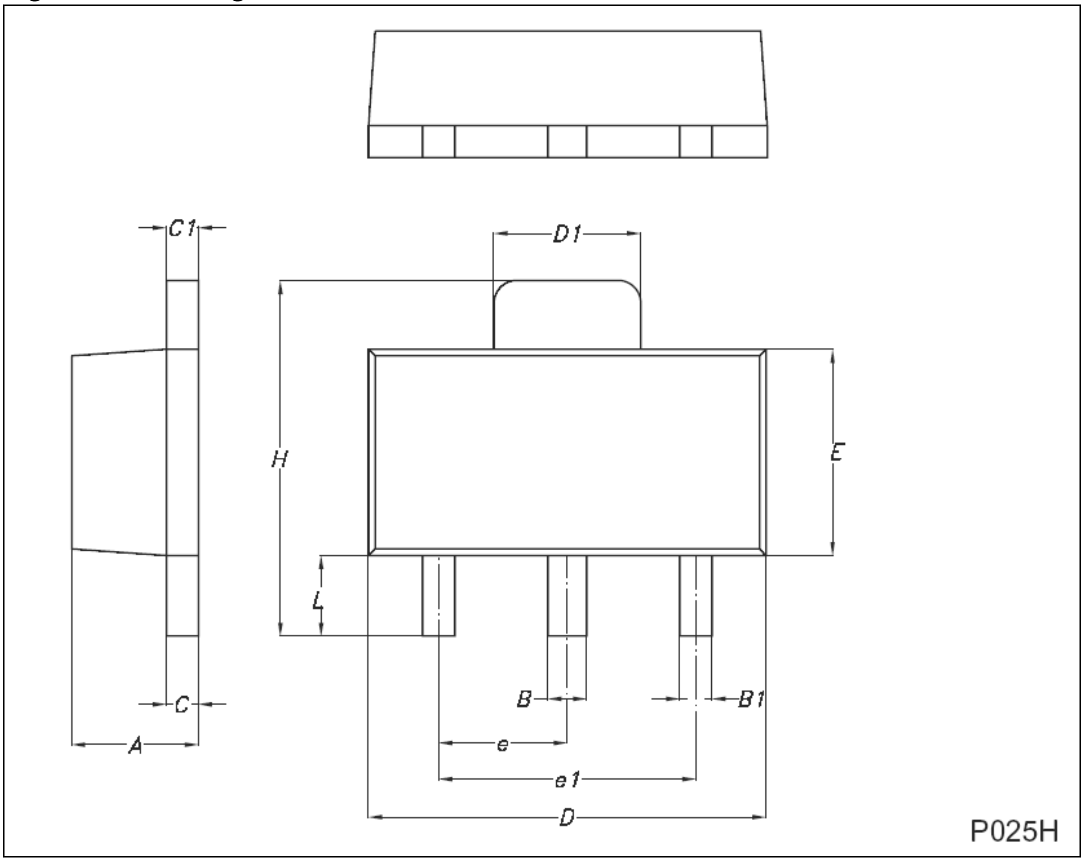
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 10. SOT-89 mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	1.4		1.6	55.1		63.0
B	0.44		0.56	17.3		22.0
B1	0.36		0.48	14.2		18.9
C	0.35		0.44	13.8		17.3
C1	0.35		0.44	13.8		17.3
D	4.4		4.6	173.2		181.1
D1	1.62		1.83	63.8		72.0
E	2.29		2.6	90.2		102.4
e	1.42		1.57	55.9		61.8
e1	2.92		3.07	115.0		120.9
H	3.94		4.25	155.1		167.3
L	0.89		1.2	35.0		47.2

Figure 15. Package dimensions

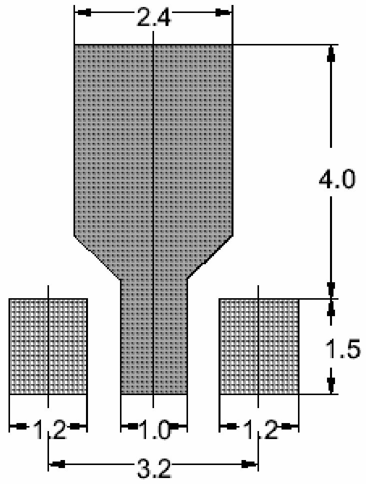


8.1 Thermal pad and via design

Thernal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device.

The via pattern is based on thru-hole vias with 0.203 mm to 0.330 mm finished hole size on a 0.5 mm to 1.2 mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Figure 16. Pad layout details



SOT89 pattern.
Minimum Pad Size (dimensions in mm)

8.2 Soldering profile

Figure 17 shows the recommeded solder for devices that have Pb-free terminal plating and where a Pb-free solder is used.

Figure 17. Recommended solder profile

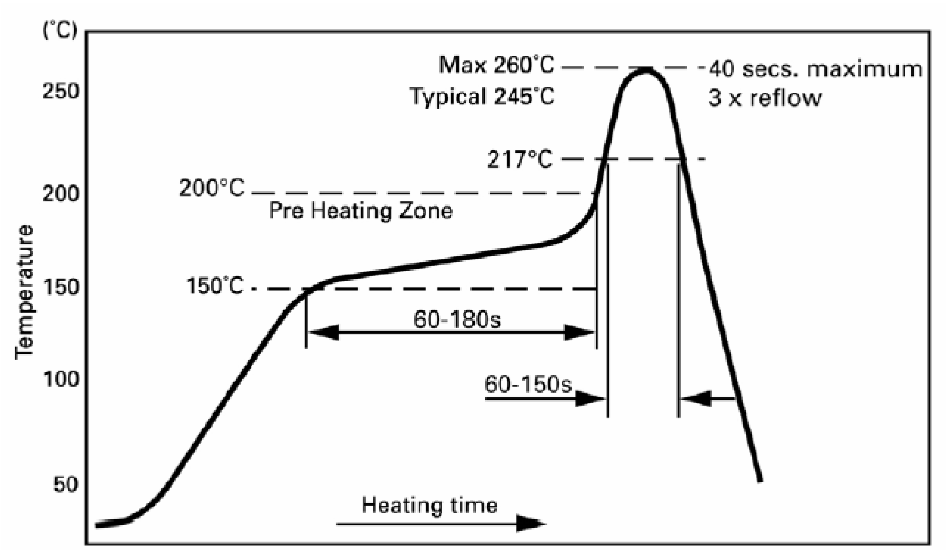


Figure 18 shows the recommeded solder for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 18. Recommended solder profile for leaded devices

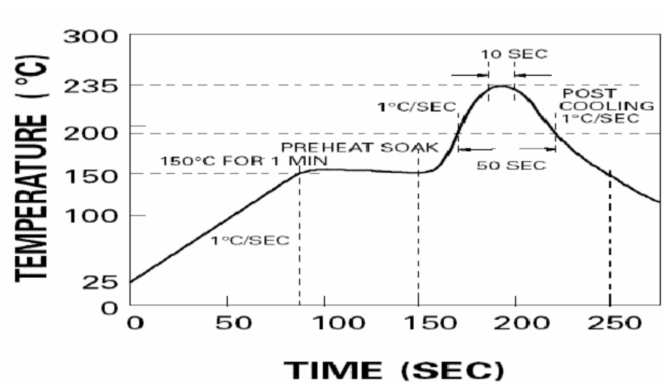
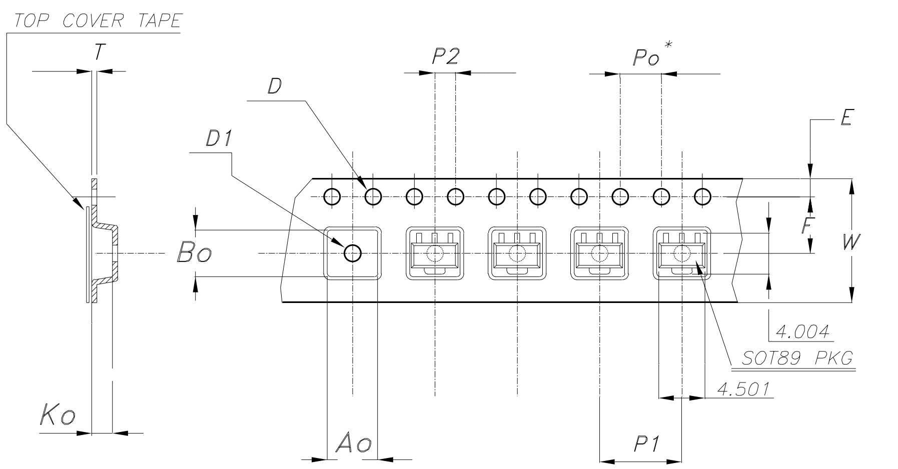


Figure 19. Reel information



Ao	4.91	±0.10
Bo	4.52	±0.10
Ko	1.90	±0.10
F	5.50	±0.10
E	1.75	±0.10
W	12	±0.30
P2	2	±0.10
Po	4	±0.10
P1	8	±0.10
T	0.30	±0.10
D	ø1.55	±0.05
D1	ø1.60	±0.10

NOTES :

– ACCEPTANCE SPEC. Nr. 0031932

* – CUMULATIVE TOLERANCE OF 10 SPROCKET HOLES IS ±0.20

– UNLESS OTHERWISE SPECIFIED TOLERANCE: ±0.10

– MATERIAL CODE : 3CP90069

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
05-Dec-2007	1	Initial release.
22-Aug-2008	2	Updated marking in *Table 1 on page 1*

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