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PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications

Description

PD70210, PD70210A & PD70210AL is an advanced PD Interface Controller (Front-end IC) for Powered Devices in PoE applications. It supports IEEE802.3af, IEEE802at, HDBaseT, and general 2/4-pair configurations.

PD70210, PD70210A & PD70210AL includes an advanced classification block that supports 2, 3, 4, and 6 event classification. Using the SUPP_Sx pins it also identifies which of the four pairs of the cable actually receives power and generates appropriate flags.

The IC features an internal bleeder for discharging the input capacitor of the DC/DC converter rapidly, so as to ensure fast re-detection and port power-up in case of sudden removal and re-insertion of Ethernet cable into RJ-45.

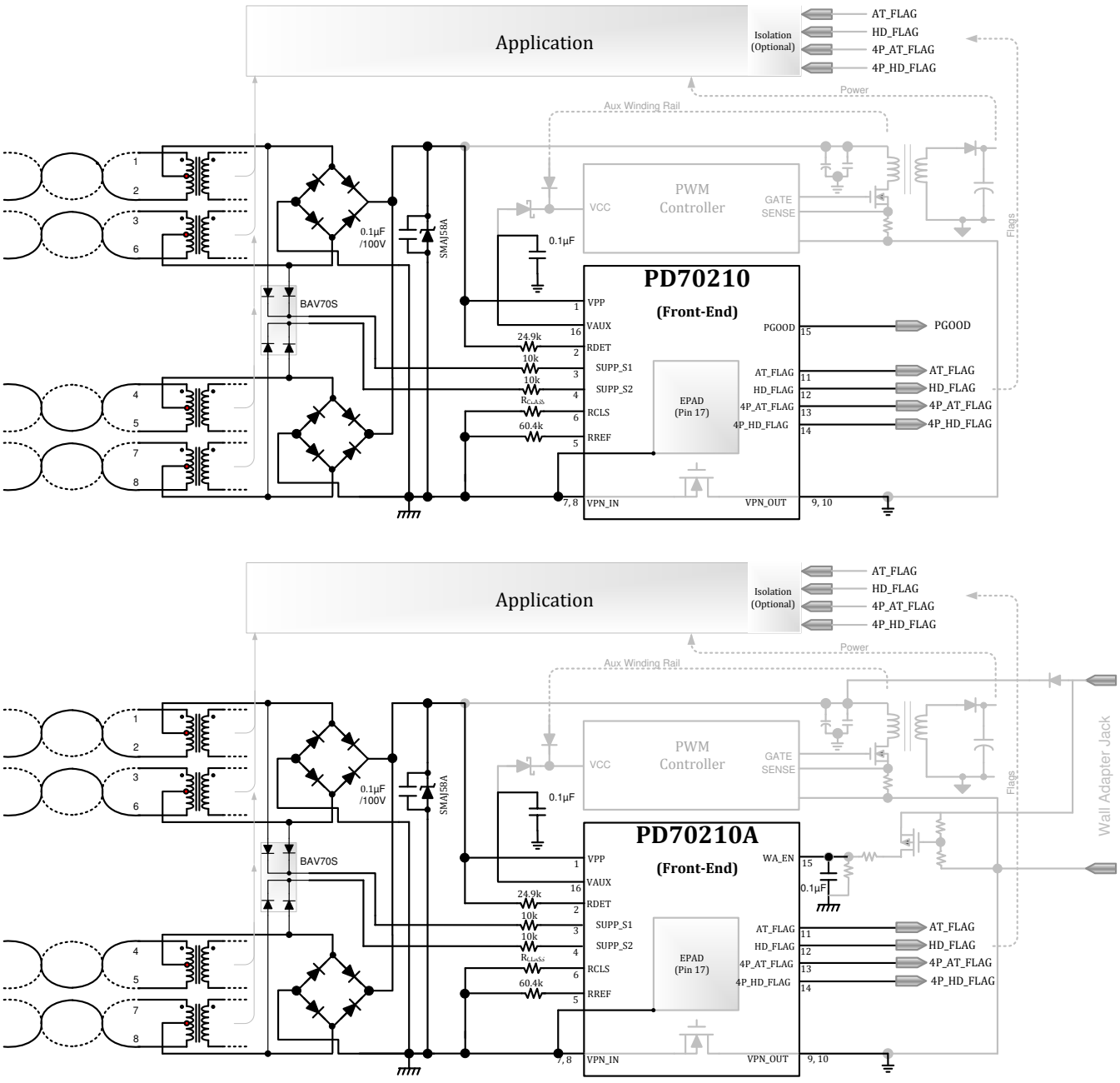
Features

- Supports IEEE802.3af/at, HDBaseT, and other 2-pair/4-pair configurations.
- PD detection & programmable classification
- 2,3,4, and 6 event classification
- Integrated 0.3Ω isolating (series-pass) FET
- Inrush current limiting
- Wall adapter support (PD70210A and PD70210AL Only)
- Less than 5µA offset current during detection
- Lead-free DFN-16 / QFN-38 package

Applications

- Single HDBaseT or Twin up to 95 Watts
- IEEE802.3af and 802.3at
- Indoor and outdoor PoE

Typical application



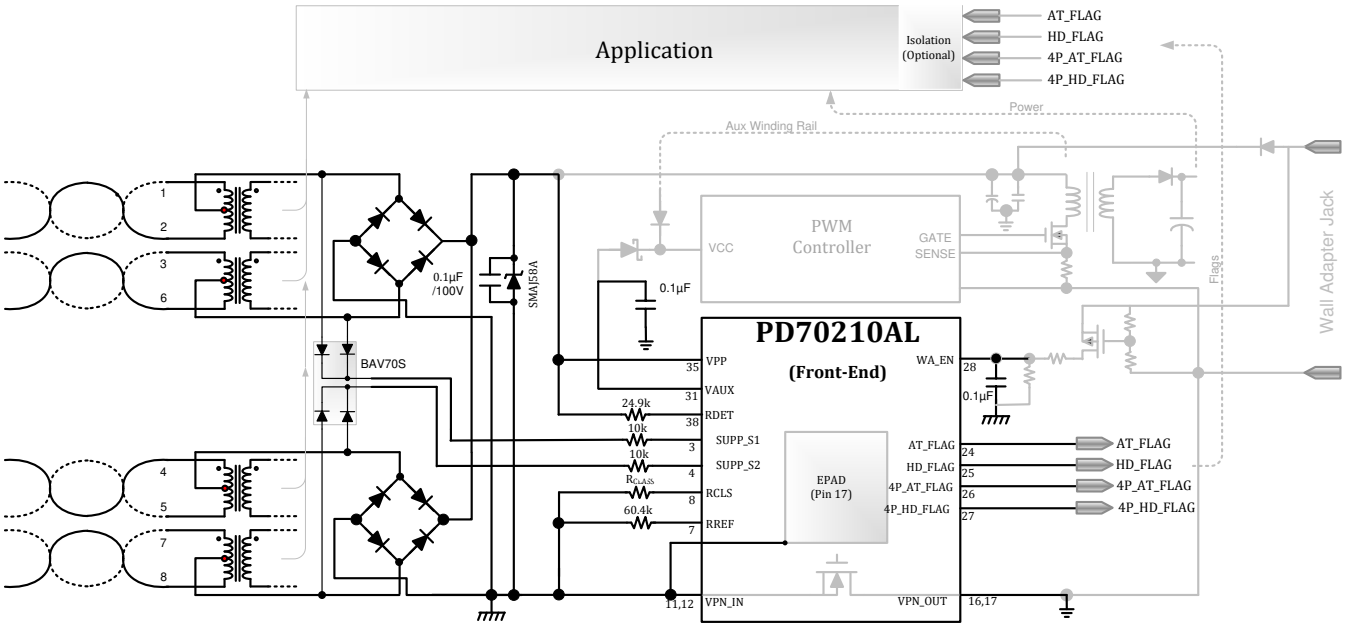
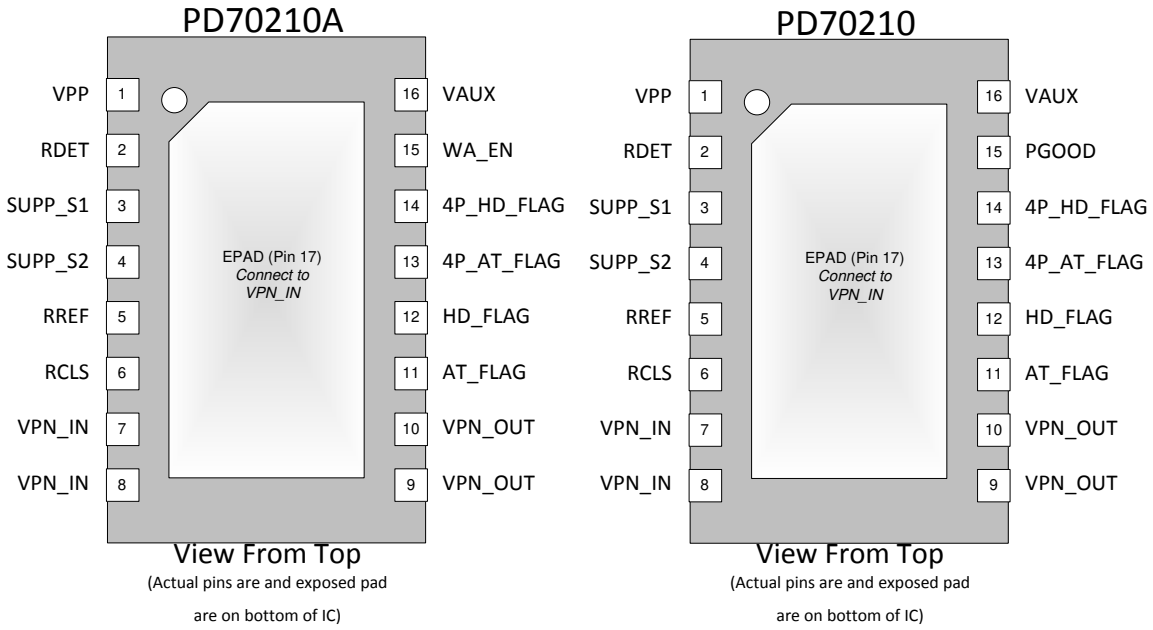


Figure 1: Typical Applications Diagram

Pin Configuration



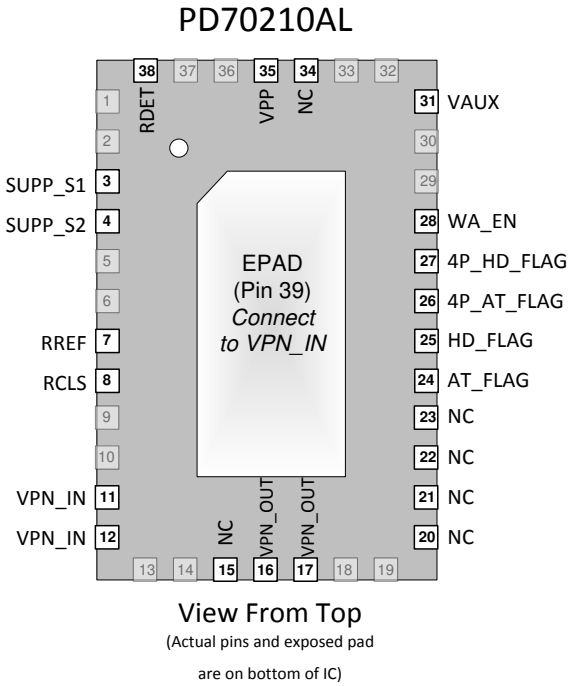


Figure 2: Pinout

** Shaded pins are not exist

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Part Marking
-40°C to 85°C	RoHS compliant, Pb-free	DFN 5 × 4 mm 16L (0.5mm pitch)	PD70210AILD	Bulk	Microsemi Logo 70210A YYWWX* MSC
			PD70210AILD-TR	Tape and Reel	
-40°C to 85°C	RoHS compliant, Pb-free	DFN 5 × 4 mm 16L (0.5mm pitch)	PD70210ILD	Bulk	Microsemi Logo 70210 YYWWX* MSC
			PD70210ILD-TR	Tape and Reel	
-40°C to 85°C	RoHS compliant, Pb-free	QFN 5 × 7 mm 38L (0.5mm pitch)	PD70210ALILQ	Bulk	Microsemi Logo MSC 70210AL YYWWX*
			PD70210ALILQ-TR	Tape and Reel	

*Year / Week / Lot number

Selection guide

Feature / IC	PD70210	PD70210A	PD70210AL
Wall adapter support	NA	Available	Available
2P/4P HDBaseT support	Available	Available	Available
Package	DFN 5 × 4 mm 16L	DFN 5 × 4 mm 16L	QFN 5 × 7 mm 38L
Clearance between HV pins	0.2mm	0.2mm	1mm

Pin Description

(PD70210 / PD70210A - DFN 5 × 4 mm 16L)

Pin #	Designator PD70210A	Designator PD70210	Description
1	VPP	VPP	Upper rail of the incoming PSE voltage rail – from the positive terminal of the two OR-ed bridge rectifiers (the corresponding lower PoE rail is VPN_IN)
2	RDET	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25KΩ (or 24.9K), 1% resistor is connected between this pin and VPP
3	SUPP_S1	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S2 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only). Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
4	SUPP_S2	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S1 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only) . Signal is referenced to VPN_IN Place a 10K resistor in the input of this pin.
5	RREF	RREF	Bias current resistor. A 60.4k, 1% resistor is connected between RREF and IC ground (VPN_IN)
6	RCLS	RCLS	Sets the Class of the PD. Connect R_{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4 respectively. If R_{CLASS} is not present, the PD will draw up to 3 mA during classification, thus indicating Class 0 (default Type 1) to the PSE. Signal is referenced to VPN_IN
7, 8	VPN_IN	VPN_IN	Lower rail of the incoming PSE voltage rail – from the negative terminal of the two OR-ed bridge rectifiers (the corresponding upper PoE rail is VPP)
9, 10	VPN_OUT	VPN_OUT	This is in effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and Power-up. It is connected to the Power ground and PWM controller IC's ground plane of the DC-DC converter section
11	AT_FLAG	AT_FLAG	Open Drain Output. This pin gets actively pulled low when a Type 2 PD-PSE mutually identifies each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
12	HD_FLAG	HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
13	4P_AT_FLAG	4P_AT_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identifies each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
14	4P_HD_FLAG	4P_HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
15	WA_EN		While this input is low (referenced to VPN_IN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature. Place 100nF/10V capacitor from WA_EN to VPN_IN pins, locate it close to device. When WA_EN is not used, connect it to VPN_IN. For further information, refer to External source connected to PD device output.
		PGOOD	Open Drain Output. Power Good output signal from the Front-End stage. This pin gets actively pulled low when power-on occurs. There is a minimum 80 ms delay from the moment VPort exceeds UVLO (~36V), to this PGOOD signal being driven low as per the IEEE standard, to allow the PSE to increase its current limit after power-up is completed. Signal is referenced to VPN_OUT.

16	**VAUX**	**VAUX**	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (at typically 10.5V). Signal is referenced to VPN_OUT and is activated once front end power up sequence is end. DC-DC should not startup until Vaux is active.
17	**EPAD**	**EPAD**	Connected on PCB plane to VPN_IN

(PD70210AL - QFN 5 × 7 mm 38L)

Pin #	Designator PD70210AL	Description
1-2	**NA**	
3	**SUPP_S1**	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S2 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only). Signal is referenced to VPN_IN Place a 10K resistor in the input of this pin.
4	**SUPP_S2**	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S1 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only) . Signal is referenced to VPN_IN Place a 10K resistor in the input of this pin.
5-6	**NA**	
7	**RREF**	Bias current resistor. A 60.4k, 1% resistor is connected between this and IC ground (VPN_IN)
8	**RCLS**	Sets the Class of the PD. Connect R_{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4 respectively. If R_{CLASS} is not present, the PD will draw up to 3 mA during classification, thus indicating Class 0 (default Type 1) to the PSE. Signal is referenced to VPN_IN
9-10	**NA**	
11-12	**VPN_IN**	Lower rail of the incoming PSE voltage rail – from the negative terminal of the two OR-ed bridge rectifiers (the corresponding upper PoE rail is VPP)
13-14	**NA**	
15	**NC**	
16-17	**VPN_OUT**	This is in effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and Power-up. It is connected to the Power ground and PWM controller IC's ground plane of the DC-DC converter section
18-19	**NA**	
20-23	**NC**	
24	**AT_FLAG**	Open Drain Output. This pin gets actively pulled low when a Type 2 PD-PSE mutually identifies each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
25	**HD_FLAG**	Open Drain Output. The pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
26	**4P_AT_FLAG**	Open Drain Output. The pin gets actively pulled low when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identifies each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT

27	**4P_HD_FLAG**	Open Drain Output. The pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT
28	**WA_EN**	While this input is low (referenced to VPN_IN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature. Place 100nF/10V capacitor from WA_EN to VPN_IN pins, locate it close to device. When WA_EN is not used, connect it to VPN_IN. For further information, refer to External source connected to PD device output.
29-30	**NA**	
31	**VAUX**	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (at typically 10.5V). Signal is referenced to VPN_OUT and is activated once front end power up sequence is end. DC-DC should not startup until Vaux is active .
32-33	**NA**	
34	**NC**	
35	**VPP**	Upper rail of the incoming PSE voltage rail – from the positive terminal of the two OR-ed bridge rectifiers (the corresponding lower PoE rail is VPN_IN)
36-37	**NA**	
38	**RDET**	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25KΩ (or 24.9K), 1% resistor is connected between this pin and VPP
39	**EPAD**	Connected on PCB plane to VPN_IN

Functional Block Diagram

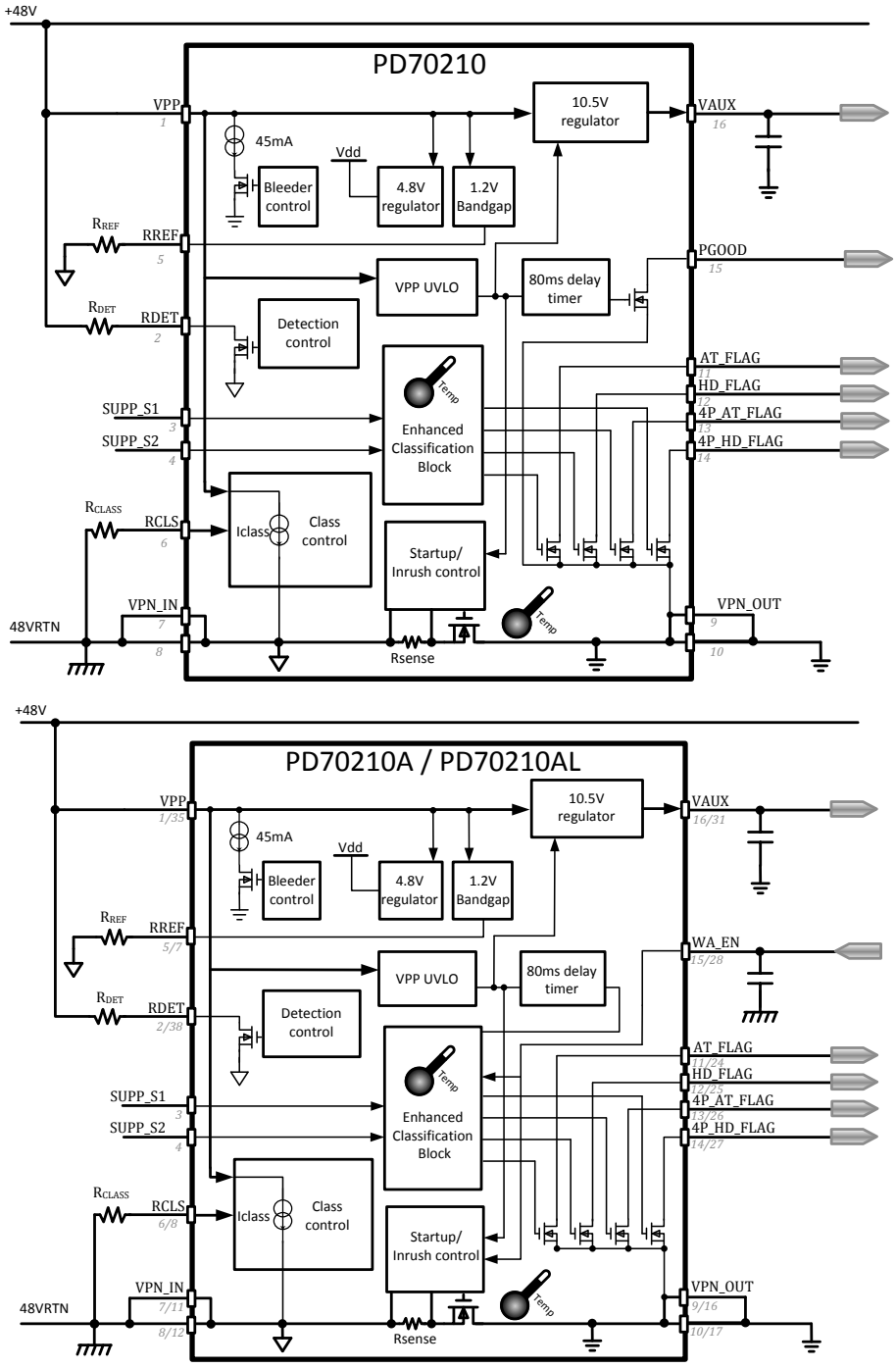


Figure 3: Block Diagram

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability. Voltages are with respect to IC ground (VPN_IN) unless otherwise specified.

		Min	Max	Units
VPP, RDET		-0.3	74	V
PGOOD, AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG referenced to VPN_OUT		-0.3	20	V
SUPP_S1, SUPP_S2		0	V_{VPP} + 1.5	V
RREF, RCLS, WA_EN		-0.3	5	V
Junction Temperature		-40	150	°C
Lead Soldering Temperature (40s, reflow)			260	°C
Storage Temperature		-65	150	°C
ESD rating	HBM (PD70210)		±1.5	kV
	HBM (PD70210A / PD70210AL)		±1.25	kV
	MM		±100	V
	CDM		±500	V

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics. Voltages are with respect to IC ground (VPN_IN).

	Min	Max	Units
VPP	0	57	V
Ambient Temperature*	-40	85	°C
Detection Range	1.1	10.1	V
Mark Event Range	4.9	10.1	V
Class Event Range	13.7	20.9	V

* Corresponding Max Operating Junction Temperature is 125°C.

Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θJA		31		°C/W
θJP		3		°C/W
θJC		4		°C/W

Note: θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} in particular is a function of the PCB construction. Stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values state, are either by design or by production testing at 25°C ambient. Voltages are with respect to IC ground (VPN_IN).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage						
I_{IN}	IC input current with I_{CLASS} off	VPP=55V		1	3	mA
Detection phase						
V_{DET}	Detection range		1.1		10.1	V
R_{DET_TH}	R_{DET} disconnect threshold		10.1		12.8	V
$R_{DS\_DET\_ON}$	On-resistance of internal FET during detection				50	Ω
$R_{DS\_DET\_OFF}$	Off-resistance of internal FET after detection		2			MΩ
I_{OFFSET_DET}	Input offset current	1.1V ≤ VPP ≤ 10.1V, T_J ≤ 85°C			5	µA
$V_{R\_DET\_ON}$	R_{DET} reconnection threshold when VPP goes low		2.8	3.0	4.85	V
Classification phase						
V_{CLS_ON}	Classification sink turn-on threshold		11.4		13.7	V
V_{CLS_OFF}	Classification sink turn-off threshold		20.9		23.9	V
$V_{HYS\_CLS\_ON}$	Hysteresis of V_{CLS_ON} threshold			1		V
V_{MARK_TH}	Mark detection threshold (VPP falling)		10.1		11.4	V
I_{MARK}	Current sink in Mark event region		0.25		4	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CLASS_CLIM}	Current limit of class current		50	68	80	mA
I_{CLASS}	Classification current sink	R_{CLASS} = not present (Class 0)			3	mA
		R_{CLASS} = 133 Ω (Class 1)	9.5	10.5	11.5	
		R_{CLASS} = 69.8 Ω (Class 2)	17.5	18.5	19.5	
		R_{CLASS} = 45.3 Ω (Class 3)	26.5	28.0	29.5	
		R_{CLASS} = 30.9 Ω (Class 4)	38.0	40.0	42.0	
Isolation FET						
R_{DSON}	On resistance	Total resistance between VPN_IN to VPN_OUT; I_{LOAD} < 600mA, -40°C <T_A< 85°C		0.22	0.3	Ω
I_{CLIM_INRUSH}	Inrush current limit		105	240	325	mA
OCP	Overcurrent protection		2.2			A
I_{LOAD}	Continuous operation load (*)				2	A
Undervoltage Lockout						
$UVLO_{ON}$	Threshold that marks start of Inrush phase		36		42	V
$UVLO_{OFF}$	Threshold where pass-FET turns off as VPP collapses		30.5		34.5	V
DC-DC Input Cap Discharger						
I_{CAP_DIS}	Discharge current (PD70210)	12V ≤ VPP ≤ 30V	22.8		60	mA
		7V ≤ VPP ≤ 12V	10			mA
I_{CAP_DIS}	Discharge current (PD70210A)	7V ≤ VPP ≤ 30V	22.8		60	mA
$timer_{dis}$	Discharge timer	Time for which discharge circuit is activated	430			ms
References, Rails and Logic						
V_{AUX}	Auxiliary voltage	0mA < I_{AUX} < 4mA	9.8	10.5	12.0	V
I_{AUX_CLIM}	Aux current limit		10		32	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	Bias current reference voltage		1.17	1.2	1.23	V
v_{FLAG_LO}	Low level flag	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG, I_{FLAG}= 3mA			0.4	V
V_{PGOOD_LO}	Power good active low voltage	I_{PGOOD} = 3mA **PD70210 Only*			0.4	V
t_{FLAG}	Delay timer between start of inrush and flags declared	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	80			ms
t_{PGOOD}	Delay timer between start of inrush and power good declared	**PD70210 Only*	80			ms
I_{FLAG_max}	Flag Current driving capability	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	5			mA
I_{PGOOD_max}	Power good current capability	**PD70210 Only*	5			mA
V_{SUPP_HI}	SUPP_Sx high voltage threshold	For SUPP_S1 and SUPP_S2	25		35	V
Wall Adapter enable pin						
V_{IH}	Input high logic	**PD70210A, PD70210AL Only*	2.4			V
V_{IL}	Input low logic	**PD70210A, PD70210AL Only*			0.8	V

(*) Actual maximum load is subject to the application environment conditions, such as ambient temperatures, air flow, mutual heating by other components etc.

Truth Table for Status of Flags

Number of Fingers "N" (N-Event Classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi Z	Hi Z	Hi Z	Hi Z
2	H	L	0V	Hi Z	Hi Z	Hi Z
2	L	H	0V	Hi Z	Hi Z	Hi Z
2	H	H	0V	Hi Z	0V	Hi Z
3	L	H	0V	0V	Hi Z	Hi Z
3	H	L	0V	0V	Hi Z	
3	H	H	0V	0V	0V	Hi Z
4	X	X	0V	0V	0V	Hi Z
5	RESERVED FOR FUTURE					
6	X	X	0V	0V	0V	0V

Note: Flags state is set only once at port turn on, while VPP-VPNin voltage crosses $UVLO_{ON}$. If SUPP_S1 and SUPP_S2 pins are changing after port turn on, the flags do not change accordingly.

Wall Adapter mode (PD70210A/L)

PD70210A / PD70210AL support wall adapter functionality, i.e. by setting WA_EN pin high it will give priority to the wall adapter jack to supply the load.

WA_EN pin is used while connecting a wall-adapter voltage between VPP and VPN_OUT by means of an OR-ing diode.

While WA_EN, Wall-adapter enable pin, is held low (referenced to VPN_IN), the front-end works as a normal PD.

When WA_EN is raised high (referenced to VPN_IN) three internal operations are forced:

- The Isolation FET is turned OFF.
- All output flags AT_FLAG, HD_FLAG, 4P_AT_FLAG and 4P_HD_FLAG are activated (low state).
- Vaux output voltage is turned ON.

While activating WA_EN pin, the wall-adapter will supply input voltage for the DC-DC converter.

Having WA_EN at high state does not dis able detection and classification modes.

Applications Information

PD70210 application is described in the following paragraph

Peripheral devices

- An 100nF/100V capacitor should be placed between device VPP and VPNI pins, and located as close as possible to the device.
- An 58V TVS should be placed between device VPP and VPNI pins.
- An 10K ohm resistor should be placed on SUPP_S1 and SUPP_S2 lines between diode bridge and PD70210/A device.
- When WA_EN is used, an 100nF/10V Capacitor should be placed between WA_EN and VPNi pin close to PD70210/A device.
- When not used, WA_EN should be connected to VPNi pin.

The Peripheral d devices are presented in Figure 4 and Figure 5.

Operation with an External DC Source

PD applications utilizing PD70210A IC may be operated with an external power source (DC wall adaptor). There are two cases of providing power with an external source, the cases are presented in Figure 4 and Figure 5.

1) External source connected to application's low voltage supply rails. External source voltage level is dependent on DCDC output characteristics. Described in Figure 4
2) External source connected to PD device output connection toward the application (VPP to VPN_{OUT}). External source voltage level is dependent on DCDC input requirements. Described in Figure 5

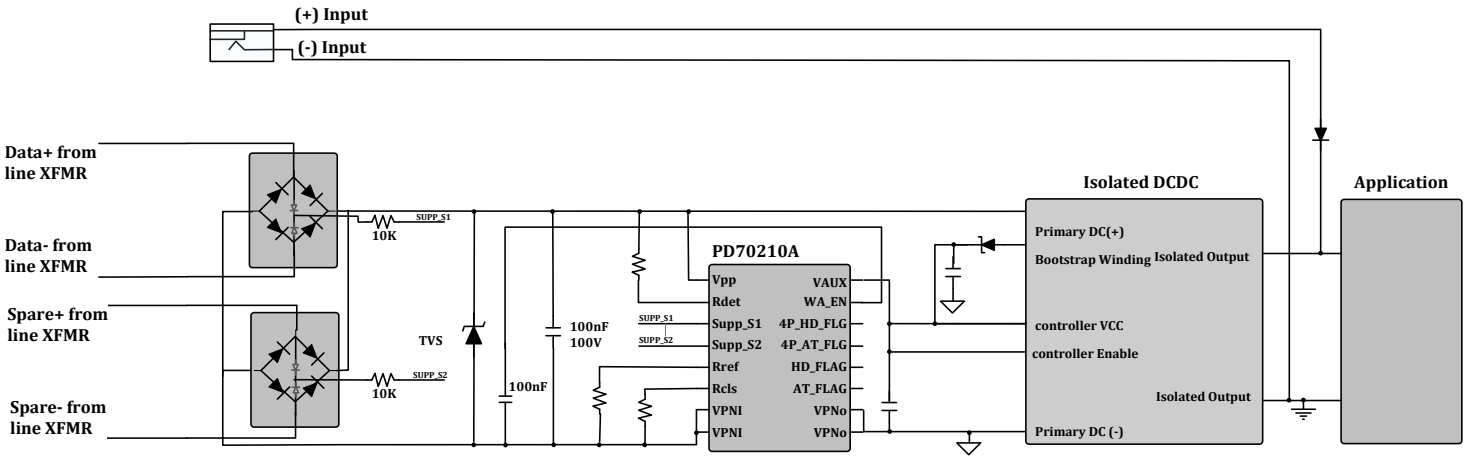


Figure 4: External Power Input connected to Application supply Rails

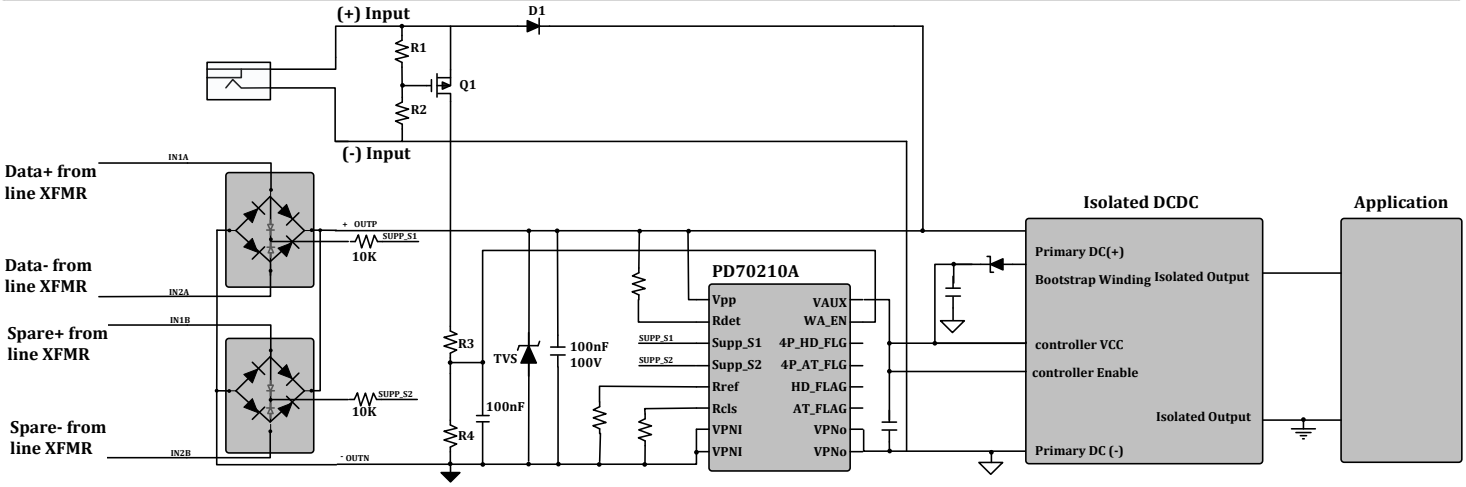


Figure 5: External Power Input connected to PD70210A Output

External source connected to PD device output (Figure 5)

PD70210A WA_EN pin is used for disabling the isolation switch and thus PSE input power, when an external adapter is connected.

WA_EN resistors divider depends on the VinH threshold of the PD70210A.

Figure 6 is zooming into the resistors to be selected in external adapter connection.

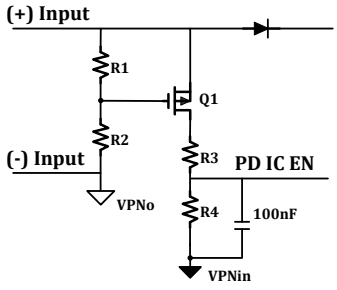


Figure 6: External Power Input resistors dividers

R1 and R2 sets a rough threshold for Pfet Q1 enable, to detect whether external adapter exists or not. It should be set to be lower threshold than PD70210A disable levels.

R3 and R4 sets PD70210A disable threshold.

So in case of 36V-57V external adapter. The disable setting can be selected as follows:

Pfet enable threshold = 30V.

R1 and R2 setting should be so that the value of Q1 VGS < 20V at max voltage condition of external adapter.

While external adapter voltage is above 30V, Q1 will be above its VGS_{th} value.

$$VGS = Vext\_adapter \times \frac{R1}{R1 + R2}$$

R1 is selected as 2KΩ.

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

Using R1=2KΩ, Vext_adapter=30V and VGS= maximum VGS_{th} =3.5V. we get R2 value.

$$R2 = 15K\Omega$$

R3 and R4 are set to the range of few KΩ- 10's of KΩ using the equation below:

=

(I) $PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4}{(R3+R4)}$

Using R3=15KΩ, Vext_adapter=33.7V and from data sheet we use PD70210A_WA_EN=2.4V as turn Off min threshold.

Solving the equation , we get the valid resistors values for an adapter of 36V and above.

$$R3 = 15K\Omega$$

$$R4 = 1.15K\Omega$$

Thermal Protection

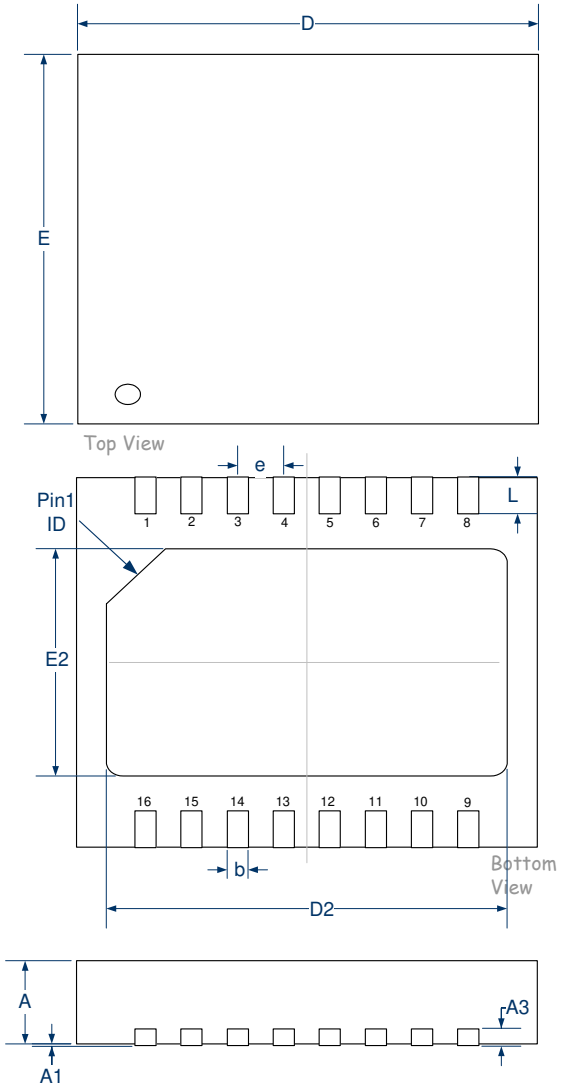
PD70210, PD70210A & PD70210AL are protected from excessive internal temperatures that may occur during various operating procedures. Two temperature sensors are located on the chip, monitoring the temperatures of the following:

- Isolating Switch (pass-FET)
- Classification Current Sink

Each of the over temperature sensor activates a protection mechanism that will disconnect the Isolation (pass) FET or the classification circuit respectively. This protects the device from being permanently damaged or even from long-term degradation.

Package Dimensions

LD **16 Pin Plastic DFN 5x4 mm**

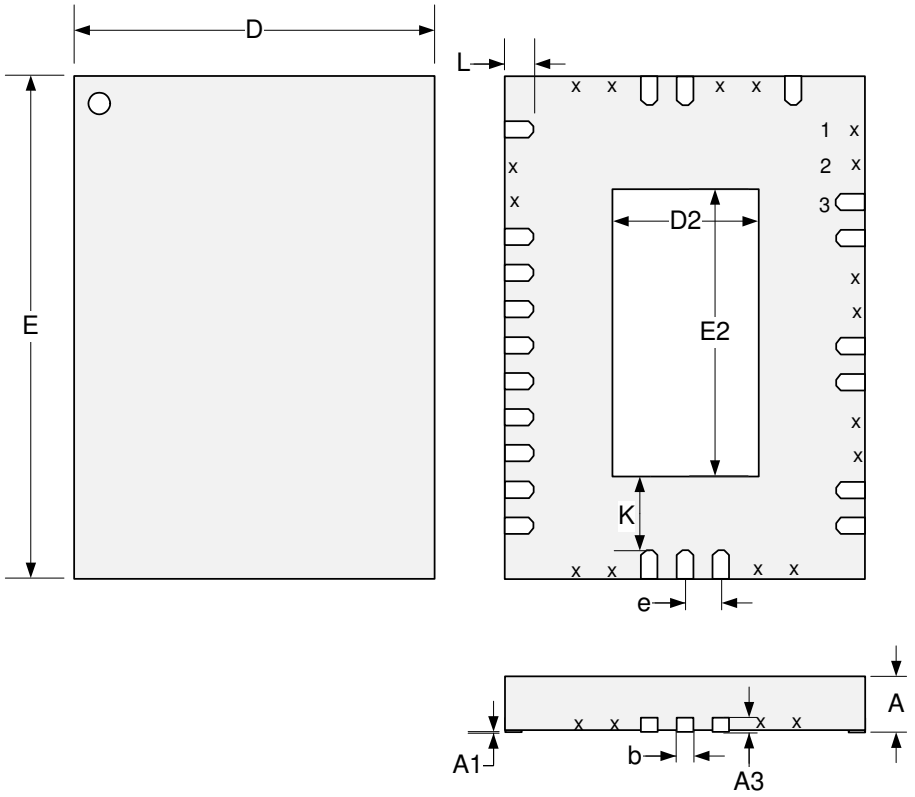


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
D	5.00 BSC		0.197 BSC	
E	4.00 BSC		0.157 BSC	
D2	4.20	4.45	0.165	0.175
E2	2.30	2.55	0.091	0.100
e	0.50 BSC		0.0197 BSC	
K	0.20 MIN		0.008 MIN	
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

LD 38 Pin Plastic QFN 5x7 mm



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.196 BSC	
E	7.00 BSC		0.275 BSC	
D2	1.85	2.10	0.073	0.083
E2	3.85	4.10	0.152	0.161
e	0.50 BSC		0.020 BSC	
K	1.016	-	0.040	-
L	0.30	0.50	0.012	0.020

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 10 June 2013	-	Initial Release
1.1 / 16 Oct 2013	-	Fix Vaux description and cap GND symbol
1.2 / 05 Nov 2013	-	Fix Figure 1 RREF
1.34 / 31 Dec 2013	Package	Add new package option PD70210AL 38pin 5 X 7 QFN Update package drawing and add application diagram for the new package Update Flag table and typos
1.36 / 07 Jan 2014		Adding IC marking information
1.37 / 24 Jan 2014		Fix ILQ package information
1.38 / 24 Apr 2014		Add continous current and thermal properties
1.40 / 25 June 2014		Add WA_EN information
1.50 / 07 Oct 2014	Page 14	Add details for Flags description
1.51 / 08 Oct 2015	Page 7, 8 Page 12	Fix Vaux pin description (without 80mS delay), Add UVLO_ON missing information.

For support contact: **sales_AMSG@microsemi.com**

Visit our web site at: **www.microsemi.com** **Catalog Number**: DS_PD70210_PD70210A