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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



PE4140

Ultra-High Linearity UltraCMOS™ Broadband Quad MOSFET Array

Features

- Ultimate Quad MOSFET array
- Ultra-high linearity, broadband performance beyond 6.0 GHz
- Ideal for mixer applications
- Up/down conversion
- Low conversion loss
- High LO Isolation
- Packaged in small 6-lead 3x3 mm DFN

Product Description

The PE4140 is an ultra-high linearity passive broadband Quad MOSFET array with high dynamic range performance capable of operation beyond 6.0 GHz. This quad array operates with differential signals at all ports (RF, LO, IF), allowing mixers to be built that use LO powers from -7 dBm to +20 dBm. Typical applications range from frequency up/down-conversion to phase detection for Cellular/PCS Base Stations, Wireless Broadband Communications and STB/Cable modems.

The PE4140 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

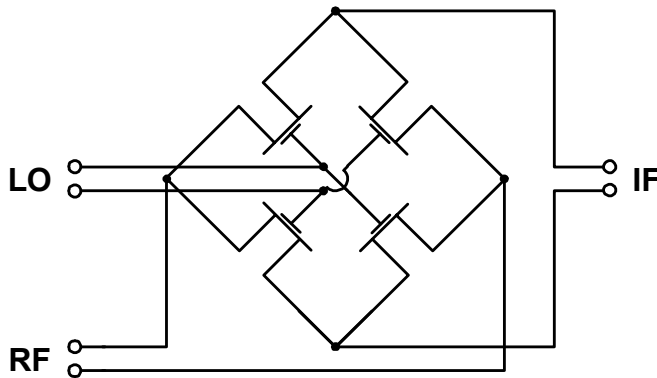


Figure 2. Package Type

6-lead DFN



Table 1. AC and DC Electrical Specifications @ +25 °C

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Units
F_{TYP}	Operating Frequency Range ¹		DC		6.0	GHz
V_{DS}	Drain-Source Voltage	$V_{GS} = +3V, I_{DS} = 40 \text{ mA}$	260	320	380	mV
$V_{DS \text{ Match}}$	Drain-Source Voltage Match			12	40	mV
V_T	Threshold Voltage	$V_{DS} = 0.1V$; per ASTM F617-00		-100		mV
R_{DS}	Drain-Source 'ON' Resistance	$V_{GS} = +3V, I_{DS} = 40 \text{ mA}$	6.5	7.75	9.5	Ω

Note 1: Typical untested operating frequency range of Quad MOSFET transistors.

Figure 3. Pin Configuration (Top View)

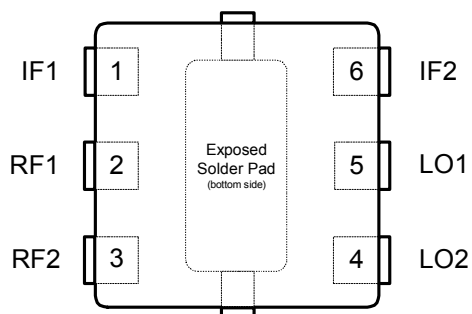


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	IF1	IF Output Connection (Drain)
2	RF1	RF Input Connection (Source)
3	RF2	RF Input Connection (Source)
4	LO2	LO Input Connection (Gate)
5	LO1	LO Input Connection (Gate)
6	IF2	IF Output Connection (Drain)

Table 3. Absolute Maximum Ratings

Symbol	Parameters/Conditions	Min	Max	Units
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
V_{DC+AC}	Maximum DC plus peak AC voltage across Drain-Source		±3.3	V
V_{DC+AC}	Maximum DC plus peak AC voltage across Gate-Drain or Gate-Source		±4.2	V
V_{ESD}	HBM ¹ ESD Voltage		100	V

Note 1: ML_STD 883 Method 3015.7

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

This MOSFET device has minimally protected inputs and is highly susceptible to ESD damage. When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Description

The PE4140 passive broadband Quad MOSFET array is designed for use in up-conversion and down-conversion applications for high performance systems such as cellular infrastructure equipment and STB/CATV systems.

The PE4140 is an ideal mixer core for a wide range of mixer products, including module level solutions that incorporate baluns or other single-ended matching structures enabling three-port operation.

The performance level of this passive mixer is made possible by the very high linearity afforded by Peregrine's UltraCMOS™ process.

Marking

Packaged devices are marked with part number "4140", date code and lot code.

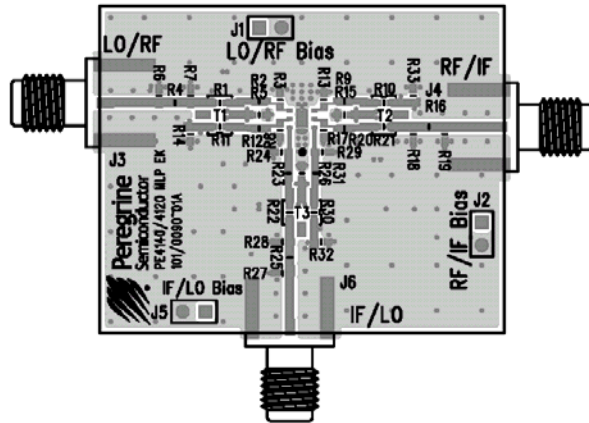
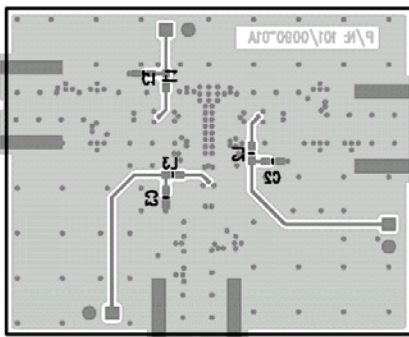
Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4140 in the 6-lead 3x3 DFN package is MSL1.

Evaluation Kit

Figure 4. Evaluation Board Layout

Peregrine Specification 101/0090



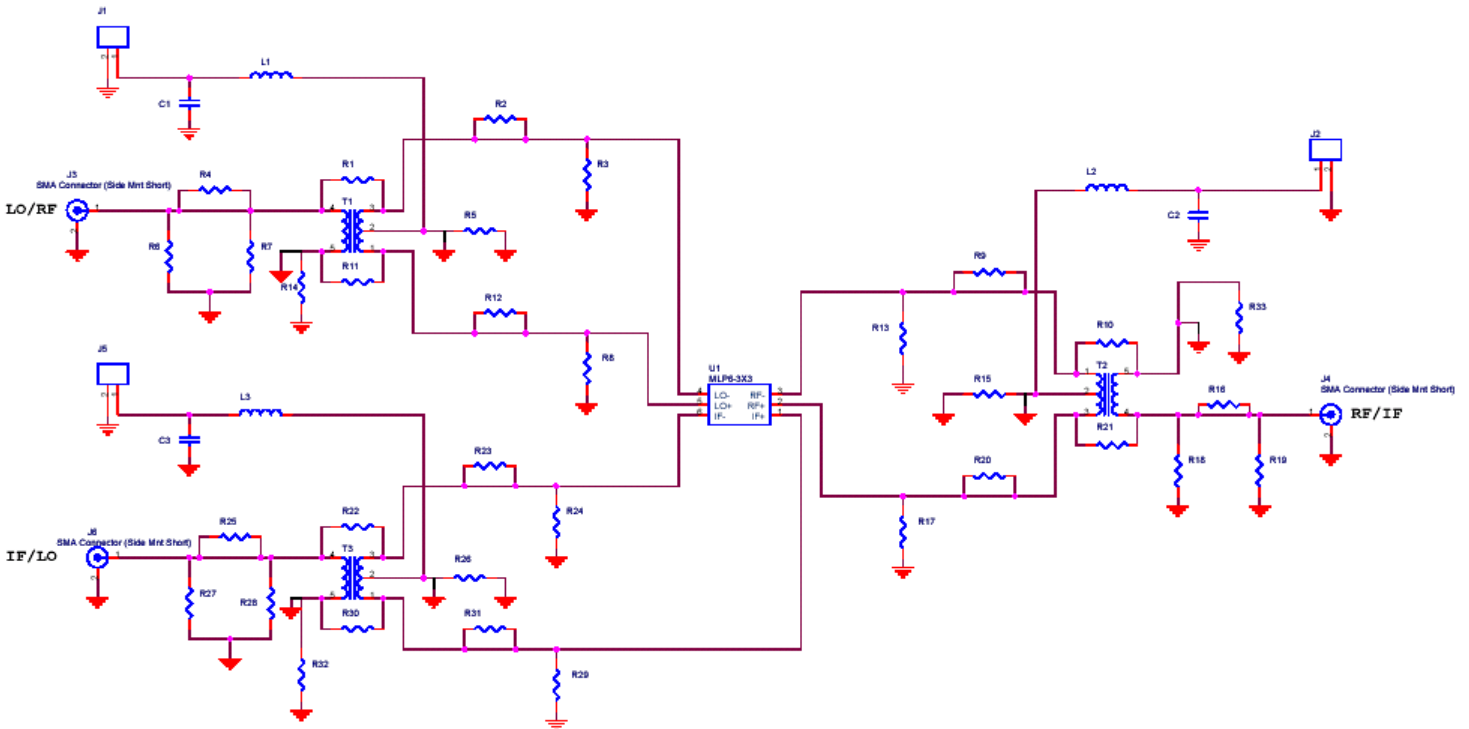
Applications Support

If you have a problem with your evaluation kit or if you have applications questions, please contact applications support:

E-Mail: help@psemi.com (fastest response)
Phone: (858) 731-9400

Figure 5. Evaluation Board Schematic

Peregrine Specification 102/0115



Note: This is the complete evaluation board schematic; which can be used for multiple configurations. Not all components need be populated. Refer to 'typical schematics' on following pages.

Figure 6. Typical Schematic for a PCS Application

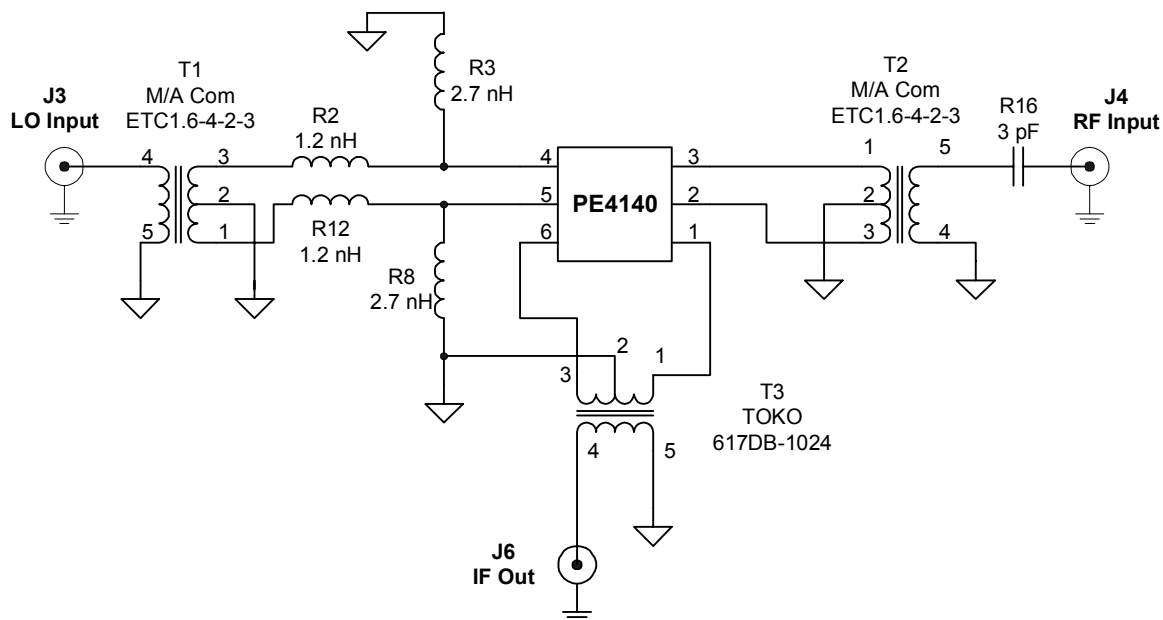


Table 4. Typical Performance in a PCS Application @ +25 °C

Parameter	Minimum	Typical	Maximum	Units
Frequency Range**				
LO	1630	--	2130	MHz
RF	1700	--	2200	MHz
IF		70		MHz
Conversion Loss** (Includes balun losses)		8.5		dB
Isolation**				
LO-RF		36		dB
LO-IF		26		dB
Input IP3**		32		dBm
Input 1 dB Compression**		22		dBm

** Data taken on an Evaluation Board narrow-band tuned to cover the PCS band, IF = 73MHz low-side, LO drive = 17dBm.

Typical Performance Plots in a PCS Application @ +25 °C (LO=17 dBm, IF=73 MHz Low-side)

Figure 7. IIP3 vs. Frequency

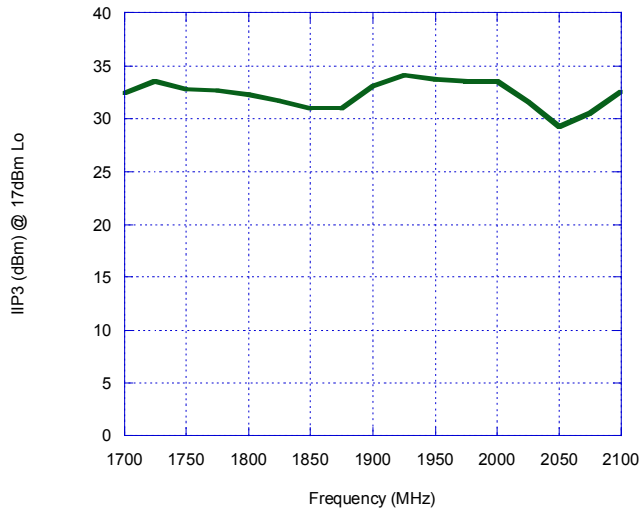


Figure 8. Conversion Loss vs. Frequency

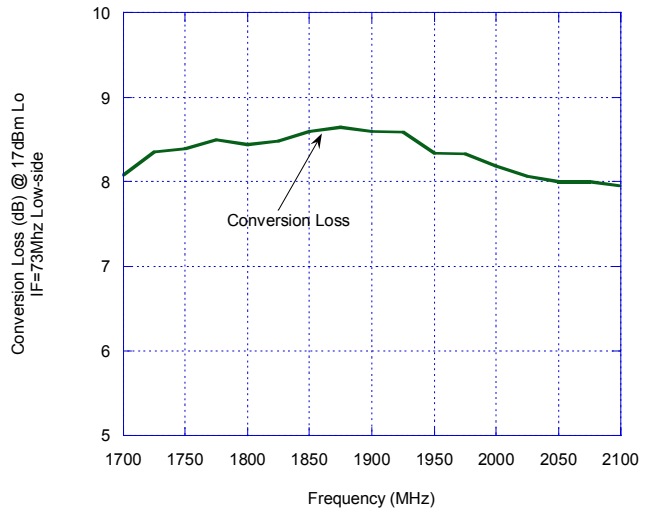


Figure 9. LO-RF & LO-IF Isolation

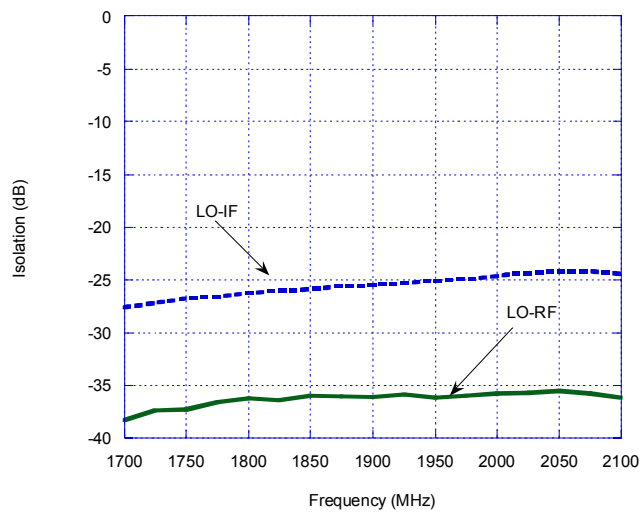
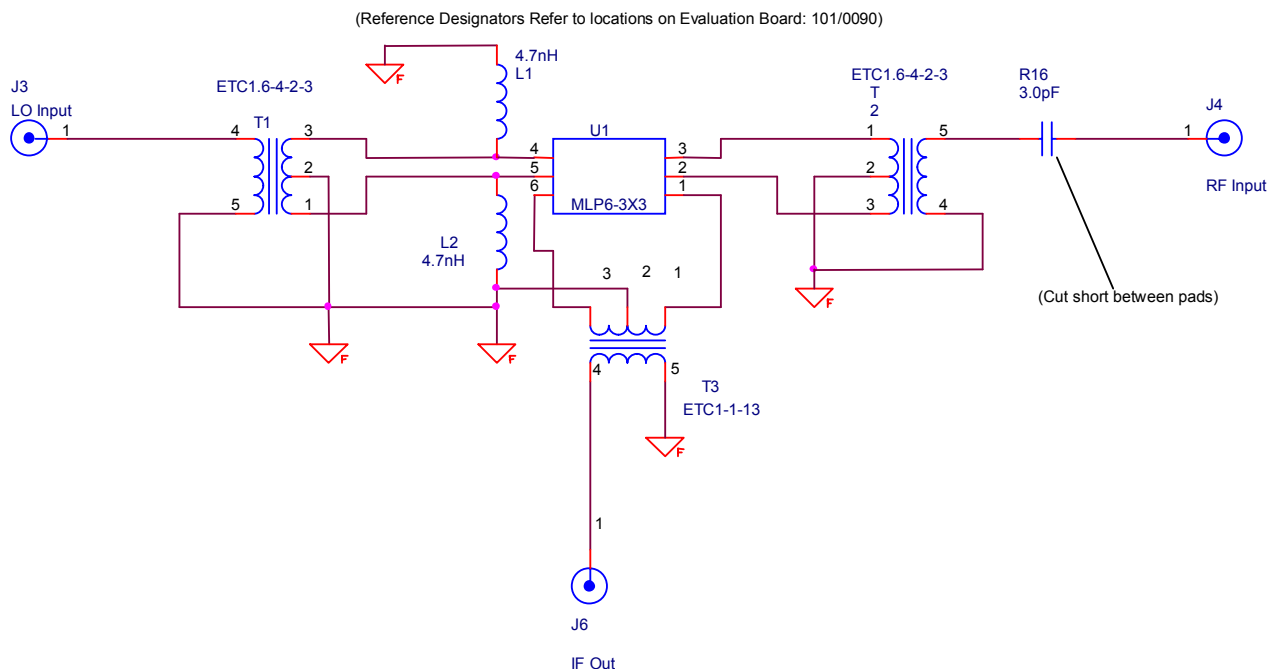


Figure 10. Typical Schematic for a CATV Application



Note: L1 and L2 provide LO port matching for optimum performance. Typical gate capacitance is approximately 2.5 pF.

Table 5. Typical Performance in a CATV Application @ +25 °C

Parameter	Minimum	Typical	Maximum	Units
Frequency Range**				
LO	1116	--	1926	MHz
RF	54	--	864	MHz
IF		1062		MHz
Conversion Loss** (Includes balun losses)		6.5		dB
Isolation**				
LO-RF		40		dB
LO-IF		28		dB
Input IP3**		23		dBm
Input 1 dB Compression**		13		dBm

** Data taken on an Evaluation Board tuned for a broadband CATV application, IF = 1062 MHz, RF drive = -5 dBm, LO drive = 10 dBm.

Typical Performance Plots in a CATV Application @ +25 °C

Figure 11. IIP3 vs. Frequency

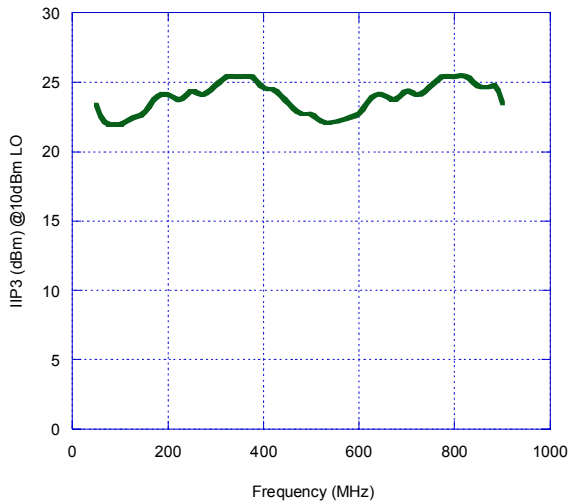


Figure 12. Conversion Loss vs. Frequency

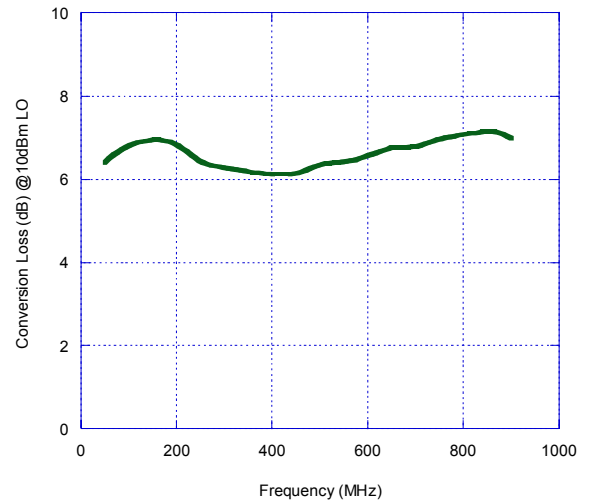


Figure 13. LO-RF & LO-IF Isolation

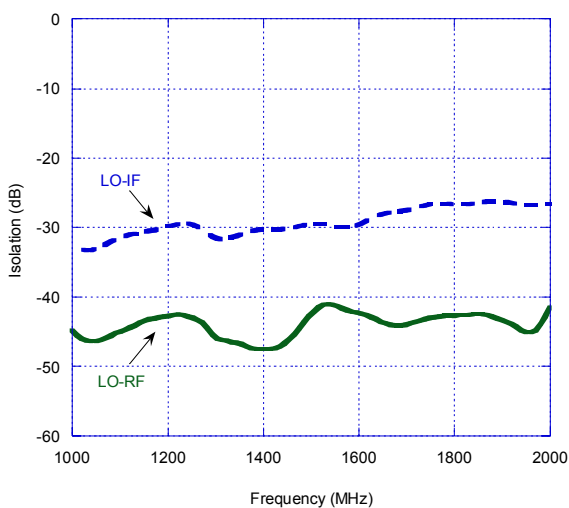
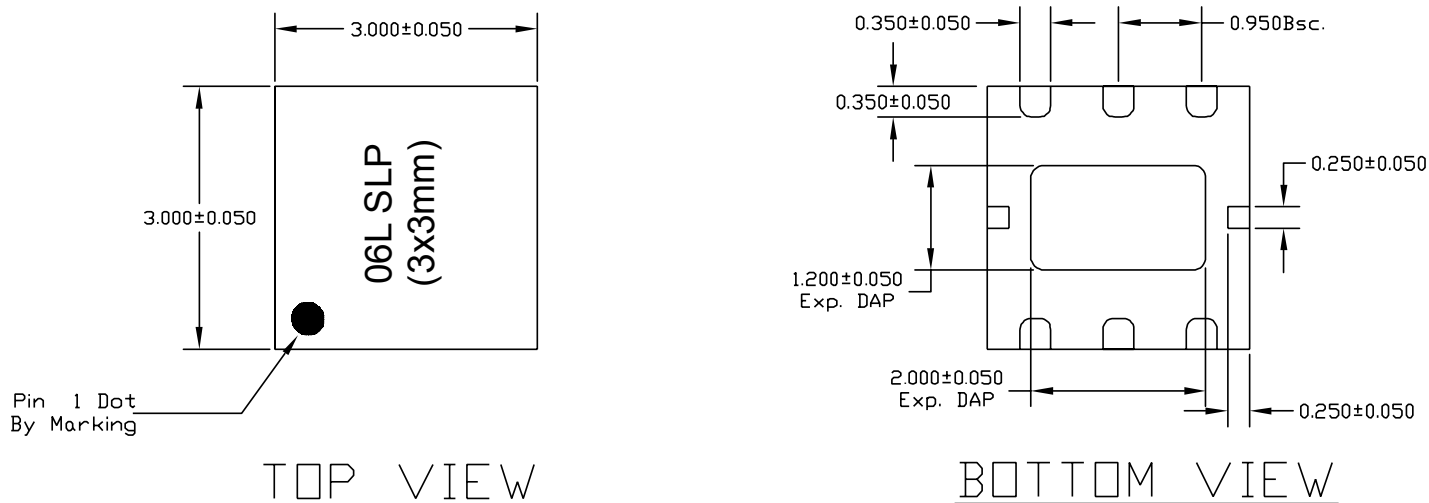


Figure 14. Package Drawing

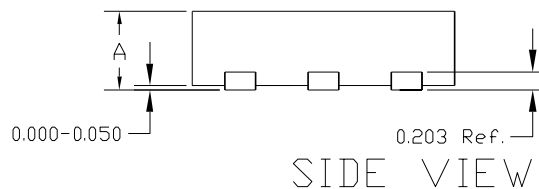
6-lead DFN



NOTE:

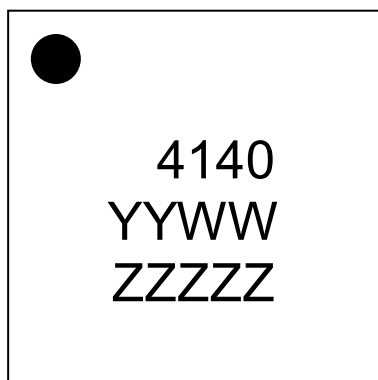
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800



NOTE: The exposed solder pad (on the bottom of the package) is not electrically connected to any other pin (isolated).

Figure 15. Marking Specifications



YYWW = Date Code (last two digits of year and work week)
ZZZZ = Last five digits of Lot Number

Figure 16. Tape and Reel Specifications

6-lead DFN

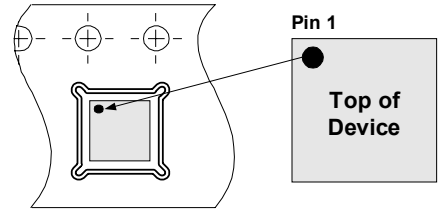
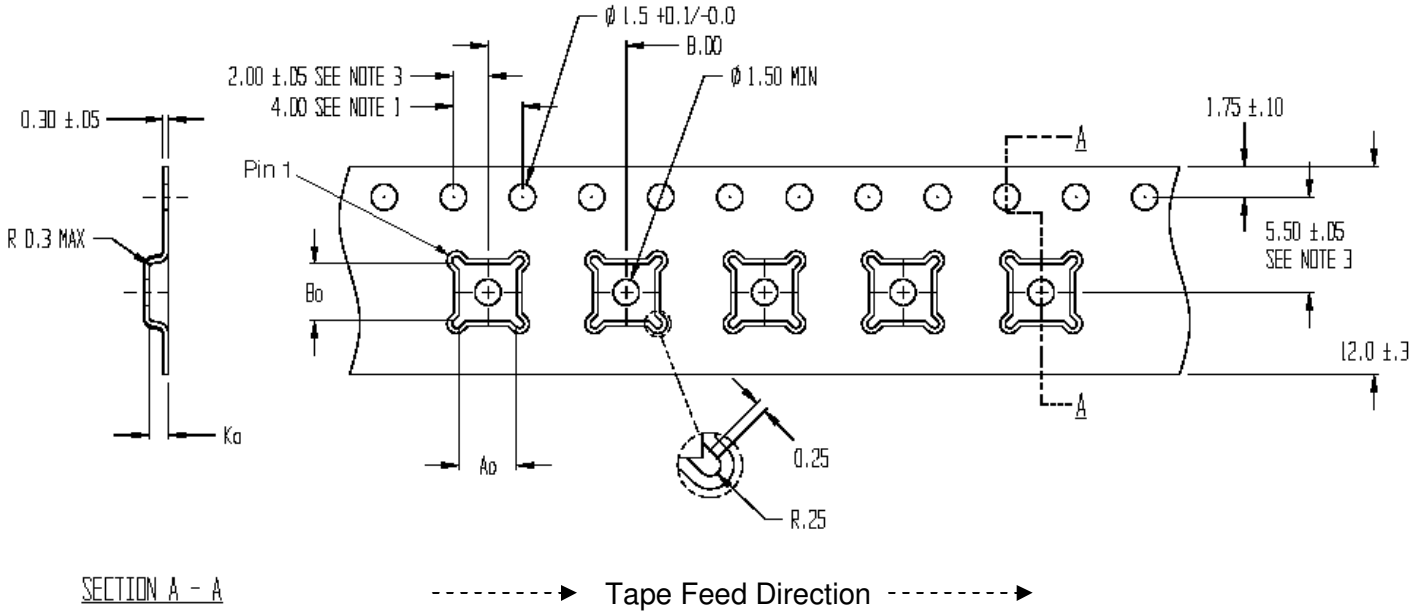


Table 6. Dimensions

Dimension	DFN 3x3 mm
Ao	3.23 ± 0.1
Bo	3.17 ± 0.1
Ko	1.37 ± 0.1
P	4 ± 0.1
W	8 +0.3, -0.1
T	0.254 ± 0.02
R7 Quantity	3000
R13 Quantity	N.A.

Note: R7 = 7 inch Lock Reel, R13 = 13 inch Lock Reel

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4140-51	4140	PE4140G-06DFN 3x3mm-Cut tape or loose	Green 6-lead 3x3 mm DFN	Cut tape or loose
4140-52	4140	PE4140G-06DFN 3x3mm-3000C	Green 6-lead 3x3 mm DFN	3000 units / T&R
4140-00	PE4140-EK	PE4140-06DFN 3x3mm-EK	Evaluation Kit	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

High-Reliability and Defense Products

Americas

San Diego, CA, USA
Phone: 858-731-9475
Fax: 848-731-9499

Europe/Asia-Pacific

Aix-En-Provence Cedex 3, France
Phone: +33-4-4239-3361
Fax: +33-4-4239-7227

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

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