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Data Sheet, DS2, April 2001

MUNICH256
Multichannel Network Interface Controller for HDLC/PPP
PEB 20256 E Version 2.1

Datacom

Infineon technologies

Never stop thinking.

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Revision History: **04.2001** DS2
Previous Version: Preliminary Data Sheet 11.1999
Major changes to document since last version

Page	Description
25	Pin Diagram added 16-Port mode
26	Pin Diagram added 28-Port mode
54	Remote payload loop block diagram redrawn
154	Swap the bit positions of TBRTC and TBFTC In the CSPEC_BUFFER register as their bit postitions were not correct in the preliminary data sheet.
155	Swap the postions of TBRTC with TBFTC in Table 8-7, as their column positions were not correct in the preliminary data sheet
159	Fixed typo in CSPEC_IMASK register, replaced ROFD with RFOD
190	Fixed typo in IQMASK, replaced ROFD with RFOD
203	Update voltage min/max information for **Table 9-1 Absolute Maximum Ratings**
205	Update timing Information for **Table 9-4 DC Characteristics (PCI Interface Pins)**
206	Update timing Information for **Table 9-5 PCI Clock Characteristics**
207	Update timing Information for **Table 9-6 PCI Interface Signal Characteristics**
210	Update timing Information for **Table 9-8 Intel Bus Interface Timing**
211	Intel Bus Interface Timing Diagram modified. The setup and hold times for “LD to LRDY” was not a valid timing parameter. Instead, the setup and hold parameters for “LD to LRD” were specified.
213	Update timing Information for **Table 9-9 Intel Bus Interface Timing (Master Mode)**
213	Timing parameter (setup time) 67a was changed from “LD to LDRY” to ”LD to LRD”, because it was not a valid timing parameter.
213	Timing parameter (hold time) 67b was changed from “LD to LDRY” to ”LD to LRD”, because it was not a valid timing parameter.
215	Update timing Information for **Table 9-10 Motorola Bus Interface Timing**
218	Update timing Information for **Table 9-11 Motorola Bus Interface Timing (Master Mode)**

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Preface

The Multichannel Network Interface Controller for HDLC/PPP is a Multichannel Protocol Controller for a wide area of telecommunication and data communication applications.

Organization of this Document

This Data Sheet is divided into ten chapters and is organized as follows:

- **Chapter 1 MUNICH256 Overview**

  Gives a general description of the product and its family, lists the key features, and presents some typical applications

  .

- **Chapter 2 Pin Description**

  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3 General Overview**

  This chapter provides short descriptions of all the internal functional blocks.

- **Chapter 4 Functional Description**

  Gives a detailed description of all functions

- **Chapter 5 Interface Description**

  This chapter provides functional diagrams of all interfaces.

- **Chapter 6 Channel Programming / Reprogramming Concept**

  This chapter provides a detailed description of the channel programming concept.

- **Chapter 7 Reset and Initialization procedure**

  Gives examples of the initialzation procedure and operation.

- **Chapter 8 Register Description**

  Gives a detailed description of all on-chip registers.

- **Chapter 9 Electrical Characteristics**

Gives a detailed description of all electrical DC and AC characteristics, and provides timing diagrams for all interfaces.

- **Chapter 10 Package Outline**.

  Shows the mechanical values of the device package.

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1 MUNICH256 Overview

The MUNICH256 is a highly integrated protocol controller that implements HDLC, PPP and transparent (TMA) protocol processing for 256 channels. An on-chip data management unit is optimized to transfer data packets via a PCI interface by minimizing the bus load.

The serial interface of the device can be configured in a 16-port mode and additionally in a 28-port mode. The 16-port mode provides a clock pin, a data pin and a frame synchronization pin for each port and direction. The 28-port mode provides a clock pin and a data pin per port and direction. In this mode frame boundaries are indicated by clock gaps. **Table 1-1** below shows the pin configuration and the supported frame structures in the 16-port mode and the 28-port mode.

Table 1-1 Interface Configuration

	Port mode	
	16-port mode	**28-port mode**
Supported Interfaces		
1.544 MBit/s channelized	x	x
2.048 MBit/s channelized	x	x
4.096 MBit/s channelized	x	
8.192 MBit/s channelized	x	
Unchannelized	x	x
Supported Pins		
Receive Data	x	x
Receive Clock	x	x
Receive Synchronization Pulse	x	
Transmit Clock	x	x
Transmit Data	x	x
Transmit Synchronization Pulse	x	
Frame Indication		
Gapped Clock		x
Synchronization Pulse	x	

1.1 General Features

- Configurable port interface which operates in 16-port mode or 28-port mode.
- In 16-port mode protocol processing on up to 16 T1, E1, channelized 4 MBit/s, channelized 8 MBit/s or unchannelized links for frame relay, router or DSLAM applications with a maximum aggregate data rate of up to 90 Mbit/s per direction at 66 MHz PCI frequency
- In 28-port mode protocol processing on up to 28 T1, E1 or unchannelized links. T1, E1 frame boundaries are indicated by clock gaps
- Support of 256 bidirectional channels, which can be assigned arbitrarily to a maximum of 16 links, for HDLC, PPP or transparent mode (TMA) processing
- Concatenation of any, not necessarily consecutive, time slots to logical channels on each physical link. Supports DS0, fractional T1/E1 or T1/E1 channels
- Additional support of unchannelized modes, with data rates of up to 45 Mbit/s on port zero and 8.192 Mbit/s on all other ports
- Provides 32kB data buffer in transmit direction and 12kB data buffer in receive direction
- Independently selectable pay load loops for each port
- Provides a test function which allows to switch one out of 16 (28) ports to a test port
- System interface is a PCI 32 bit, 66 MHz Rev. 2.1 compliant bus interface, which supports configuration of subsystem ID / subsystem vendor ID via a serial EEPROM interface
- Integrates a local microprocessor master and slave interface (demultiplexed 16 bit address and data bus in Intel mode or Motorola mode) which allows access to the local bus via the PCI bus or which can communicate with a PCI host processor through an on-chip mailbox
- JTAG boundary scan according to IEEE1149.1 (5 pins)
- 0.25 µm, 2.5V core technology
- I/Os are 3.3V tolerant and have 3.3V driving capability
- Package P-BGA 388 (35mm x 35mm, pitch 1.27mm)
- Full scan path and BIST of on-chip RAMs for production test
- Performance: 90 Mbit/s data throughput per direction at 66 MHz
- Estimated power consumption: 3W at 66 MHz
- Also available as device with extended temperature range -40..+85°C

1.2 Logic Symbol

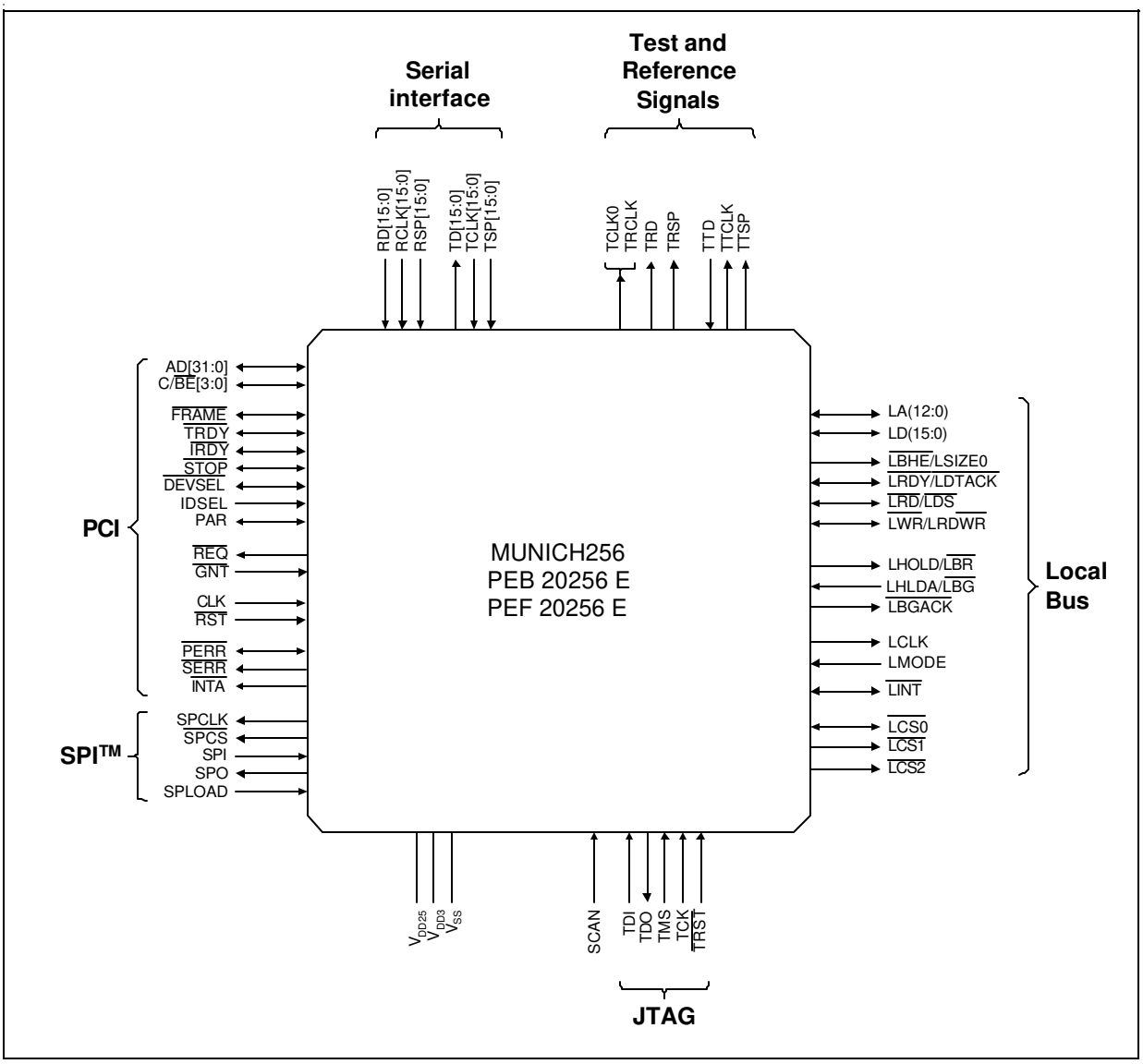

Figure 1-1 MUNICH256 16-port Mode Logic Symbol

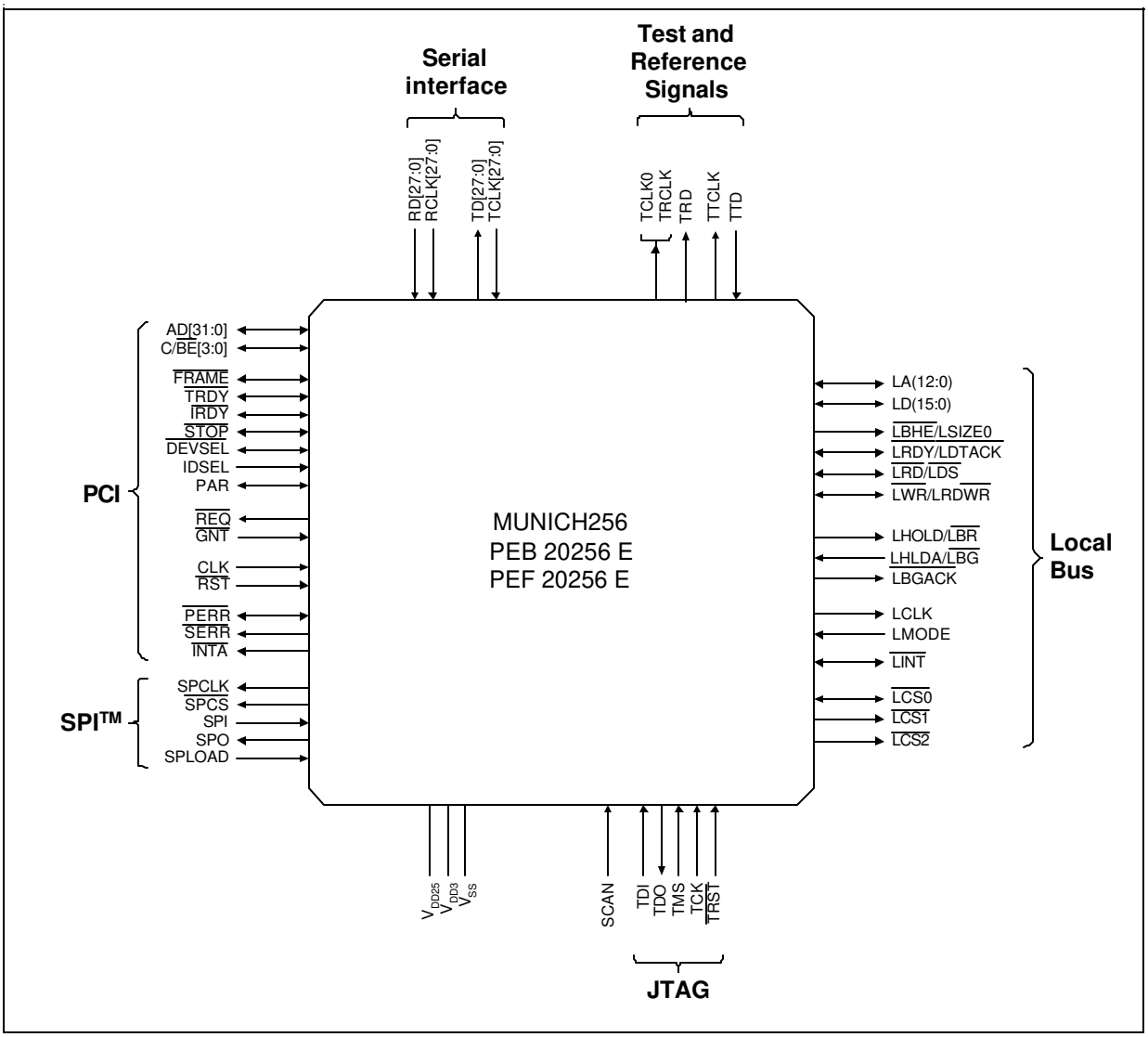

Figure 1-2 MUNICH256 28-port Mode Logic Symbol

1.3 General System Integration MUNICH256

The MUNICH256 provides the HDLC/PPP or transparent (TMA) protocol handling for channelized or unchannelized applications with up to 16 links. Protocol data is transferred to the packet RAM via the PCI bus and handled (e.g. for layer3 protocol handling) by a central CPU. An integrated mailbox allows to exchange information between a local CPU and the line card processor.

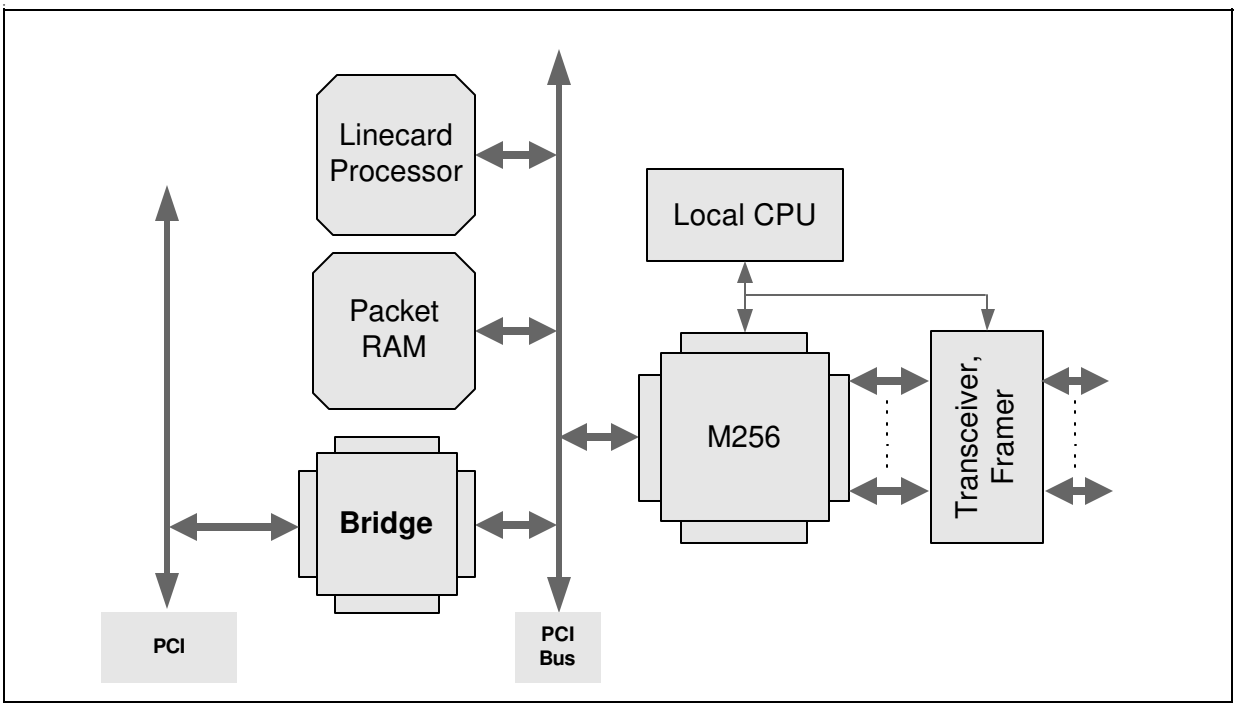

Figure 1-3 System Integration of the MUNICH256

2 Pin Description

2.1 Pin Diagram 16-Port Mode MUNICH256

(Top view)

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AF	VSS	LD(3)	NC22	LD(5)	VDD25	LD(11)	LD(13)	LA(1)	VSS	LA(4)	LA(8)	VDD25	LA(10)	LA(11)	VDD25	AD(0)	AD(5)	VSS	AD(6)	AD(9)	AD(12)	VDD25	PAR	STOP	NC24	VSS
AE	LD(2)	VDD25	LD(4)	NC23	NC20	LD(8)	VSS	LD(12)	LA(0)	VDD25	LA(5)	VSS	LA(9)	LA(12)	VSS	AD(2)	VDD25	C/BE(0)	AD(10)	VSS	AD(14)	SERR	DEVSEL	NC25	VDD25	NC28
AD	VSS	LD(1)	VSS	NC17	NC18	VDD3	LD(7)	LD(9)	VDD3	LD(14)	LD(2)	LA(6)	VDD3	LBHE/LSIZE0	AD(1)	AD(4)	AD(8)	VDD3	AD(13)	C/BE(1)	VDD3	TRDY	NC27	VSS	NC29	AD(17)
AC	LINT	LCS2	LRD/LDS	VDD3	NC16	NC19	NC21	LD(6)	LD(10)	VDD3	LD(15)	LA(3)	LA(7)	INTA	AD(3)	AD(7)	VDD3	AD(11)	AD(15)	PERR	IRDY	NC26	VDD3	NC31	AD(16)	AD(21)
AB	VDD25	LHLDA/LBG	LWR/LRD/WR	LD(0)																			NC30	FRAME	AD(20)	VDD25
AA	RD(1)	LHOLD/LBR	VDD3	LRDY																			C/BE(2)	VDD3	AD(23)	IDSEL
Y	VDD25	VSS	LCLK	LCS0																			AD(18)	AD(19)	VSS	VDD25
W	RD(2)	RCLK (1)	LMODE	LCS1																			AD(22)	VDD3	AD(25)	AD(26)
V	VSS	TCLK (14)	VDD3	LBGACK																			AD24	C/BE(3)	AD(27)	VSS
U	TCLK (13)	VDD25	RD(3)	VDD3																			VDD3	AD(28)	VDD25	AD(29)
T	TCLK (9)	TCLK (11)	RCLK (3)	RCLK (2)							VSS	VSS	VSS	VSS	VSS	VSS							AD(30)	AD(31)	REQ	GNT
R	VDD25	VSS	TCLK (12)	TCLK (15)							VSS	VSS	VSS	VSS	VSS	VSS							CLK	RST	VSS	VDD25
P	TCLK (7)	TCLK (8)	TCLK (10)	VDD3							VSS	VSS	VSS	VSS	VSS	VSS							SPLOAD	VDD3	SPI	SPO
N	TTCLK	TCLK (6)	VDD3	TCLK (5)							VSS	VSS	VSS	VSS	VSS	VSS							SPCLK	SPCS	RSP (15)	TSP (15)
M	VDD25	VSS	TRD	TD(14)							VSS	VSS	VSS	VSS	VSS	VSS							RSP (14)	TSP (14)	VSS	VDD25
L	TCLK (4)	TD(13)	VDD3	TD(11)							VSS	VSS	VSS	VSS	VSS	VSS							RSP (12)	TSP (12)	TSP (13)	RSP (13)
K	TD(15)	VDD25	RCLK (4)	VDD3																			RES14	RES15	VDD25	RES16
J	VSS	RD(4)	VDD3	RD(6)																			RES11	VDD3	RES13	VSS
H	TD(12)	RD(5)	RCLK (6)	VDD3																			RSP (11)	RES9	RES10	RES12
G	VDD25	VSS	RCLK (7)	RCLK (8)																			RSP (9)	RSP (10)	VSS	VDD25
F	RCLK (5)	RD(7)	VDD3	TMS																			TSP (8)	VDD3	TSP (10)	TSP (11)
E	VDD25	RD(9)	SCAN	NC12																			NC0	RES7	TSP(9)	VDD25
D	RD(8)	VSS	TDO	VDD3	NC15	NC9	TD(10)	TD(6)	RD(10)	VDD3	RCLK (13)	TD(0)	TCLK (1)	RCLK (14)	RES20	TSP(0)	VDD3	RSP (2)	RSP (4)	TSP(6)	RSP (7)	RES3	VDD3	NC7	RES8	RSP (8)
C	RCLK (9)	TCK	VSS	NC14	NC10	VDD3	TD(7)	TD(4)	VDD3	RD(12)	TD(2)	TCLKO / TRCLK	TCLK (2)	VDD3	TTD	RCLK (0)	TSP(1)	TSP(2)	TSP(4)	RSP (5)	VDD3	TTSP	RES6	VSS	NC3	NC1
B	TRST	VDD25	NC13	NC8	TD(9)	TD(5)	VSS	RCLK (10)	RCLK (11)	VDD25	TD(1)	VSS	TCLK (3)	RD(15)	VSS	RD(0)	VDD25	RSP (1)	RSP (3)	VSS	TSP(7)	TRSP	RES5	NC6	VDD25	NC2
A	VSS	NC11	TDI	TD(8)	VDD25	TD(3)	RD(11)	RCLK (12)	VSS	RD(13)	TCLK (0)	VDD25	RD(14)	RCLK (15)	VDD25	RES21	RSP (0)	VSS	TSP(3)	TSP(5)	RSP (6)	VDD25	RES4	NC4	NC5	VSS

Figure 2-1 MUNICH256 Pin Configuration 16-Port Mode