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ICs for Communications

ISDN High Voltage Power Controller
IHPC

PEB 2026 Version 1.1

Data Sheet 09.99

| PEB 2026 | | |
|----------------------------------|---------------------------------|--|
| Revision History: | | Current Version: 09.99 |
| Previous Version: | | preliminary Data Sheet 02.96 |
| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| | 3-2 | Information added about thermal protection and life time |
| | 3-3 | Information added about parasitic diodes |
| | 3-3 | Extra paragraph for subject " I_{BAT} current peak" |
| 16 | 7-1 | Some values for absolute maximum ratings are extended/adapted. |
| 17 | 7-4 | The static thermal resistances are updated. The last two paragraphs on this page, explaining the reason for the different packages are additional. |

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Edition 09.99

**Published by Infineon Technologies AG,
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Balanstraße 73,
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1 Overview

The IHPC is an integrated power controller especially designed for feeding two-wire ISDN-transmission lines. One line can be powered by one IHPC. An external resistor defines the value of the current-limit for the line. Powering can be switched on or off by the logic inputs "PFEN" and "PFENQ". With a logic low at the "APFI" output the IHPC signals that current-limiting is active; this signal is low-pass filtered. An external capacitor defines the corner frequency of this low-pass filter and the resulting delay time respectively. A second external capacitor is needed to make sure that longitudinal disturbances (AC) will not produce a current limiting effect. Line current-limiting and reducing this limiting level in case of overtemperature guards the IHPC against overloads.

ISDN High Voltage Power Controller IHPC

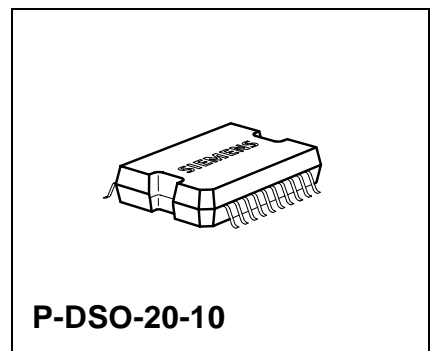
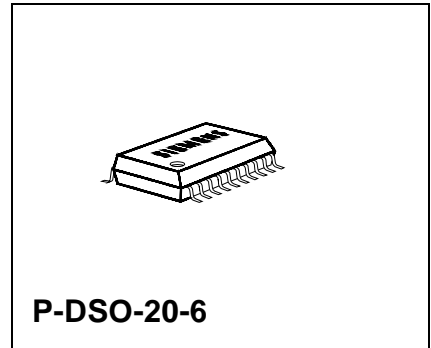
PEB 2026

Version 1.1

CMOS

1.1 Features

- Battery voltage up to 130 V
- Supplies power for one transmission line
- Current limiting and chip temperature control
- Limiting current can be programmed by an external resistor
- Automatically reduced feeding current in case of overtemperature
- Reliable 170 V Smart Power Technology (SPT 170)
- Small P-DSO-20 package



| Type | Package |
|----------|-------------|
| PEB 2026 | P-DSO-20-6 |
| | P-DSO-20-10 |

2 Pin Description

2.1 Pin Configuration

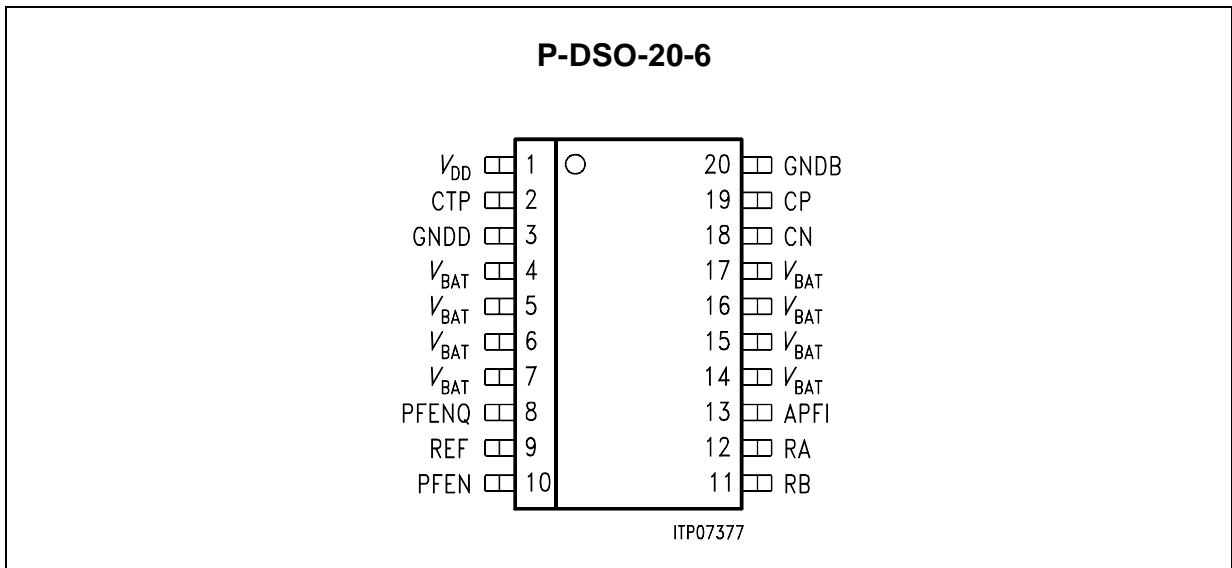


Figure 2-1 Pin Configuration P-DSO-20-6 (top view)

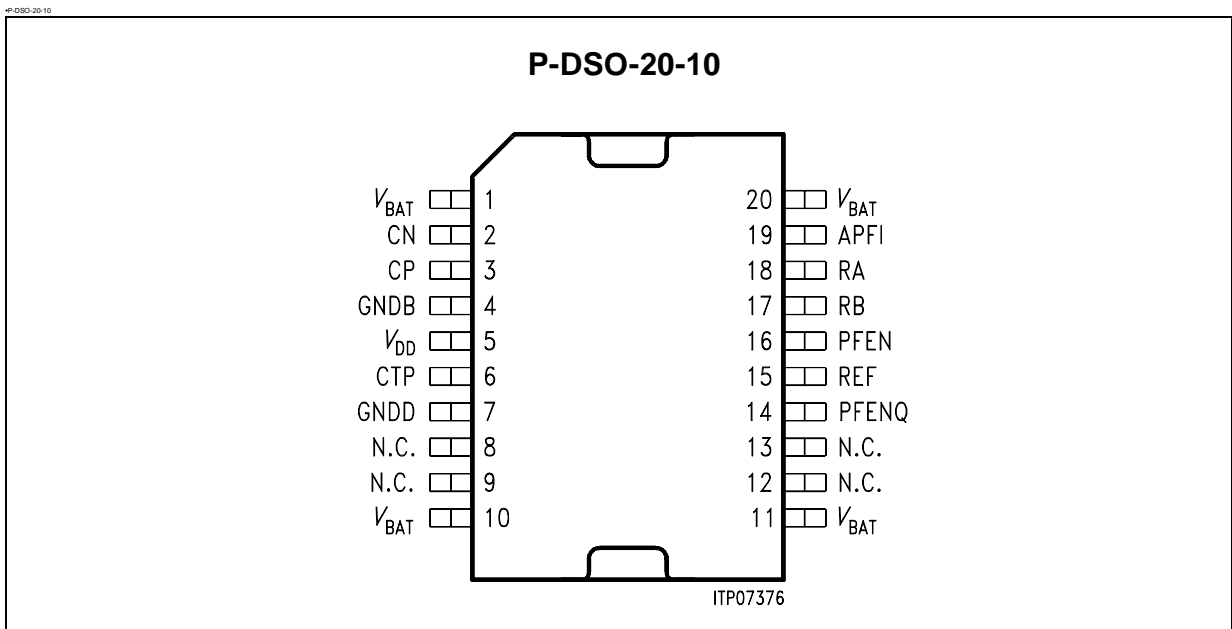


Figure 2-2 Pin Configuration P-DSO-20-10 (top view)

2.2 Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions P-DSO-20-6

| Pin | Symbol | Type | Description |
|---------------|-----------|--------|---|
| 4-7, 14-17 | V_{BAT} | Supply | Negative battery supply voltage (– 100 V), referred to GNDB |
| 20 | GNDB | Supply | Battery ground: RB and RA refer to this pin |
| 1 | V_{DD} | Supply | Positive supply voltage (+ 5 V), referred to GNDD |
| 3 | GNDD | Supply | Digital ground: V_{DD} , REF, CP, CN, CTP, PFEN, PFENQ and APFI refer to this pin |
| 9 | REF | O | Reference output, connected to GNDD via a resistor |
| 19 | CP | O | Positive pole of the external capacitor C_{HP} |
| 18 | CN | I | Negative pole of the external capacitor C_{HP} |
| 2 | CTP | O | Positive pole of the external capacitor C_{TP} |
| 11 | RB | O | Output for powering line b (tip), current sensing |
| 12 | RA | O | High voltage output for powering line a (ring), current limiting/switching |
| 10 | PFEN | I | Logic high on this pin switches on the current feeding |
| 8 | PFENQ | I | Logic low on this pin switches on the current feeding |
| 13 | APFI | O | Logic low on this pin signals active current-limiting |

Table 2-2 Pin Definitions and Functions P-DSO-20-10

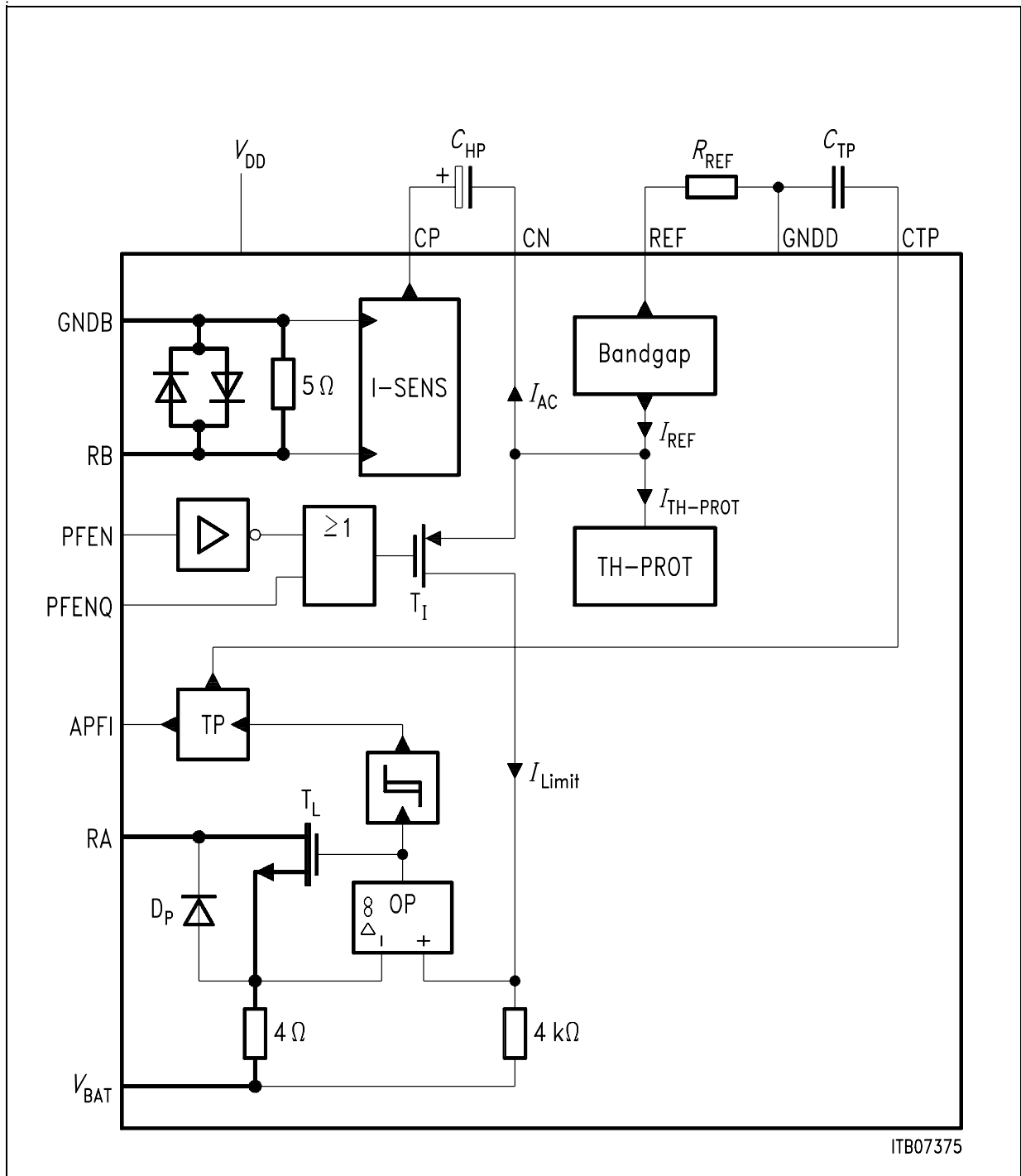
| Pin | Symbol | Type | Description |
|----------------|-----------|--------|---|
| 1,10, 11,20 | V_{BAT} | Supply | Negative battery supply voltage (– 100 V), referred to GNDB |
| 4 | GNDB | Supply | Battery ground: RB and RA refer to this pin |
| 5 | V_{DD} | Supply | Positive supply voltage (+ 5 V), referred to GNDD |
| 7 | GNDD | Supply | Digital ground: V_{DD} , REF, CP, CN, CTP, PFEN, PFENQ and APFI refer to this pin |
| 15 | REF | O | Reference output, connected to GNDD via a resistor |
| 3 | CP | O | Positive pole of the external capacitor C_{HP} |
| 2 | CN | I | Negative pole of the external capacitor C_{HP} |
| 6 | CTP | O | Positive pole of the external capacitor C_{TP} |
| 17 | RB | O | Output for powering line b (tip), current sensing |

Pin Description

Table 2-2 Pin Definitions and Functions P-DSO-20-10 (cont'd)

| Pin | Symbol | Type | Description |
|-----|--------|------|--|
| 18 | RA | O | High voltage output for powering line a (ring), current limiting/switching |
| 16 | PFEN | I | Logic high on this pin switches on the current feeding |
| 14 | PFENQ | I | Logic low on this pin switches on the current feeding |
| 19 | APFI | O | Logic low on this pin signals active current-limiting |

3 Functional Description



ITB07375

Figure 3-1 Block Diagram

The current flowing from **GNDB** to **RB** is measured. A down scaled image of this current is filtered by a high-pass filter with a corner frequency f_{CHP} of approximately 3 Hz (see

Functional Description

Figure 5-4). This filter needs the external capacitor C_{HP} . This “AC”-current is subtracted from the reference-current generated in the bandgap. The value of the reference-current is defined by the external resistor R_{REF} .

In case of overtemperature the thermal protection TH-PROT sinks a current, so that the current I_{Limit} is reduced. So in case of high power dissipation on chip the junction temperature is limited to about 165 °C.

This function is a protection against instant damages due to overload at the outputs. Continuous high temperatures during operation, however, will reduce the life time of the IHPC. A maximum junction temperature of 150°C shall not be exceeded (See section 7, "Electrical Characteristics")

Measures have to be taken to switch off the IHPC in case of a short-circuit. E.g. if pin APFI indicates active current-limiting, the IHPC should be deactivated after 1.5 sec using pin PFEN or PFENQ. A consecutive power-up attempt shall give enough time to the IHPC to cool down again (e.g. 30 sec).

The current I_{Limit} is reflected to the output current I_{Line} flowing from RA to V_{BAT} using the operational-amplifier OP, the transistor T_L and two resistors (4 Ω, 4 kΩ).

$$I_{Line,max}(t) = 1000 \times I_{Limit}(t) = 1000 \times (I_{REF} - I_{TH-PROT}(t) - I_{AC}(t))$$

In case of “no current-limiting” the output voltage of the operational-amplifier OP is equal to the positive OP-supply voltage. The transistor T_L is “switched on”.

If the output current I_{Line} rises to $I_{Line,max}$ the current-mirror becomes active and keeps the output current at this level.

The voltage level at the gate of transistor T_L shows the state of the current-limiter (current-limiting active or not). This state-signal is filtered by a low-pass filter and generates the logic output APFI. The external capacitor C_{TP} of this low-pass filter defines the corner frequency and the resulting delay times t_{LIMON} (Spec.-No.: 17) and t_{LIMOFF} (Spec.-No.: 18) respectively.

Summarized, the current sensor I-SENS and the high-pass filter prevent, that a longitudinal disturbance in the frequency range from about ($5 \cdot f_{CHP}$) to about 100kHz result in a current limitation. This applies if the maximum amplitude of the longitudinal current is lower than about half of the current limit (Spec.-No.: 3) defined by the external resistor R_{REF} , see also Spec.-No.: 15 and 16.

There is also another effect from the current sensing and high-pass filtering, which can be seen when changing from status LIMOFF to LIMON. This can occur by switching power on to the line (loading the line capacitor) or in case of short-circuiting the line. The resulting current transient starts at half of $I_{Line,max}$ and increases (capacitor loading function) to $I_{Line,max}$ with a time constant t_{CHP} also defined by the value of C_{HP} .

Functional Description

The diodes connected to GNDB and RB protect the IHPC against lightning and overvoltages (**see Absolute Maximum Ratings**). The diode D_p is the parasitic bulk-drain-diode of the DMOS-transistor T_L .

Because of technology reasons („p“-substrate, junction isolation) there are also parasitic diodes from pin V_{BAT} to all other pins.

 I_{BAT} current peak:

When line feeding is switched on (transistor T_L is on) and a short circuit occurs between pins RA and GNDB (or GNDD) then it needs a certain time to unload the gate-source-capacitance of T_L and to limit the current to the defined maximum value. In the meantime a current peak I_{BAT} on the supply voltage V_{BAT} can be seen.

An overvoltage protection circuit for pin RA, for example can produce such a short circuit between pins RA and GNDB.

In the IHPC a fast bipolar npn-transistor limits such current peaks. With $V_{BAT} = 100\text{ V}$, the resulting I_{BAT} current transient has the profile of one triangular pulse with a peak value of about 1.5A and a time duration (50% to 50%) of about 130nsec.

4 Operating Modes

| Operating Mode | Status | PFEN | PFENQ | APFI |
|-------------------|------------------------------|--------------------|--------------------|--------------------|
| OFF, powering off | | "V _{IL} " | Don't care | "V _{OL} " |
| OFF, powering off | | Don't care | "V _{IH} " | "V _{OL} " |
| ON, powering on | LIMON, limiter is active | "V _{IH} " | "V _{IL} " | "V _{OL} " |
| ON, powering on | LIMOFF, limiter isn't active | "V _{IH} " | "V _{IL} " | "V _{OH} " |

The logic input pins PFEN and PFENQ are connected to GNDD by integrated current sources. If these pins are not connected externally the logic level is "V_{IL}".

5 Designing the External Components

Resistor R_{REF} :

The value of this resistor defines the current limit $I_{Limit,ON}$ (Spec.-No.: 3) and it will also effect power supply currents I_{BAT} (Spec.-No.: 2) and I_{DD} (Spec.-No.: 1). For typical values of $I_{Limit,ON}$, I_{BAT} and I_{DD} as a function of R_{REF} see the following diagrams.

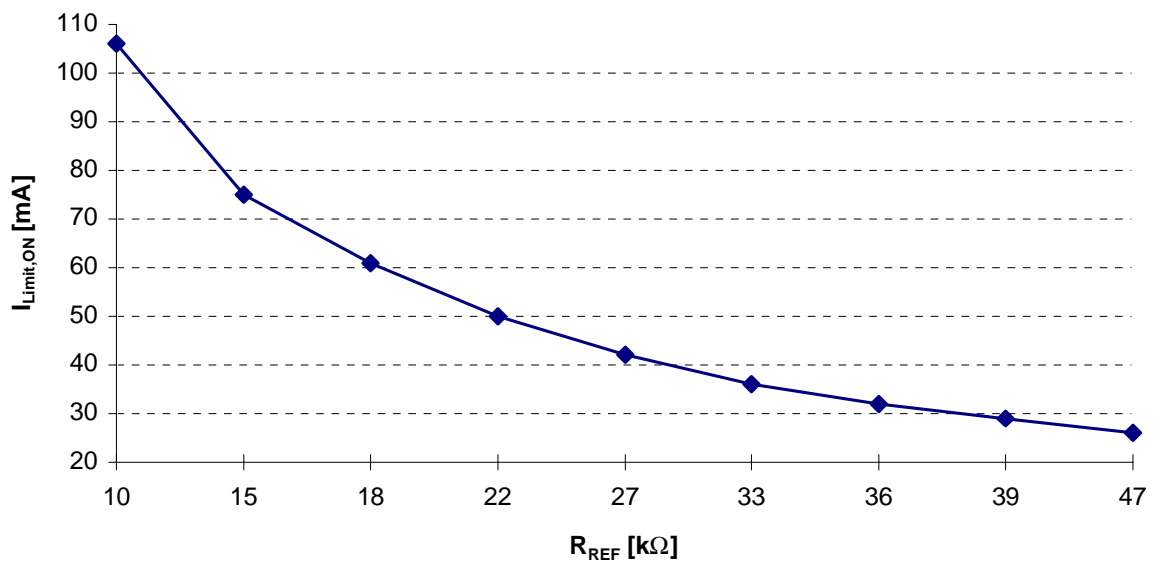


Figure 5-1 Current limit $I_{Limit,ON}$ as a function of R_{REF} (typical values)

Designing the External Components

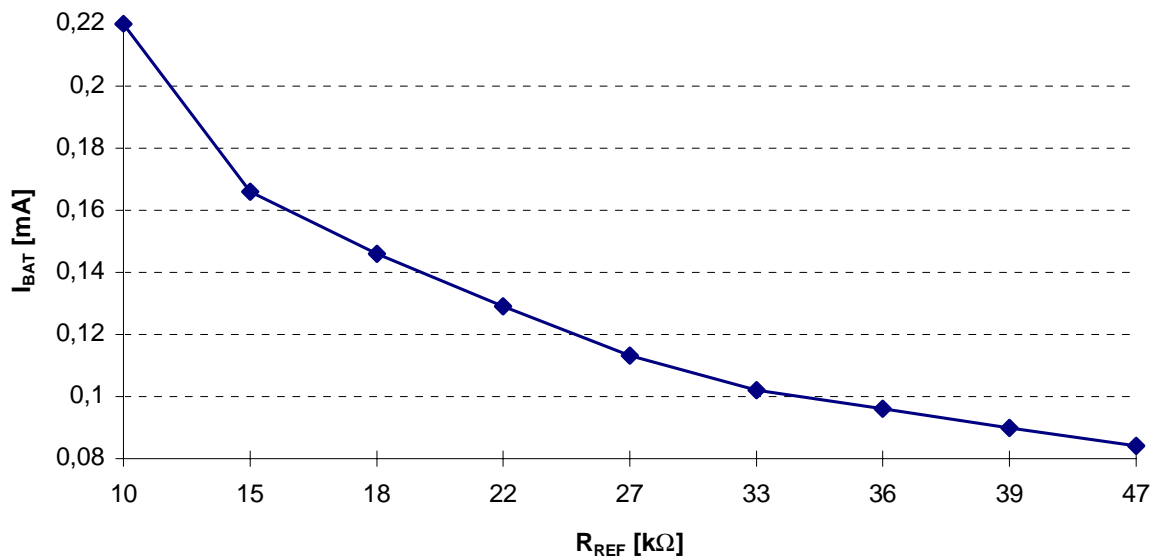


Figure 5-2 Power Supply Current I_{BAT} as a function of R_{REF} (typical values)

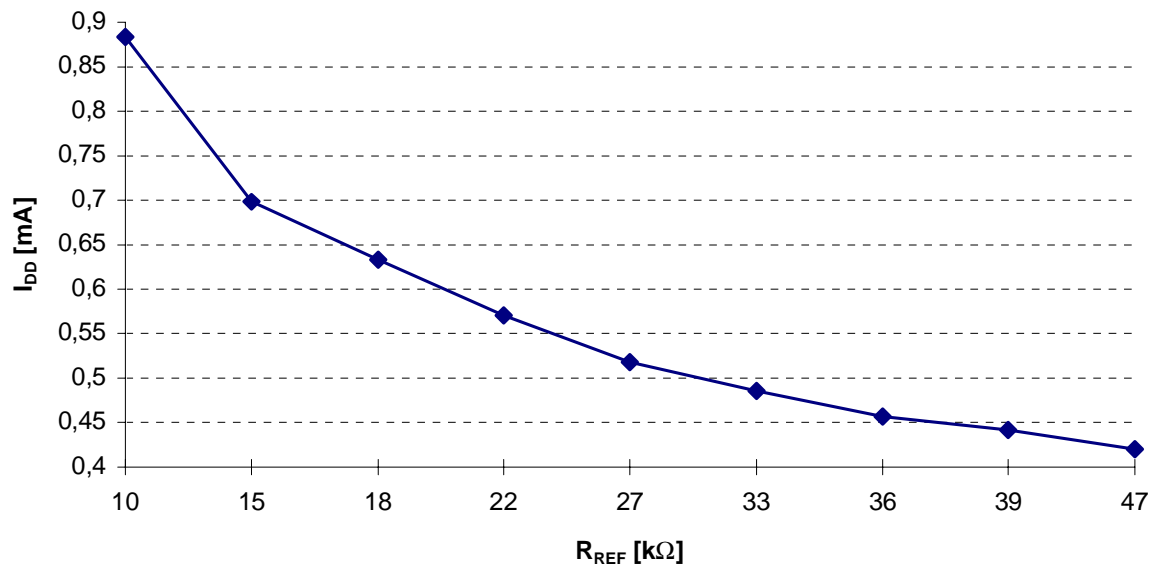


Figure 5-3 Power Supply Current I_{DD} as a function of R_{REF} (typical values)

Capacitor C_{HP} :

The value of this capacitor defines the corner frequency f_{CHP} of the high-pass filter and the time constant t_{CHP} of the current transient described at the last but one paragraph of chapter 2. The following diagrams show typical values of f_{CHP} and t_{CHP} as a function of C_{HP} .

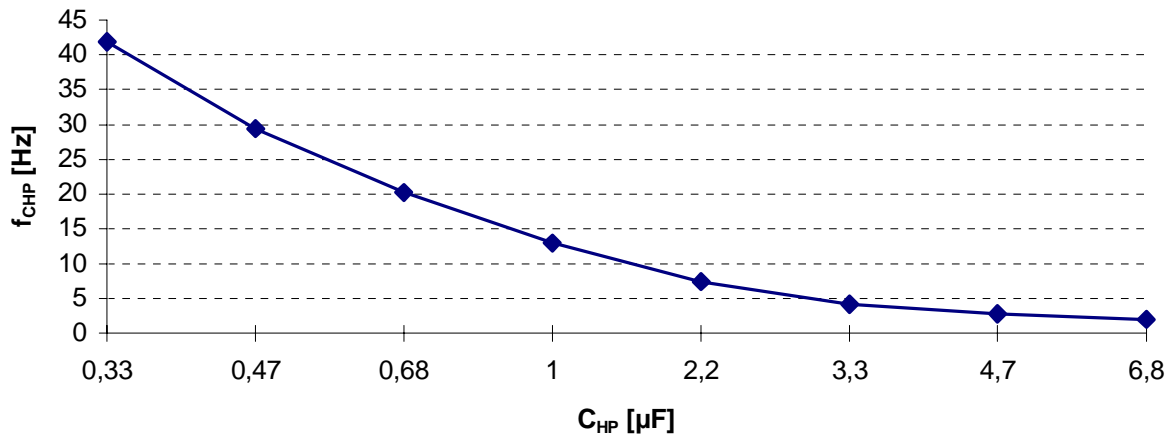


Figure 5-4 Corner frequency of high-pass filter as a function of C_{HP} (typical values)

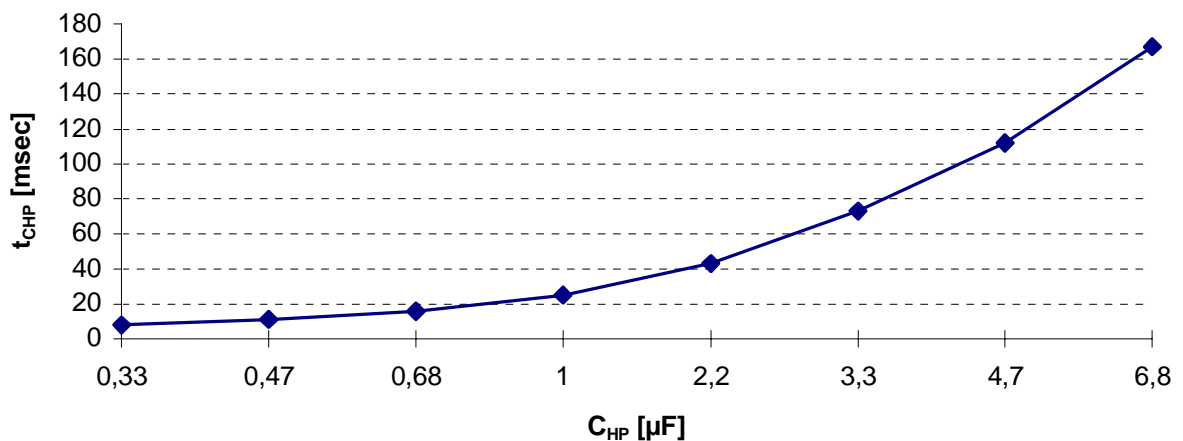


Figure 5-5 Time constant of high-pass filter as a function of C_{HP} (typical values)

Capacitor C_{TP} :

The value of this capacitor defines the corner frequency and the resulting delay times t_{LIMON} (Spec.-No.: 17) and t_{LIMOFF} (Spec.-No.: 18), of the low-pass filter. For typical values of t_{LIMON} and t_{LIMOFF} as a function of C_{TP} see the following diagrams.

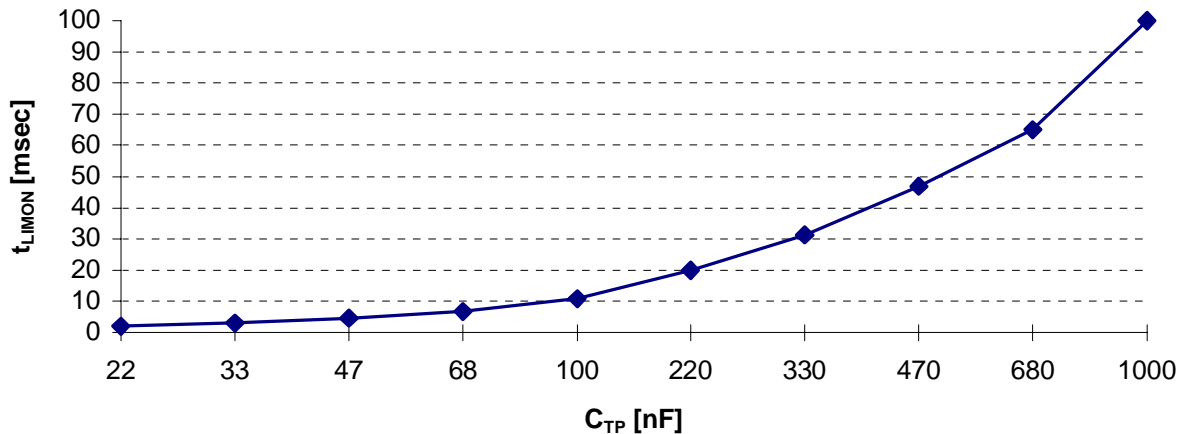


Figure 5-6 Delay time of the low-pass filter for the status output signal (typical values)

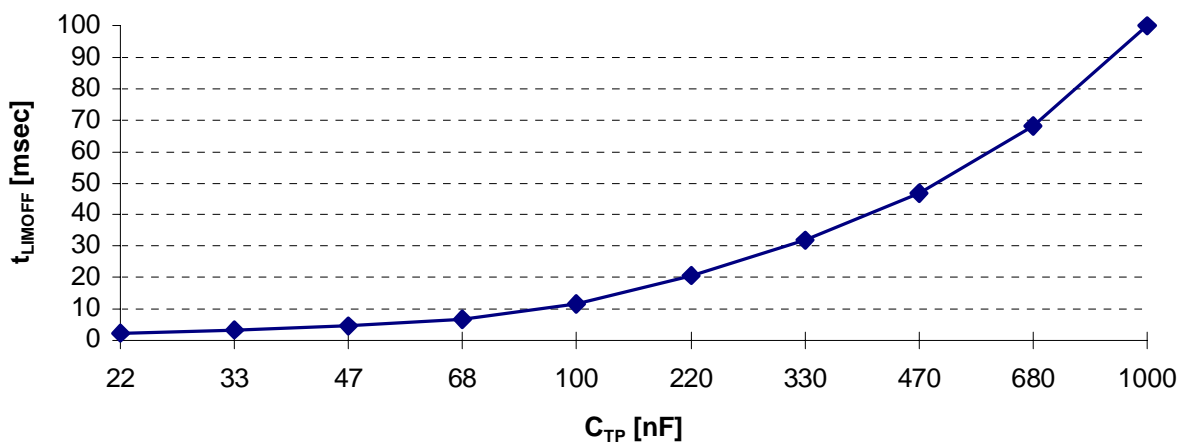


Figure 5-7 Delay time of the low-pass filter for the status output signal (typical values)

6 Application Note

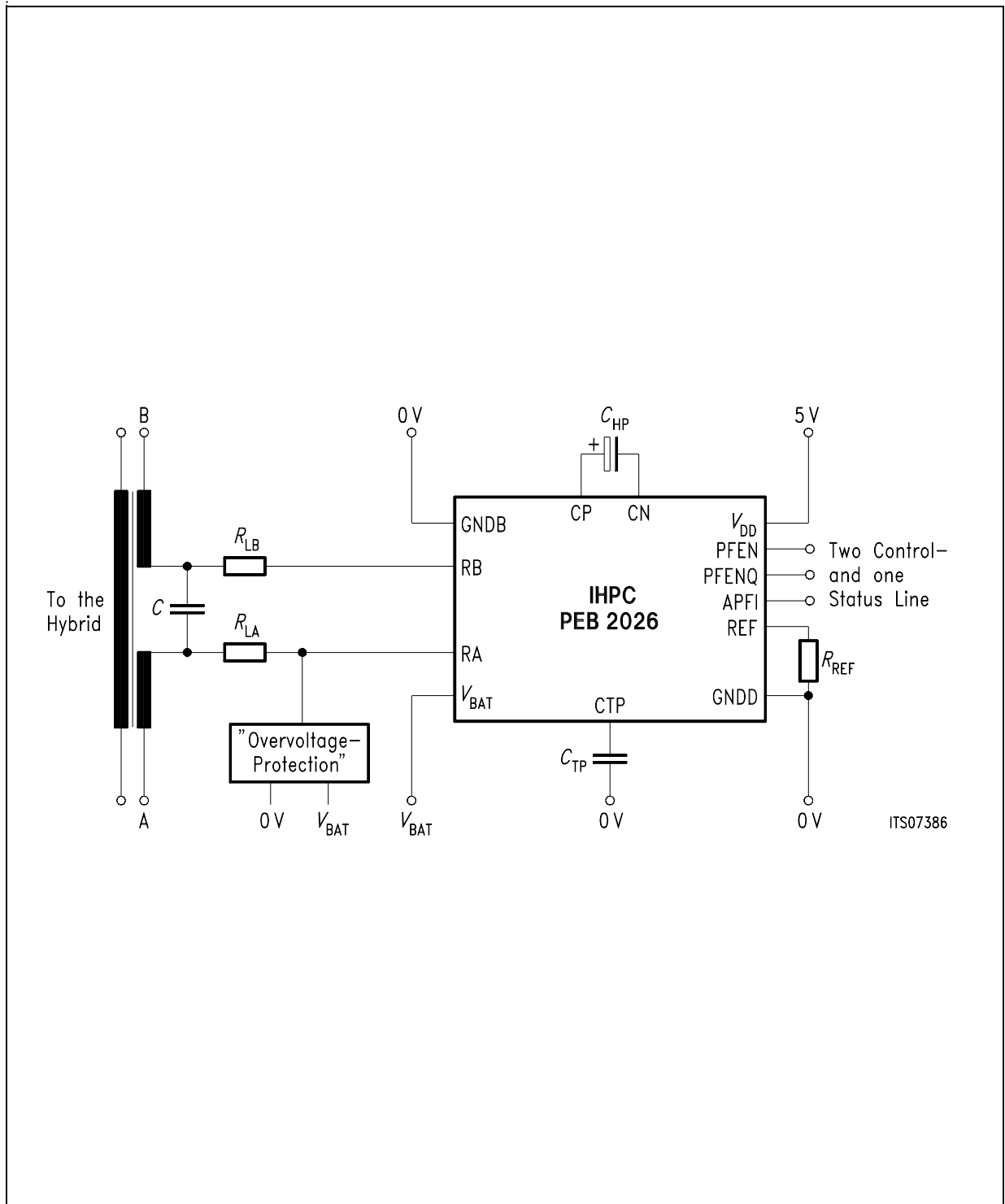


Figure 6-1 Application Circuit

Application Note

| | |
|------------------------|--|
| R_{REF} | Defines the current-limit and the internal biasing currents. A smaller/bigger value increases/decreases the current limit. It will also effect power supply currents. |
| C_{TP} | Defines with an internal resistor the delay time (a typical value is 20 msec) from the low pass filter, whose output signal is called 'APFI'. Short disturbances will therefore be filtered. A smaller/bigger value decreases/increases the delay time. |
| C_{HP} | Defines with an internal resistor the corner frequency from a high pass filter. It is used to make sure that longitudinal disturbances (AC) will not produce a current limiting effect. A smaller/bigger value decreases/increases the corner frequency. |
| R_{LA}, R_{LB} | These resistors limit the peak currents during lightning transients. The maximum value for these resistors is defined by the allowed voltage drop on the resistors. |
| C | The AC-signal-current will be shunted by this capacitor. |
| A, B | A- and B-line to the subscriber |
| V_{BAT} | The most negative supply voltage; also called battery voltage. |
| overvoltage protection | This circuit makes sure that the voltage from R_A to V_{BAT} will not exceed the defined limits in case of lightning (see Absolute Maximum Ratings). |

Recommended Device Values:

| | |
|------------------|---|
| R_{REF} | 22 k Ω , Current limiting is set to 50 mA |
| C_{TP} | 220 nF, 'APFI' delay time is set to 20 msec |
| C_{HP} | 4.7 μ F, AC longitudinal disturbances in a frequency range higher than 16.666 Hz do not effect a current limiting. |
| R_{LA}, R_{LB} | 23 Ω , Minimum value, so that peek currents don't exceed 16 A (using voltage peek = 1 kV from 40 Ω source resistance) in case of lightning. |

7 Electrical Characteristics

Table 7-1 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--------------------------------------|------------------------|--------------|----------------|------|---|
| | | min. | max. | | |
| Battery voltage | V_{BAT} | - 150 | 0.5 | V | Referred to GNDB |
| V_{DD} supply voltage | V_{DD} | - 0.5 | 6 | V | Referred to GNDD |
| Ground voltage difference | $V_{GNDB} - V_{GNDD}$ | - 0.5 | 0.5 | V | |
| Ground pulse voltage difference | $V_{GNDB} - V_{GNDD}$ | - 1 | 1 | V | $t_{max} = 1$ msec |
| Junction temperature | T_j | | 150 | °C | |
| Voltages on logic inputs PFEN, PFENQ | V_{PFEN}, V_{PFENQ} | - 0.3 | $V_{DD} + 0.3$ | V | Referred to GNDD |
| Voltages on REF | V_{REF} | - 0.3 | $V_{DD} + 0.3$ | V | Referred to GNDD |
| Voltages on CP | V_{CP} | - 0.3 | $V_{DD} + 0.3$ | V | Referred to GNDD |
| Voltages on CN | V_{CN} | - 0.3 | $V_{DD} + 0.3$ | V | Referred to GNDD |
| Voltages on CTP | V_{CTP} | - 0.3 | $V_{DD} + 0.3$ | V | Referred to GNDD |
| Voltages on logic output APFI | V_{APFI} | - 0.3 | $V_{DD} + 0.3$ | V | Referred to GNDD |
| RB voltage | V_{RB} | - 0.5 | + 0.5 | V | Referred to GNDB |
| RB pulse current | I_{RB} (into pin RB) | - 8 | 8 | A | $t_{max} = 1$ msec |
| RB peak current | I_{RB_peak} | - 16 | 16 | A | See figure 7-7 |
| RA voltages | V_{RA} | - 0.3 | 150 | V | Referred to V_{BAT} |
| RA pulse current | I_{RA} (into pin RA) | - 1 | 1 | A | $t_{max} = 1$ msec |
| RA pulse voltage | V_{RA_pulse} | - 1 | 170 | V | $t_{max} = 1$ msec, Referred to V_{BAT} |
| ESD-voltage, all pins | | | 1 | kV | Human body model |

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Electrical Characteristics
Table 7-2 Operating Range

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---------------------------|-----------------------|--------------|------|------|------------------|
| | | min. | max. | | |
| Battery voltage | V_{BAT} | - 130 | - 30 | V | Referred to GNDB |
| V_{DD} supply voltage | V_{DD} | 4.75 | 5.25 | V | Referred to GNDD |
| Ground voltage difference | $V_{GNDB} - V_{GNDD}$ | - 0.3 | 0.3 | V | |
| Ambient temperature | | | | | |
| PEB 2026 | T_A | 0 | +70 | °C | |
| PEF 2026 | T_A | -40 | +85 | °C | |

Static Thermal Resistance

| | | | | | |
|---------------------|-----------------|--|----|-----|-------------|
| Junction to ambient | $R_{th, jA}$ | | 55 | K/W | P-DSO-20-10 |
| Junction to case | $R_{th, jC}$ | | 4 | K/W | P-DSO-20-10 |
| Junction to ambient | $R_{th, jA}$ | | 65 | K/W | P-DSO-20-6 |
| Junction to pins | $R_{th, jPins}$ | | 15 | K/W | P-DSO-20-6 |

Note: In the operating range the functions given in the circuit description are fulfilled.

The power package P-DSO-20-10 has an exposed copper-heatspreader with a high thermal capacitance. For power feeding to ISDN-lines which are in a fault condition (e.g. short circuit) the maximum power dissipation on chip will become V_{BAT} supply voltage times limiting current (e.g.: 100V * 50mA = 5W). It is necessary to try to feed the line for about 2 seconds under this condition (5W), then the feeding can be switched off but must be switched on again about 30 seconds later. In this application the thermal capacitance of the cooper-heatspreader helps to keep the maximum chip temperature below the thermal protection temperature level (165°C). No extra heatsink is necessary.

The small P-DSO-20-6 package is applicable if the device is mounted on a pcb having at least 900 mm² copper area close to the device. The pcb serves as heat sink, heat flowing off through the pins, particularly the Vbat pins. With a mounting like this, the IHPC performs as follows: a current of 50 mA is supplied for 5 sec, while the device is shorted to Vbat=100V. At an ambient temperature of 70°C the current pulse may be periodically repeated with a period of 32 sec.

Electrical Characteristics

Electrical Parameters

Typical values are defined at the following test conditions:

$$V_{DD}=5V \pm 1 \% C_{HP}=4.7\mu F \pm 10 \% (6.3 V)$$

$$V_{BAT}=-100V \pm 1 \% C_{TP}=220nF \pm 10 \% (6.3 V)$$

$$R_{LA}=23\Omega \pm 1 \% T_A=25 \pm 5 \text{ }^\circ\text{C}$$

$$R_{LB}=23\Omega \pm 1 \% R_{Line}=\pm 0.1 \%$$

$$R_{REF}=22k\Omega \pm 1 \% \text{no heatsink}$$

Min. and max. values are in force within the whole operating range.

Table 7-3 Power-Supply

| No. | Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Fig. | Mode |
|-----|-----------|--------|--------------|------|------|------|----------------|-----------|------|
| | | | min. | typ. | max. | | | | |

Supply Currents ($I_{RB} = I_{RA} = 0$)

| | | | | | | | | | |
|---|-------------------|-----------|--|------|------|----|--|-----|-----|
| 1 | V_{DD} current | I_{DD} | | 0.57 | 0.9 | mA | | 7-1 | all |
| 2 | V_{BAT} current | I_{BAT} | | 0.13 | 0.25 | mA | | 7-1 | all |

Table 7-4 DC-Characteristics

| No. | Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Fig. | Mode |
|-----|-----------|--------|--------------|------|------|------|----------------|-----------|------|
| | | | min. | typ. | max. | | | | |

Maximal Line Currents

| | | | | | | | | | |
|---|--------------|----------------|----|----|----|---------|--|-----|------------------------------|
| 3 | Line current | $I_{limit,ON}$ | 45 | 50 | 55 | mA | | 7-2 | ON, Sta- tus: LIMON |
| 4 | Line current | $I_{max,OFF}$ | | 0 | 10 | μ A | | 7-2 | OFF |

Logic Input Levels on PFEN and PFENQ

| | | | | | | | | | |
|---|-----------------|-----------|---|----|-----|---------|----------------------------------|--|-----|
| 5 | H-input voltage | V_{IH} | 2 | | | V | | | all |
| 6 | L-input voltage | V_{IL} | | | 0.8 | V | | | all |
| 7 | Input current | I_{inp} | 2 | 11 | 20 | μ A | $0.8 V \leq V_{inp} \leq V_{DD}$ | | all |

Electrical Characteristics

Table 7-4 DC-Characteristics (cont'd)

| No. | Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Fig. | Mode |
|-----|-----------|--------|--------------|------|------|------|----------------|-----------|------|
| | | | min. | typ. | max. | | | | |

Logic Output Levels on APFI

| | | | | | | | | | |
|---|------------------|----------|----------------|--|-----|---|--------------------------|--|---------|
| 8 | H-output voltage | V_{OH} | $V_{DD} - 0.4$ | | | V | $I_{Source} = 100 \mu A$ | | ON |
| 9 | L-output voltage | V_{OL} | | | 0.4 | V | $I_{Sink} = 100 \mu A$ | | ON, OFF |

Resistance from GNDB to R_B

| | | | | | | | | | |
|----|---------------|----------|---|---|---|----------|--|-----|---------|
| 10 | R: GNDB to RB | R_{RB} | 3 | 5 | 7 | Ω | $I_{RB} = 30 \text{ mA}$ $\pm 5 \%$ | 7-3 | ON, OFF |
|----|---------------|----------|---|---|---|----------|--|-----|---------|

ON-resistance from R_A to V_{BAT}

| | | | | | | | | | |
|----|--|----------|------|---|------|----------|--|-----|--------------------|
| 11 | ON-R: RA to V_{BAT} ($T_L - R_{on}$ included) | R_{RA} | 2.65 | 5 | 7.35 | Ω | $I_{RA} = 30 \text{ mA}$ $\pm 5 \%$ | 7-3 | ON, Status: LIMOFF |
|----|--|----------|------|---|------|----------|--|-----|--------------------|

Difference-resistance between R_{RA} and R_{RB}

| | | | | | | | | | |
|----|---|------------|-------|---|------|----------|--|--|--------------------|
| 12 | $R_{RA} - R_{RB}$ PEB 2026 PEF 2026 | R_{DIFF} | -0.35 | 0 | 0.35 | Ω | | | ON, Status: LIMOFF |
| | | | -0.40 | 0 | 0.40 | Ω | | | |

Table 7-5 Indication of Current Limit

| No. | Parameter | Symbol | Mode | Test Condition | Status | Test Fig. |
|-----|-----------|--------|------|----------------|--------|-----------|
|-----|-----------|--------|------|----------------|--------|-----------|

Indication of Current Limit

| | | | | | | |
|----|-------------|--------------|----|--------------------------|-------------------------|-----|
| 13 | Line Status | S_{LIMON} | ON | $R_{Line} = 1762 \Omega$ | LIMON, APFI = V_{OL} | 7-4 |
| 14 | Line Status | S_{LIMOFF} | ON | $R_{Line} = 2166 \Omega$ | LIMOFF, APFI = V_{OH} | 7-4 |

Table 7-5 Indication of Current Limit (cont'd)

| No. | Parameter | Symbol | Mode | Test Condition | Status | Test Fig. |
|-----|-----------|--------|------|----------------|--------|-----------|
|-----|-----------|--------|------|----------------|--------|-----------|

Indication of Current Limit under Superimposed Longitudinal Current

| | | | | | | |
|----|-------------|---------------|----|--------------------------|----------------------------|-----|
| 15 | Line Status | S_{LLIMON} | ON | $R_{Line} = 1482 \Omega$ | LIMON, APFI = V_{OL} | 7-5 |
| 16 | Line Status | $S_{LLIMOFF}$ | ON | $R_{Line} = 2801 \Omega$ | LIMOFF, APFI = V_{OH} | 7-5 |

Calculation and Values of R_{Line}

$$R_{Line} = \frac{V_{BAT}}{I_{Line}} - R_{RA} - R_{RB} - R_{LA} - R_{LB} = \frac{100V}{I_{Line}} - 5 \Omega - 5 \Omega - 23 \Omega - 23 \Omega$$

where:

R_{LA} , R_{LB} ... referred to page 7-3, electrical parameters

R_{RA} , R_{RB} ... referred to Spec.-No.: 10 and 11

| I_{Line} | R_{Line} |
|------------|---------------|
| 35 mA | 2801 Ω |
| 45 mA | 2166 Ω |
| 55 mA | 1762 Ω |
| 65 mA | 1482 Ω |

Note: In some of these cases the IHPC will limit the line current to lower values.