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Data Sheet, DS 1, Sep. 2000

SEROCCO-M

2 Channel Serial Optimized Communication Controller

PEB 20532 Version 1.2
PEF 20532 Version 1.2

Datacom

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Never stop thinking.

Edition 2000-09-14

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Revision History:	**2000-09-14**	DS 1
Previous Version:	SEROCCO V1.1 Preliminary Data Sheet, 08.99, DS1	
Page (previous Version)	Page (current Version)	Subjects (major changes since last revision)
32-34	35-37	Correction: signal 'OSR' is multiplexed with signal 'CD', signal 'OST' is multiplexed with '$\overline{\text{CTS}}$' (was vice versa)
80	83	corrected HDLC receive address recognition table
214, 222	218, 226	Corrected location of TCD interrupt (async/bisync modes only) in registers ISR0 and IMR0 from bit 7 to bit 2.
n.a.	263, 266	Added timing diagram for external DMA support signals
n.a.	263	Added address timing diagram for Intel multiplexed mode (signal ALE)
253	257	Chapter "Electrical Characteristics" updated with final characterization results.

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Preface

The 2 Channel Serial Optimized Communication Controller PEB 20532 (SEROCCO-M) is a Protocol Controller for a wide range of data communication and telecommunication applications. This document provides complete reference information on hardware and software related issues as well as on general operation.

Organization of this Document

This Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1, Introduction**
  Gives a general description of the product, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Functional Overview**
  This chapter provides detailed descriptions of all SEROCCO-M internal functional blocks.

- **Chapter 4, Detailed Protocol Description**
  Gives a detailed description of all protocols supported by the serial communication controllers SCCs.

- **Chapter 5, Register Description**
  Gives a detailed description of all SEROCCO-M on chip registers.

- **Chapter 6, Programming**
  Provides programming help for SEROCCO-M initialization procedure and operation.

- **Chapter 7, Electrical Characteristics**
  Gives a detailed description of all electrical DC and AC characteristics and provides timing diagrams and values for all interfaces.

- **Chapter 8, Test Modes**
  Gives a detailed description of the JTAG boundary scan unit.

- **Chapter 9, Package Outlines**

Your Comments

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sc.docu_comments@infineon.com

Please provide in the *subject* of your e-mail:
device name (SEROCCO-M), device number (PEB 20532, PEF 20532), device version (Version 1.2),

and in the *body* of your e-mail:
document type (Data Sheet), issue date (2000-09-14) and document revision number (DS 1).

1 Introduction

The SEROCCO-M is a Serial Communication Controller with two independent serial channels[1]. The serial channels are derived from updated protocol logic of the ESCC and DSCC4 device family providing a large set of protocol support and variety in serial interface configuration. This allows easy integration to different environments and applications.

A generic 8- or 16-bit multiplexed/demultiplexed slave interface provides fast device access with low bus utilization and easy software handshaking. DMA handshake control signals allow connection to an external DMA controller.

Large on-chip FIFOs of 64 byte capacity per port and direction in combination with enhanced threshold control mechanisms allow decoupling of traffic requirements on host bus and serial interfaces with little exception probabilities such as data underruns or overflows.

Each of the two Serial Communication Controllers (SCC) contains an independent Baud Rate Generator, DPLL and programmable protocol processing (HDLC, PPP, ASYNC and BISYNC). Data rates of up to 16 Mbit/s (HDLC, PPP, bit transparent) and 2 Mbit/s (DPLL assisted modes) are supported. The channels can also handle a large set of layer-2 protocol functions (LAPD, SS7) reducing bus and host CPU load. Two channel specific timers are provided to support protocol functions.

[1] The serial channels are also called 'ports' or 'cores' depending on the context.

2 Channel Serial Optimized Communication Controller SEROCCO-M

PEB 20532
PEF 20532

Version 1.2 **CMOS**

1.1 Features

P-TQFP-100-3

Serial communication controllers (SCCs)

- Two independent channels
- Full duplex data rates on each channel of up to 16 Mbit/s sync - 2 Mbit/s with DPLL
- 64 Bytes deep receive FIFO per SCC
- 64 Bytes deep transmit FIFO per SCC

Serial Interface

- On-chip clock generation or external clock sources
- On-chip DPLLs for clock recovery
- Baud rate generator
- Clock gating signals
- Clock gapping capability
- Programmable time-slot capability for connection to TDM interfaces (e.g. T1, E1)
- NRZ, NRZI, FM and Manchester data encoding
- Optional data flow control using modem control lines ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, CD)
- Support of bus configuration by collision detection and resolution

Bit Processor Functions

- HDLC/SDLC Protocol Modes
  - Automatic flag detection and transmission
  - Shared opening and closing flag
  - Generation of interframe-time fill ’1’s or flags
  - Detection of receive line status
  - Zero bit insertion and deletion

Type	Package
PEB 20532, PEF 20532	P-TQFP-100-3

  - CRC generation and checking (CRC-CCITT or CRC-32)
  - Transparent CRC option per channel and/or per frame
  - Programmable Preamble (8 bit) with selectable repetition rate
  - Error detection (abort, long frame, CRC error, short frames)
- Bit Synchronous PPP Mode
  - Bit oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Zero bit insertion/deletion
  - 15 consecutive ’1’ bits abort sequence
- Octet Synchronous PPP Mode
  - Octet oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Programmable character map of 32 hard-wired characters (00_H-$1F_H$)
  - Four programmable characters for additional mapping
  - Insertion/deletion of control-escape character ($7D_H$) for mapped characters
- Asynchronous PPP Mode
  - Character oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Start/stop bit framing of single character
  - Programmable character map of 32 hard-wired characters (00_H-$1F_H$)
  - Four programmable characters for additional mapping
  - Insertion/deletion of control-escape character ($7D_H$) for mapped characters
- Asynchronous (ASYNC) Protocol Mode
  - Selectable character length (5 to 8 bits)
  - Even, odd, forced or no parity generation/checking
  - 1 or 2 stop bits
  - Break detection/generation
  - In-band flow control by XON/XOFF
  - Immediate character insertion
  - Termination character detection for end of block identification
  - Time out detection
  - Error detection (parity error, framing error)
- BISYNC Protocol Mode
  - Programmable 6/8 bit SYN pattern (MONOSYNC)
  - Programmable 12/16 bit SYN pattern (BISYNC)
  - Selectable character length (5 to 8 bits)
  - Even, odd, forced or no parity generation/checking
  - Generation of interframe-time fill ’1’s or SYN characters
  - CRC generation (CRC-16 or CRC-CCITT)
  - Transparent CRC option per channel and/or per frame
  - Programmable Preamble (8 bit) with selectable repetition rate
  - Termination character detection for end of block identification
  - Error detection (parity error, framing error)
- Extended Transparent Mode
  - Fully bit transparent (no framing, no bit manipulation)
  - Octet-aligned transmission and reception

- Protocol and Mode Independent
  - Data bit inversion
  - Data overflow and underrun detection
  - Timer

Protocol Support

- Address Recognition Modes
  - No address recognition (Address Mode 0)
  - 8-bit (high byte) address recognition (Address Mode 1)
  - 8-bit (low byte) or 16-bit (high and low byte) address recognition (Address Mode 2)
- HDLC Automode
  - 8-bit or 16-bit address generation/recognition
  - Support of LAPB/LAPD
  - Automatic handling of S- and I-frames
  - Automatic processing of control byte(s)
  - Modulo-8 or modulo-128 operation
  - Programmable time-out and retry conditions
  - SDLC Normal Response Mode (NRM) operation for slave
- Signaling System #7 (SS7) support
  - Detection of FISUs, MSUs and LSSUs
  - Unchanged Fill-In Signaling Units (FISUs) not forwarded
  - Automatic generation of FISUs in transmit direction (incl. sequence number)
  - Counting of errored signaling units
- Optional $\overline{\text{DTACK}}$/$\overline{\text{READY}}$ controlled cycles

Microprocessor Interface

- 8/16-bit bus interface
- Multiplexed and De-multiplexed address/data bus
- Intel/Motorola style
- Asynchronous interface
- Maskable interrupts for each channel

General Purpose Port (GPP) Pins (up to 7)

General

- 3.3V power supply with 5V tolerant inputs
- Low power consumption
- Power safe features
- P-TQFP-100-3 Package (Thermal Resistance: R_{JA} = 42 K/W)

1.2 Logic Symbol

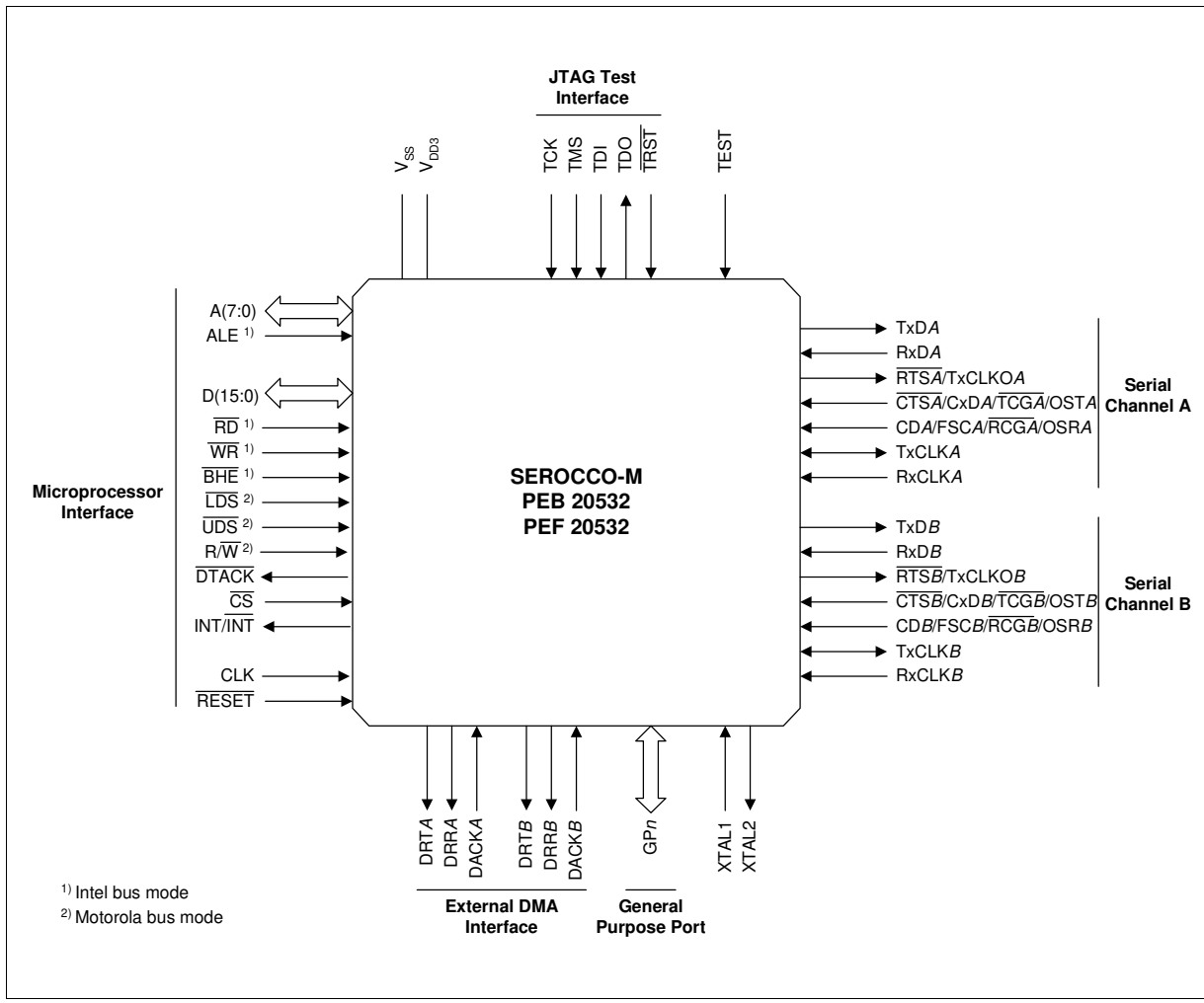

Figure 1 Logic Symbol

1.3 Typical Applications

SEROCCO-M devices can be used in LAN-WAN inter-networking applications such as Routers, Switches and Trunk cards and support the common V.35, ISDN BRI (S/T) and RFC1662 standards. Its new features provide powerful hardware and software interfaces to develop high performance systems.

1.3.1 System Integration Example

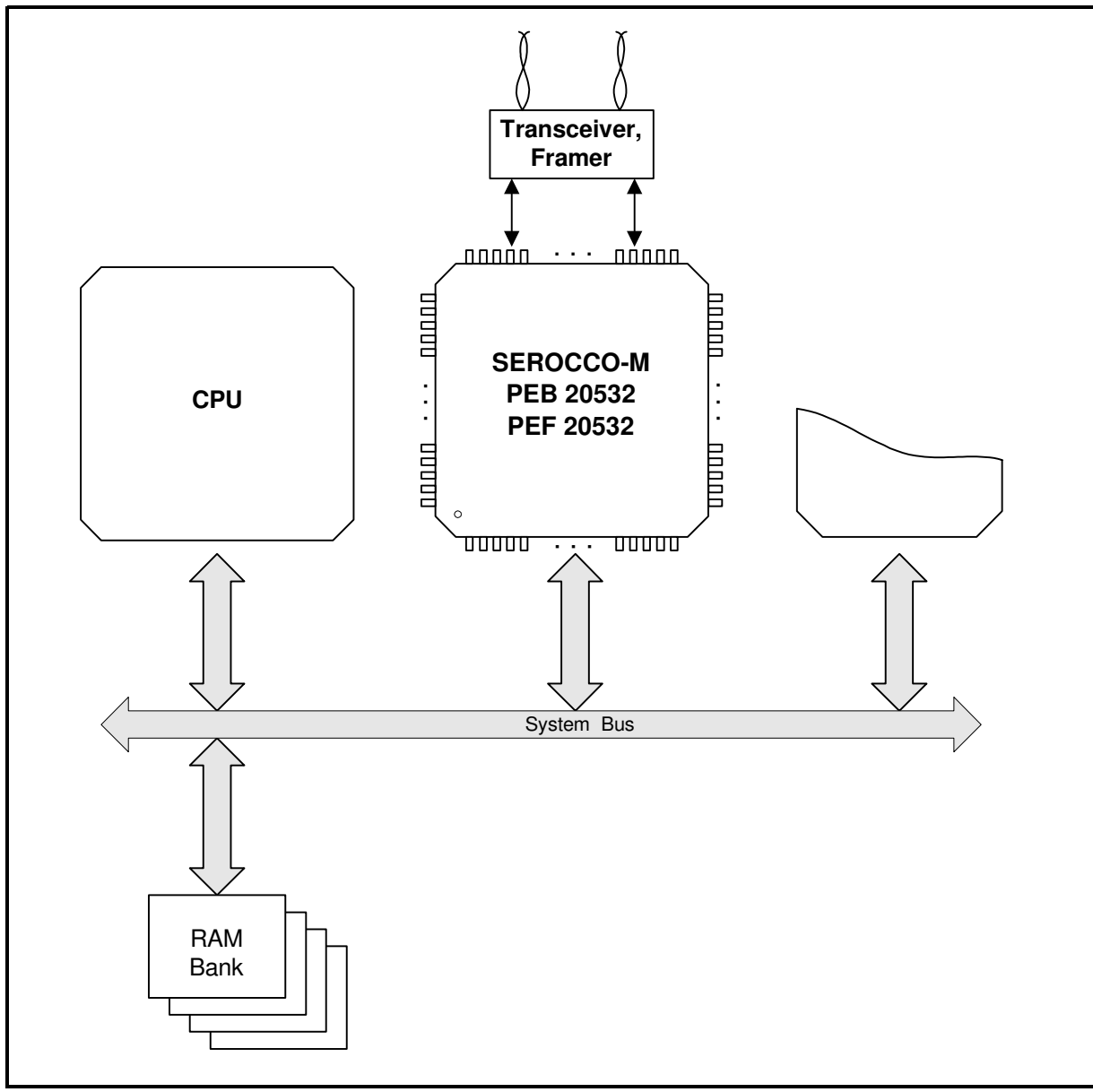

Figure 2 System Integration

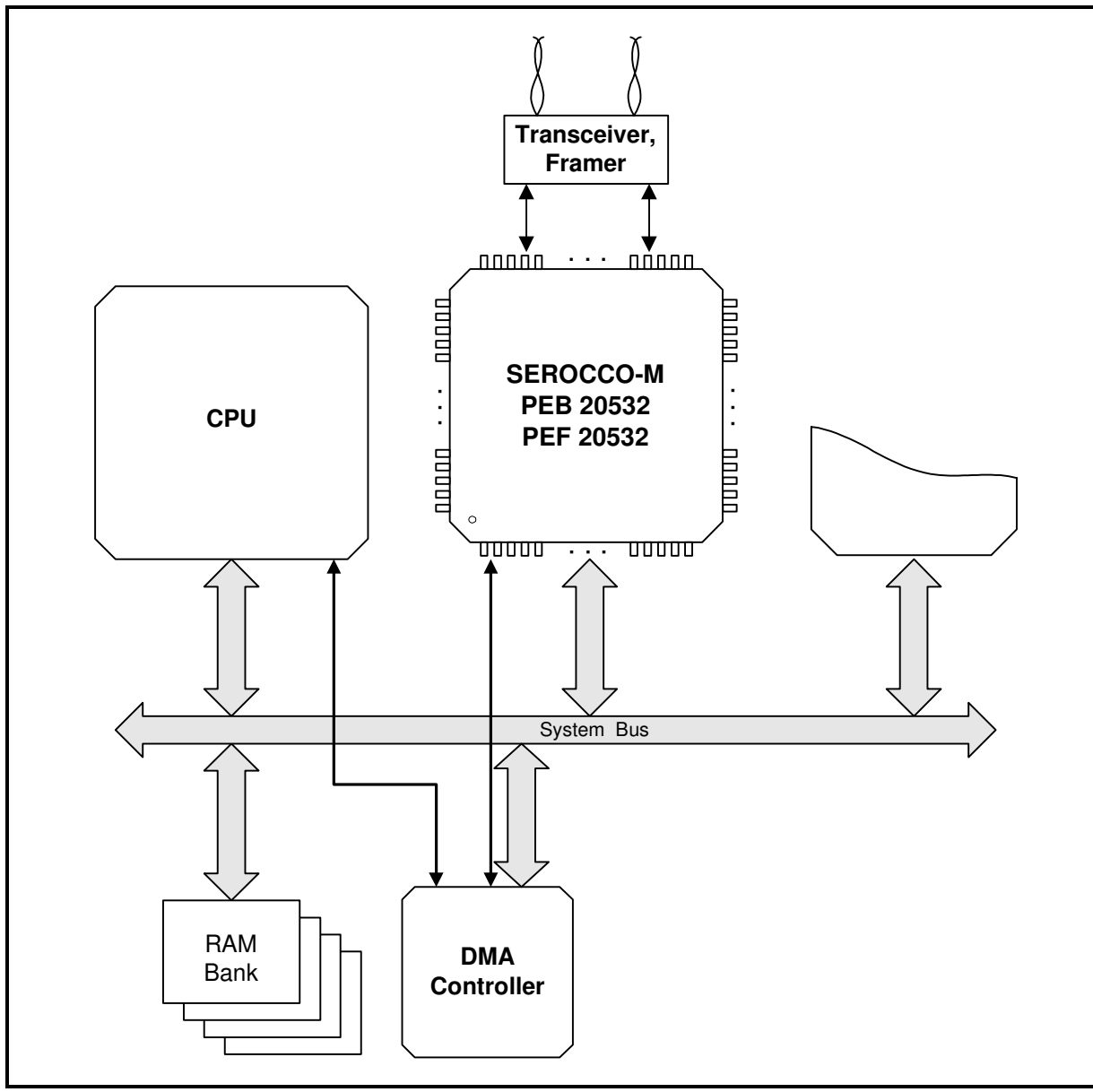

Figure 3 System Integration With External DMA Controller

1.3.2 Serial Configuration Examples

SEROCCO-M supports a variety of serial configurations at Layer-1 and Layer-2 level. The outstanding variety of clock modes supporting a large number of combinations of external and internal clock sources allows easy integration in application environments.

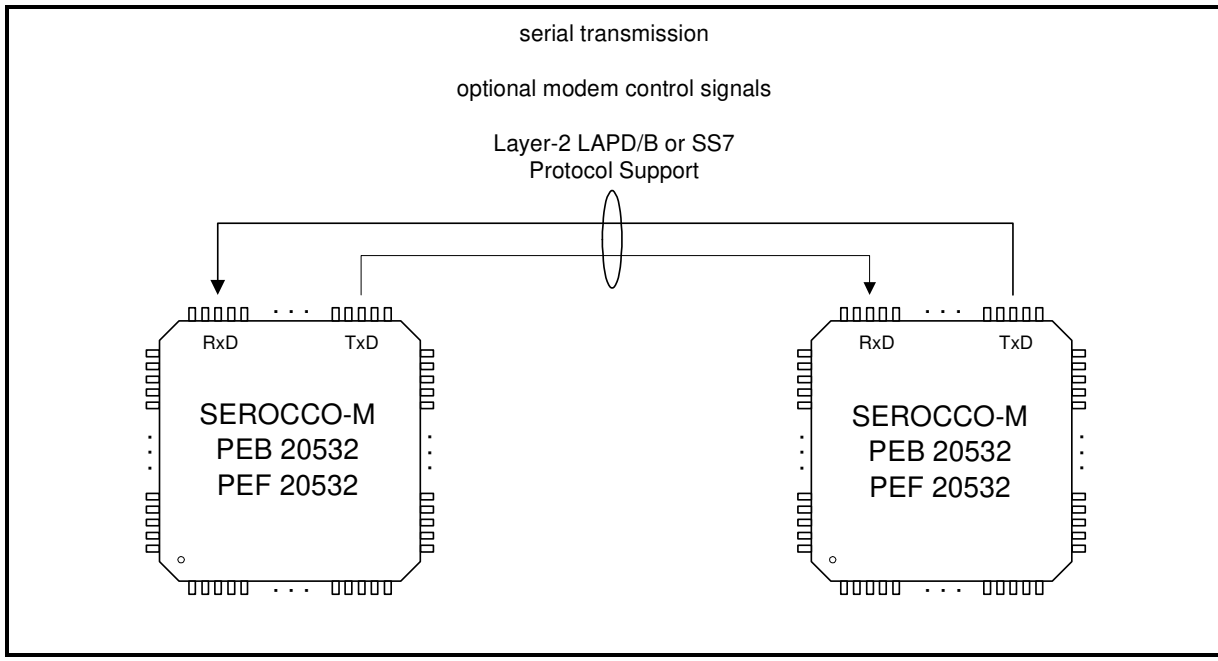

Figure 4 Point-to-Point Configuration

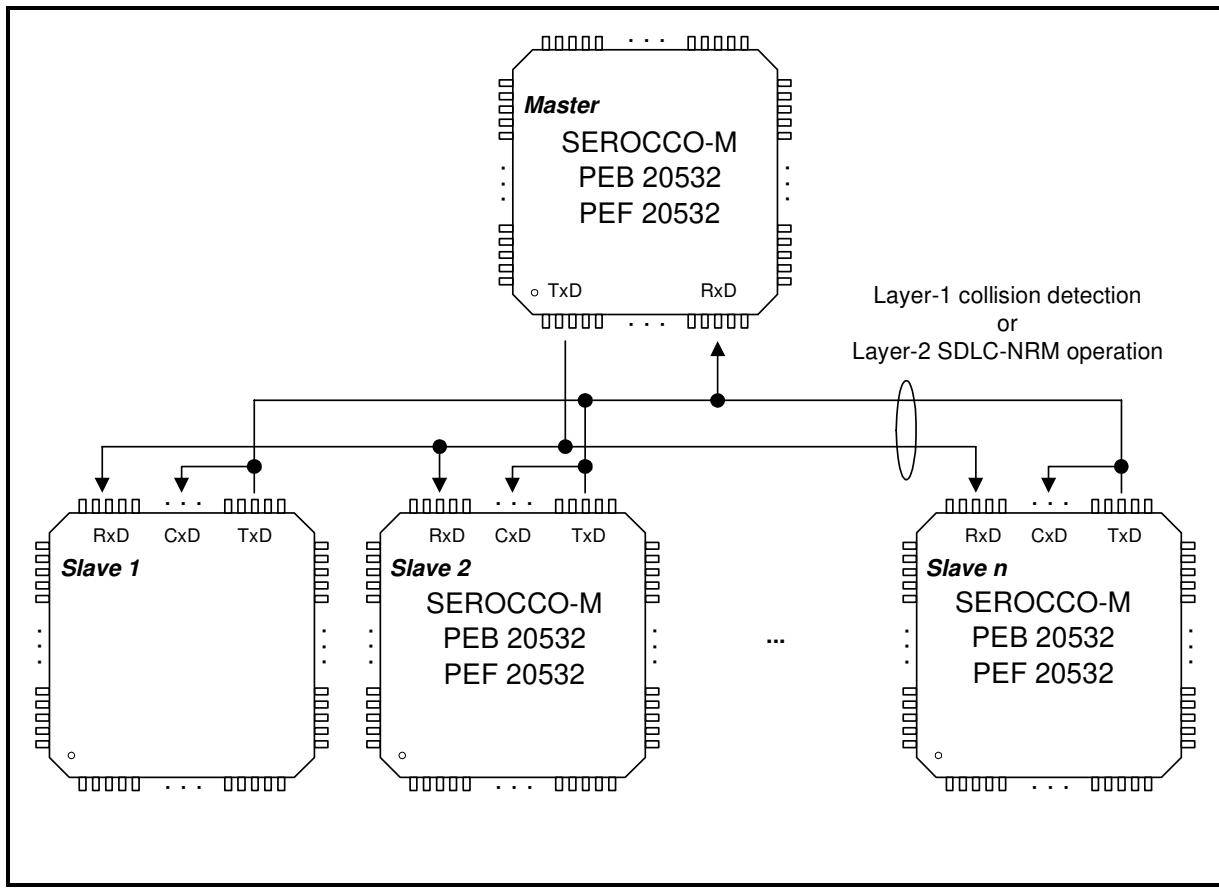

Figure 5 Point-to-Multipoint Bus Configuration

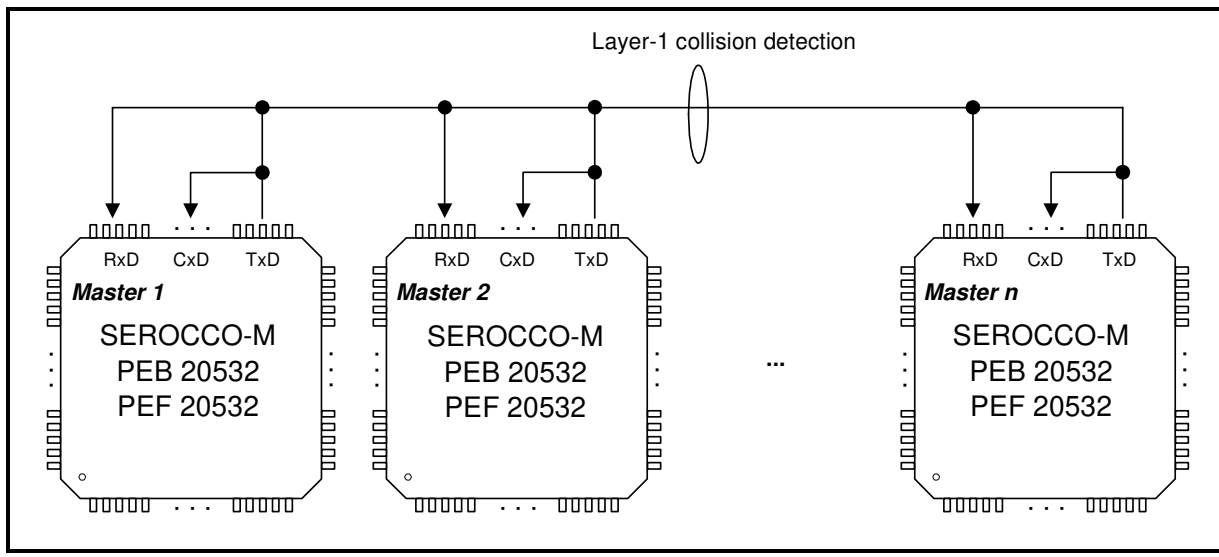

Figure 6 Multimaster Bus Configuration