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Data Sheet, DS 2.1, July 2003

DELIC-LC
DELIC-PB
DSP Embedded Line and Port Interface Controller

PEB 20570 Version 3.1
PEB 20571 Version 3.1

Wired Communications

Never stop thinking.

Edition 2003-07-31

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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PEB 20570

Revision History:	**2003-07-31**	DS 2.1
Previous Version:	DS2	

Page	Subjects (major changes since last revision)
	Trademarks updated

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Preface

This document provides reference information on the DELIC-LC/-PB Version 3.1.

Organization of this Document

This Data Sheet is divided into 11 chapters and appendices. It is organized as follows:

- **Chapter 1 Introduction**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- **Chapter 2 Pin Description**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
- **Chapter 3 Interface Description**
  Describes the DELIC external interfaces.
- **Chapter 4 Functional Description**
  Describes the features of the main functional blocks.
- **Chapter 5 DELIC Memory Structure**
  Containes the memory organisation of the OakDSPCore®.
- **Chapter 6 Register Description**
  Containes the detailed register description.
- **Chapter 7 Package Outlines**
- **Chapter 8 Electrical Characteristics and Timing Diagrams**
  Containes the DC specification.
  Contains the AC specification.
- **Chapter 9 Application Hints**
  Provides e.g. a worksheet
- **Chapter 10 Glossary**
- **Chapter 11 Index**

Your Comments

We welcome your comments on this document as we are continuously aiming at improving our documentation. Please send your remarks and suggestions by e-mail to

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Please provide in the subject of your e-mail:
device name (DELIC-LC/ -PB), device number (PEB 20570/PEB 20571), device version (Version 3.1), or and in the body of your e-mail:
document type (Data Sheet), issue date (2003-07-31) and document revision number (DS 2.1).

1 Introduction

The DELIC and VIP chipset realizes multiple ISDN S/T and U_{PN} interfaces together with controller functionality typically needed in PBX or Central Office systems. This functionality comprises voice channel handling, signaling control, layer-1 control, and even signal processing tasks.

Moreover it provides a programmable master/slave clock generator with 2 PLLs, an universal µP interface and a DMA interface.

The controller part, **DELIC,** is available in two different versions:

- **DELIC-LC** (**PEB 20570**) is a line card controller providing voice channel switching, multiple HDLC and layer-1 control for up to three VIPs (24 ISDN channels). Other transceiver ICs (32 analog or 16 digital channels) may additionally be connected via IOM-2/GCI interface.
- **DELIC-PB (PEB 20571**) additionally provides a programmable telecom DSP including program and data RAM. This DSP can be used for layer-1 control, protocol support and signal processing. The flexibility gained by the programmability allows Infineon to offer different application specific solutions with the same silicon just by software configuration.
  A configuration tool assists the user in finding a valid system configuration. Even more customer specific DSP-routines can be integrated with the assistance of Infineon.

The transceiver part, **VIP**, is available in two different versions:

- **VIP PEB 20590** is the first (8 channel) ISDN transceiver that implements multiple U_{PN} and S/T interfaces within one device. The user can decide by programming in which mode a desired channel shall work.
  A total of 8 channels are provided for layer-1 subscriber or trunk line characteristic. The VIP is programmed by the DELIC via the IOM-2000 interface. VIP's eight channels are programmable in the following maximum partitioning between U_{PN} and S/T channels:

	Max. number of U_{PN} and S/T Channels				
U_{PN}	8	7	6	5	4
S/T	0	1	2	3	4

- **VIP-8 PEB 20591** Additionally to the features of the VIP, the VIP-8 allows any combination of U_{PN} S/T interface (i.e. each of the 8 channels may be programmed to S/T or U_{PN} mode)

Block diagrams:

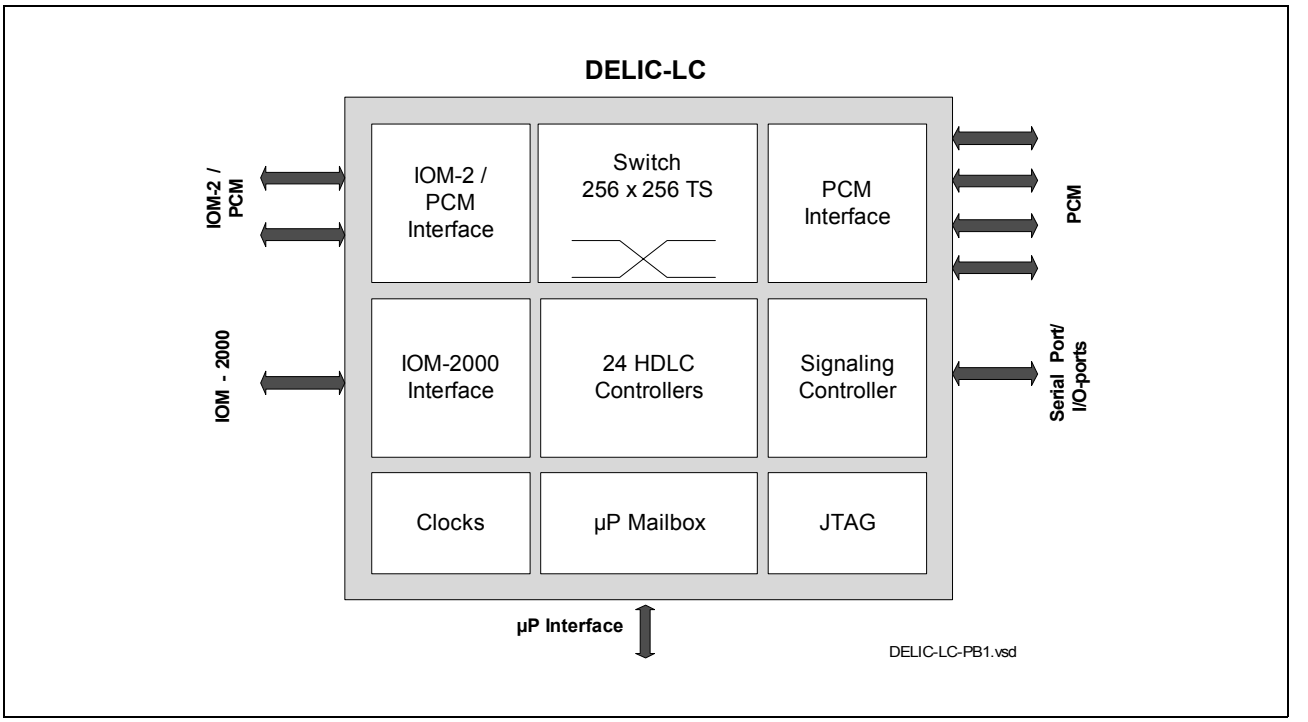


Figure 1 Block Diagram of the DELIC-LC

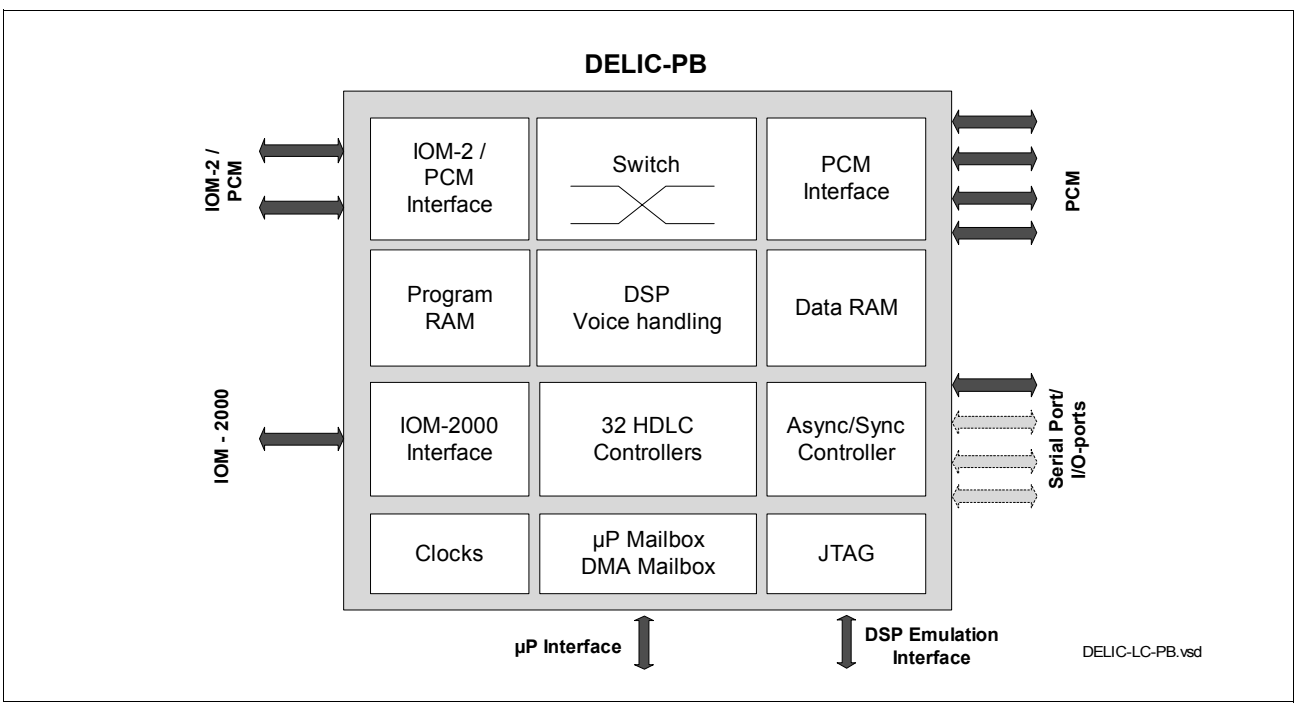
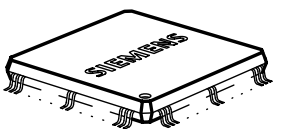


Figure 2 Block Diagram of the DELIC-PB

DSP Embedded Line and Port Interface Controller **PEB 20570**
DELIC-LC
DELIC-PB **PEB 20571**

Version 3.1 **CMOS**

1.1 DELIC-LC Key Features



P-TQFP-100-3

DELIC-LC is optimized for line card applications:

- One IOM-2000 interface supporting three VIPs i.e. up to 24 ISDN channels
- Two IOM-2 (GCI) ports (configurable as PCM ports) supporting up to 16 ISDN channels or 32 analog subscribers
- Four PCM ports with up to 4 x 2.048 Mbit/s (4 x 32 TS) or 2 x 4.096 Mbit/s or 1 x 8.192 Mbit/s
- Switching matrix 256 x 256 TS (8-bit switching)
- 24 HDLC controllers assignable to any D- or B-channel (at 16 kbit/s or 64 kbit/s)
- Serial communication controller: high-speed signaling channel for 2.048 Mbit/s
- General purpose I/O ports
- Standard multiplexed and de-multiplexed µP interface: Infineon, Intel, Motorola
- Programmable PLL based Master/Slave clock generator, providing all system clocks from a single 16.384 MHz crystal source
- JTAG compliant test interface
- single 3.3 V power supply, 5 V tolerant inputs

1.2 DELIC-PB Key Features

Compared to the DELIC-LC, having a fixed functionality, the DELIC-PB provides a high degree of flexibility (in terms of selected number of ports or channels).

Additionally it features computing power for typical DSP-oriented PBX tasks like conferencing, DTMF etc.

A Microsoft Windows based configuration tool, the Configurator, enables to generate an application specific functionality. Its features are mainly determined by the firmware of the integrated telecom DSP.

Type	Package
PEB 20571/ PEB 20570	P-TQFP-100-3

List of maximum available features:

- One IOM-2000 interface supporting up to three VIPs i.e. up to 24 ISDN channels
- Support of DASL mode
- Up to two IOM-2 (GCI) ports (also configurable as PCM ports) supporting up to 16 ISDN channels or 32 analog subscribers
- Up to four PCM ports with up to 4 x 2.048 Mbit/s (4 x 32 TS) or 2 x 4.096 Mbit/s or 1 x 8.192 Mbit/s
- Switching matrix 256 x 256 TS (switching of 4-/8- bit time slots)
- Up to 32 HDLC controllers assignable to any D- or B-channel (at 16 kbit/s or 64 kbit/s)
- Up to 4 serial communication controllers: one of them with up to 8.192 Mbit/s data rate
- General purpose I/O ports
- DECT synchronization support
- Standard multiplexed and de-multiplexed µP interface: Infineon, Intel, Motorola
- Dedicated DMA support mailbox for 2 DMA-channels
- Integrated DSP core OAK+ (60 MIPS for layer 1 control, signalling and DSP-algorithms)
- 4 kWord on-chip program memory
- 2 kWord on-chip data memory
- 2 kWord ROM
- DSP work load measurement for run-time statistics, DSP alive indication
- On chip debugging unit
- Serial DSP program debugging interface connected via JTAG port
- A-/µ-law conversion unit
- Programmable PLL based Master/Slave clock generator, providing all system clocks from a single 16.384 MHz crystal source
- JTAG compliant test interface
- single 3.3 V power supply, 5 V compatible inputs

*Note: As each feature consumes system resources (DSP-MIPS, memory, port pins), the maximum available number of supported interfaces or HDLC channels is limited by the totally available resources. A System Configurator tool (**see DELIC Software User's Manual)** helps to determine a valid configuration.*

1.3 Logic Symbol

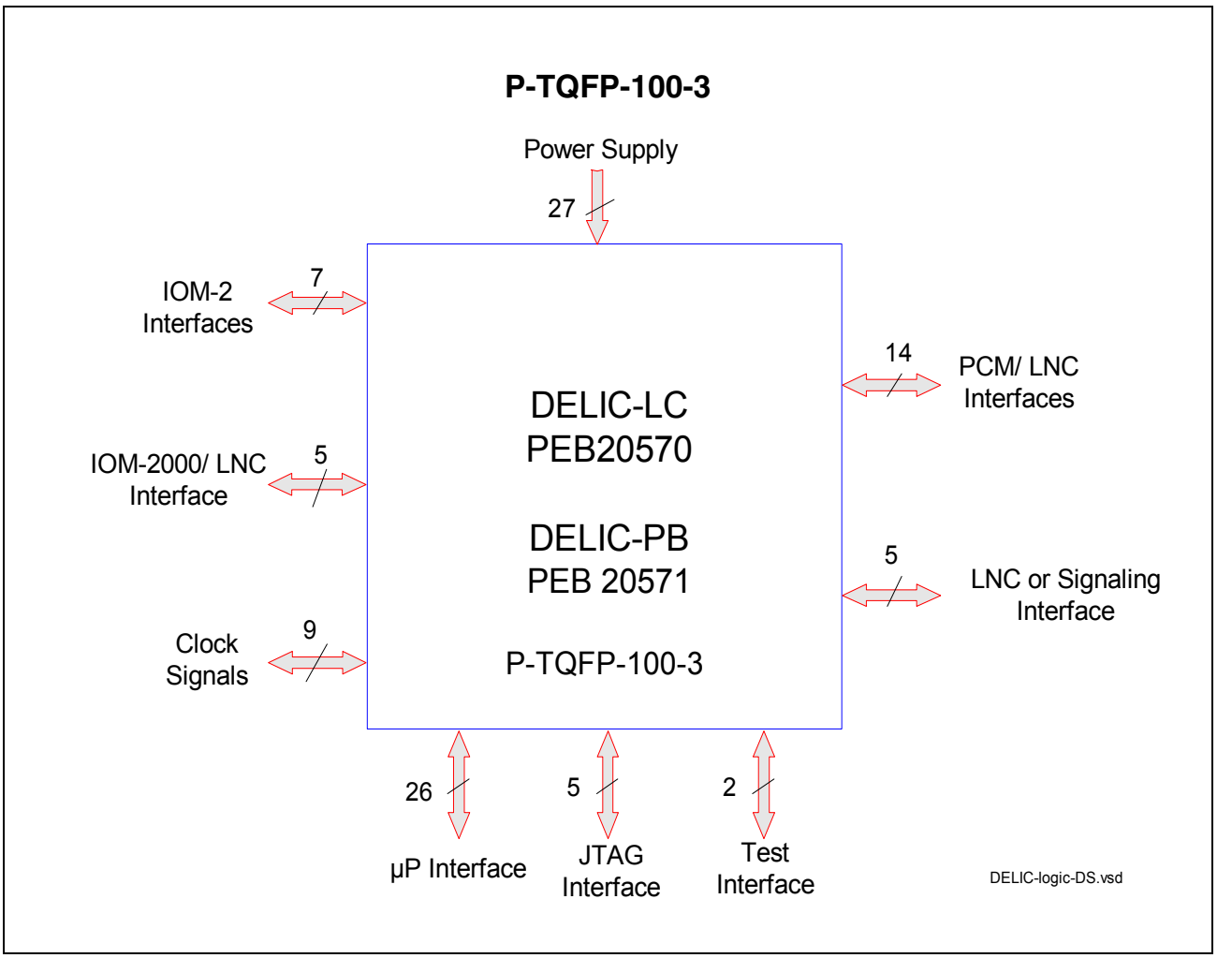


Figure 3 Logic Symbol

1.4 Typical Applications

1.4.1 Applications for DELIC-LC

The following two figures show example configurations of DELIC-LC Line card applications for different ISDN interface standards.

In **Figure 4**, three VIP transceiver ICs are connected to the DELIC-LC via the IOM-2000 interface, whereas in **Figure 5** and **Figure 6** an IOM-2 (GCI) interface is used to connect other ISDN transceivers.

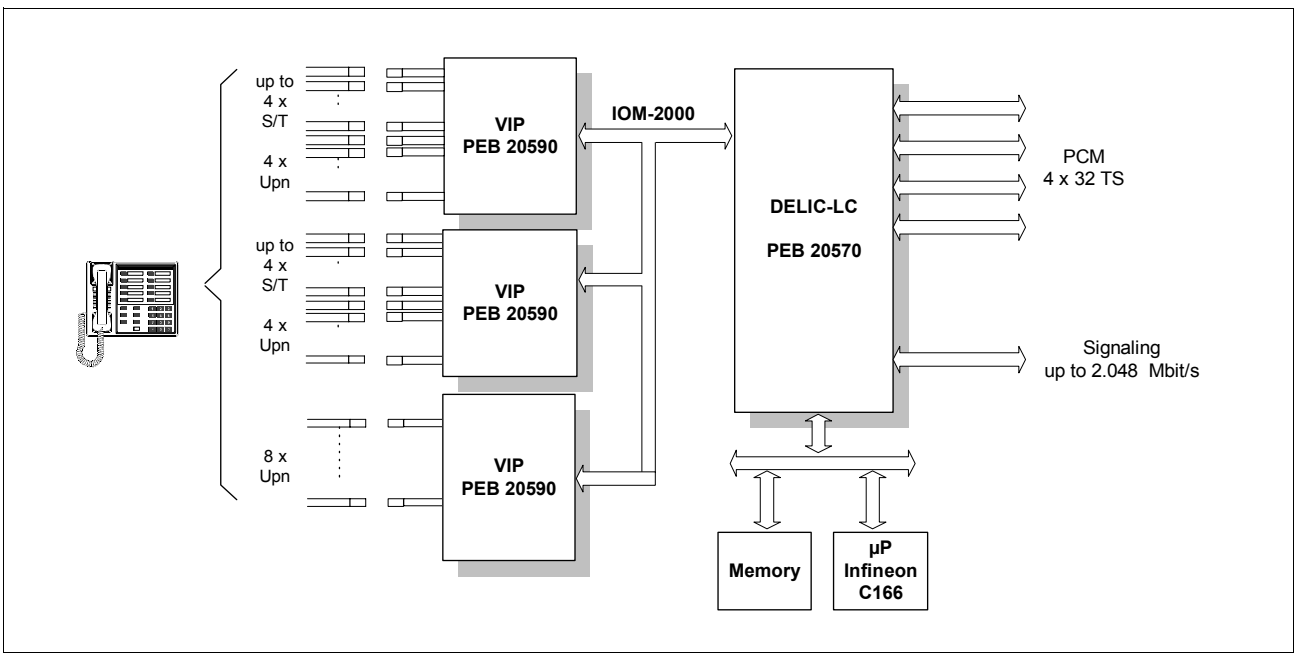


Figure 4 DELIC-LC in S/T and U_{PN} Line Cards (up to 8 S/T and 16 U_{PN})

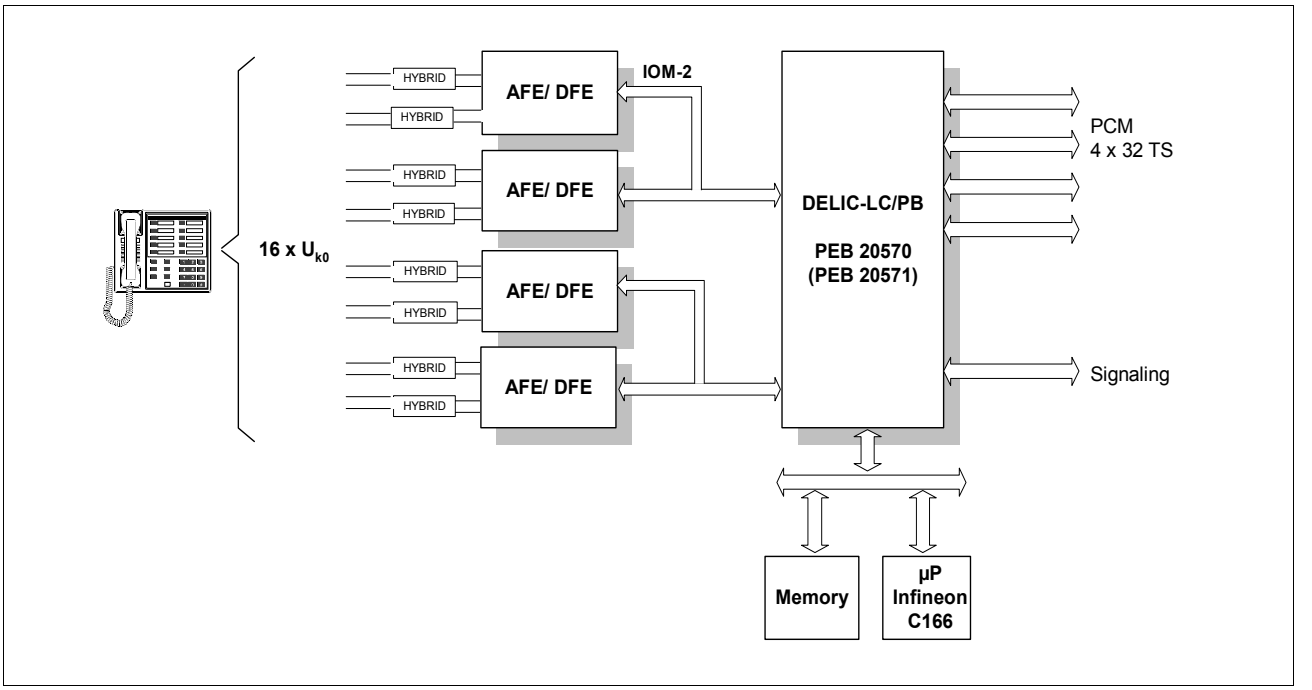


Figure 5 DELIC-LC/PB in Uk0 Line Card for 16 Subscribers

Note: In this application DELIC-PB is also meaningful.

1.4.2 Applications for DELIC-PB

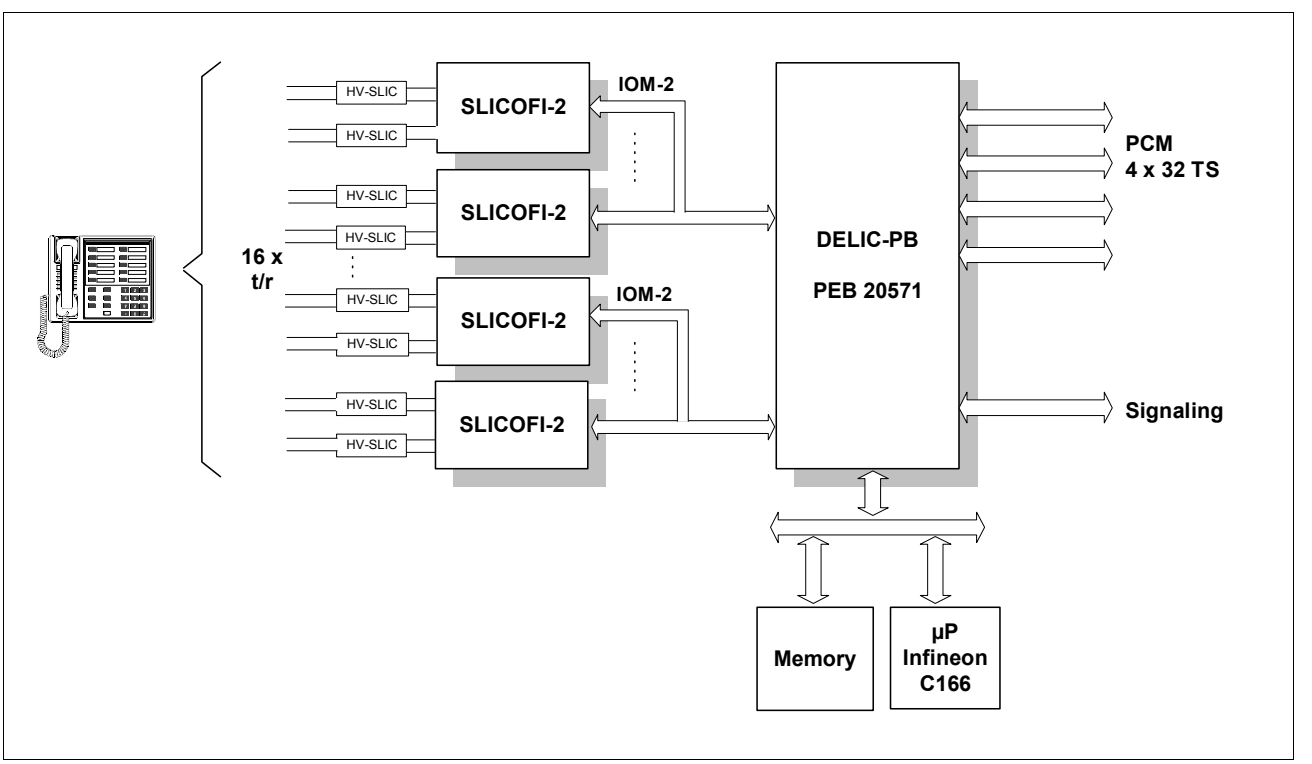


Figure 6 DELIC-PB in Analog Line Card for 16 Subscribers