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Data Sheet, Rev. 1, May 2004

IEC-4-AFE-X

Quad ISDN Echocancellation Circuit Analog Front End for Splitterless ADSL over ISDN

PEB 24902, Version 3.2

PEF 24902, Version 3.2

Wireline Communications

Infineon technologies

Never stop thinking.

Edition 2004-05-28

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Revision History: **2004-05-28** Rev. 1

Previous Version: **AFE V3.2 Preliminary Data Sheet DS1**

Page	Subjects (major changes since last revision)
Page 9	Aplication: Added reference to System Description GEMINAX MAX
Page 10	References: Updated
Page 13	Added N.C.: Not connected.
Page 28	Removed Figure 7 (PSD mask for 4B3T ADSL-friendly) and Figure 8 (PSD mask 2B1Q ADSL-friendly) (described in System Description GEMINAX MAX)
Page 29	Absolute peak voltage: Removed values (There is no pulse mask specified) Added common DC level
Page 38	Reset & POR reset also the digital low pass filter
Page 40	Added power consumption values for 2B1Q
Page 40	Initialization and Operation: Added reference to System Description GEMINAX MAX
Page 42	Starpoint hybrid: Added values for main inductance of blocking coils, removed reference to FTZ 1 TR 216
Page 43	Added trafo type
Page 44	Added external circuitry for 2B1Q ADSL-friendly
Page 48	Removed pull-up specification

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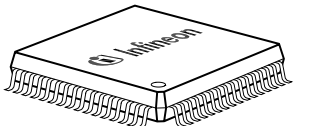
Quad ISDN Echocancellation Circuit Analog Front End for Splitterless ADSL over ISDN **PEF 24902**
IEC-4-AFE-X

Version 3.2

Features



P-MQFP-64-9 HS

1 Overview

The IEC-4-AFE-X Version 3.2 is part of Infineon´s chip set for a splitterless, FDD (non-overlapped) ADSL over ISDN linecard based on GEMINAX MAX according to **Ref [3.]**, chapter 4.2.2 of **Ref [5.]**, Annex B of **Ref [6.]** / **Ref [7.]**, and **Ref [8.]**. **Figure 1** shows the basic architecture of an integrated ISDN and ADSL linecard based on GEMINAX MAX chip set. The IEC-4-AFE-X Version 3.2 is designed for use in central office, DLCs and DSLAMs.

1.1 Features of the IEC-4-AFE-X Version 3.2

- Four port ISDN Echo Cancellation Circuit Analog Frontend
- Offers all features of AFE V2.1 (**Ref [1.]**)[1)]
- Integrated digital transmit low-pass filter, which obsoletes the need for an discrete, passive splitter device
- Conforms in connection with GEMINAX MAX chip set to **Ref [3.]**, especially to the following ISDN PSD masks:
  - 'PSD mask for a 4B3T ISDN system with integrated splitter' acc. to **Ref [3.]** (4B3T ADSL friendly, compatible to ADSL US spectrum down to 138 kHz)
  - 'PSD mask for a 2B1Q ISDN system with integrated splitter' acc. to **Ref [3.]** (2B1Q ADSL friendly, compatible to ADSL US spectrum down to 120 kHz)
- Footprint compatible to AFE V2.1 (**Ref [1.]**)
- Serial control interface for communication with GEMINAX MAX chip set

1) With the exception of features for ISDN only, which are overruled by **Ref [3.]**

Type	Package
PEB 24902	P-MQFP-64-9 HS
PEF 24902	P-MQFP-64-9 HS

1.2 Application Diagram

Figure 1 shows a typical application of IEC-4-AFE-X Version 3.2 together with Infineon´s IC family for splitterless FDD ADSL over ISDN and DFE-T/Q Version V2.2 (**Chapter 1.3**) for an integrated voice and data solution (IVD).

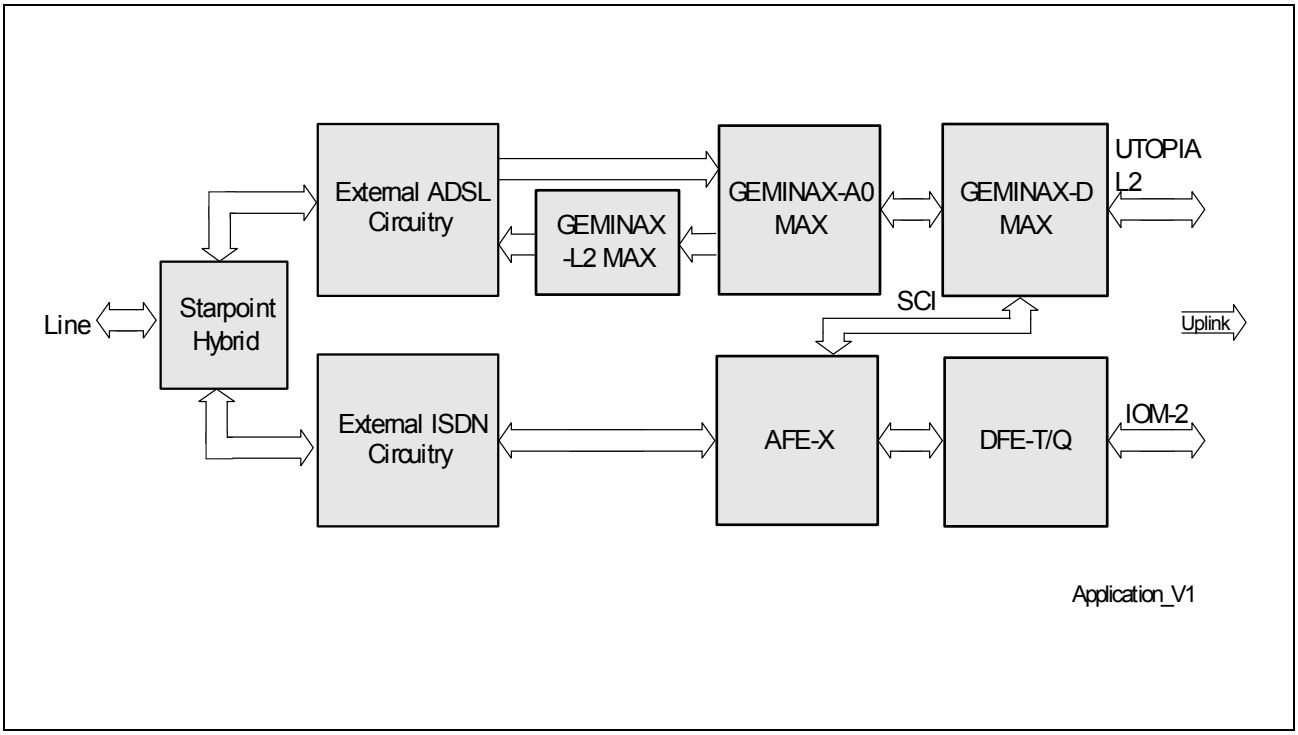


Figure 1 Application Diagram

*Note: IEC-4-AFE-X Version 3.2 is designed for operation with GEMINAX MAX chip set. The system properties of an IVD ISDN consisting of GEMINAX MAX chipset, IEC-4-AFE-X Version 3.2 and DFE-Q/T V2.2 are described in **Ref [9.]**.*

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1.3 Infineon´s IC Family for Splitterless FDD ADSL over ISDN

ISDN

- PEB 24902 / PEF 24902 IEC-4-AFE-X Version 3.2
- PEF 24911 DFE-Q Version 2.2
- PEF 24901 DFE-T Version 2.2

ADSL

- PEF 55008 GEMINAX-D MAX
- PEF 55204 GEMINAX-A0 MAX
- PEF 55208 GEMINAX-A8 MAX
- PEB 22716 GEMINAX-L2 MAX

1.4 Related Documentation

1. AFE V2.1, Quad ISDN Echocancellation Circuit Analog Front End, PEF / PEB 24902 Version 2.1, Data Sheet DS2, Infineon Technologies AG, January 2001
2. TS 102080 V1.3.2, Transmission and Multiplexing; ISDN basic rate access, Digital transmission system on metallic local lines, ETSI, May 2000
3. TS 102080 V1.4.1, Transmission and Multiplexing; ISDN basic rate access, Digital transmission system on metallic local lines, Annex-D: ISDN systems requirements when coexisting with ADSL or VDSL, ETSI, July 2003
4. TS 101952-1-3 V1.1.1, Access network xDSL transmission filters; Part 1: ADSL splitters for European Deployment; Sub-part 3: Specification of ADSL/ISDN Splitters, ETSI, May 2002
5. TS 101388 V1.3.1, Transmission and Multiplexing (TM); Access transmission systems on metallic access cables; Asymmetric Digital Subscriber Line (ADSL)-European specific requirements, ETSI, May 2002
6. G.992.1, Asymmetrical digital subscriber line (ADSL) transceivers, ITU-T, June 1999
7. G.992.3, Asymmetrical digital subscriber line transceivers 2 (ADSL2), ITU-T, July 2002
8. 1 TR 112, Description of the U-R2 Interface of ADSL Systems, U-R2 Interface, V5.1, DTAG, Dezember 2003
9. GEMINAX MAX, Preliminary User´s Manual, Rev. 1.0, ADSL2+ Data Only and Integrated Voice and Data Linecard, System Description, Infineon, Apr. 2004

1.5 Not Supported

IEC-4-AFE-X Version 3.2 does not support ISDN-only operation according to **Ref [2.]**. IEC-4-AFE-X Version 3.2 in connection with GEMINAX MAX chip set supports ADSL-friendly operation according to **Ref [3.]**, which overrules several requirements of **Ref [2.]**.

2 External Signals

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2.1 Logic Symbol

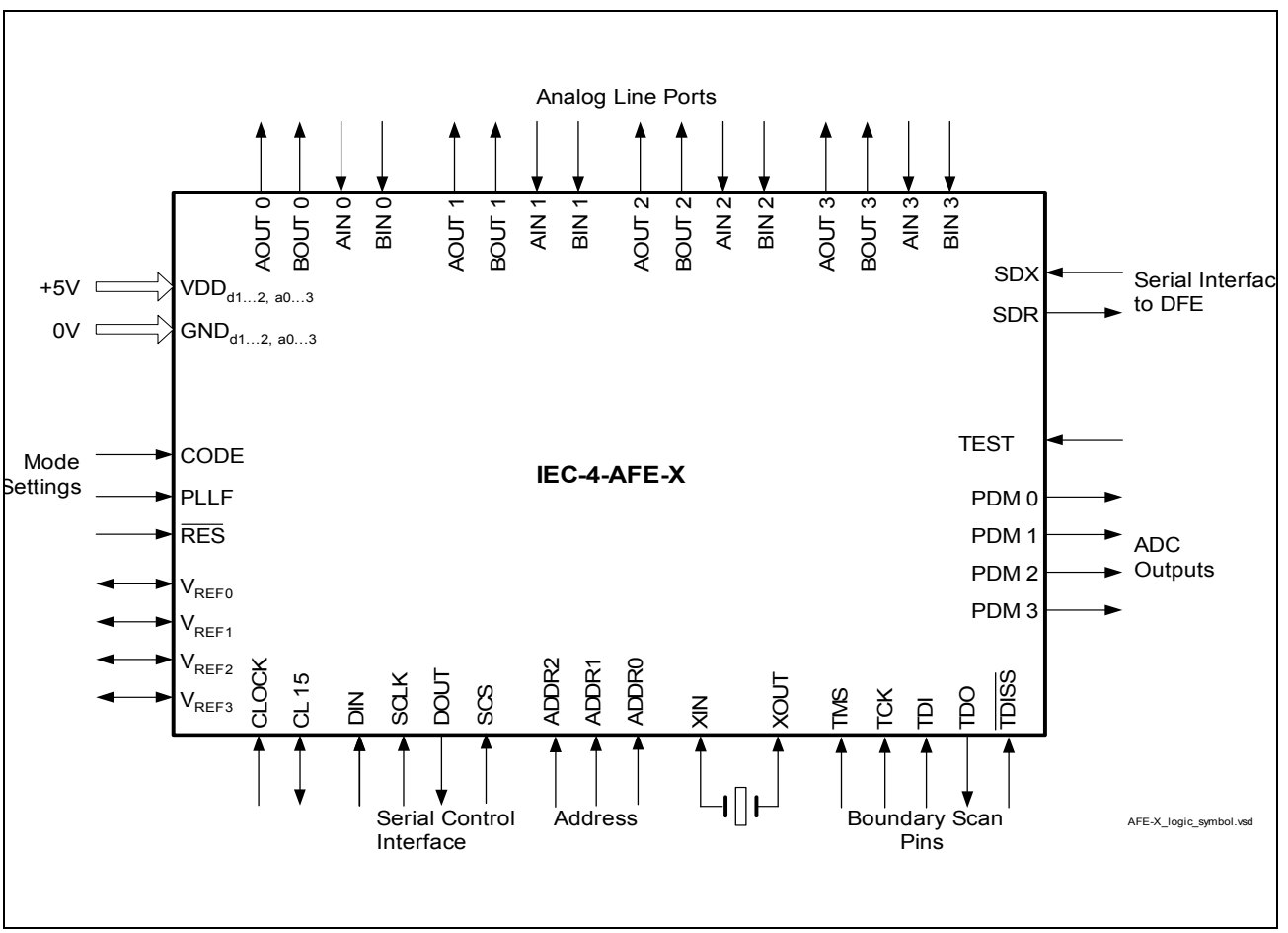

Figure 2 Logic Symbol IEC-4-AFE-X Version 3.2

2.2 Pin Diagram

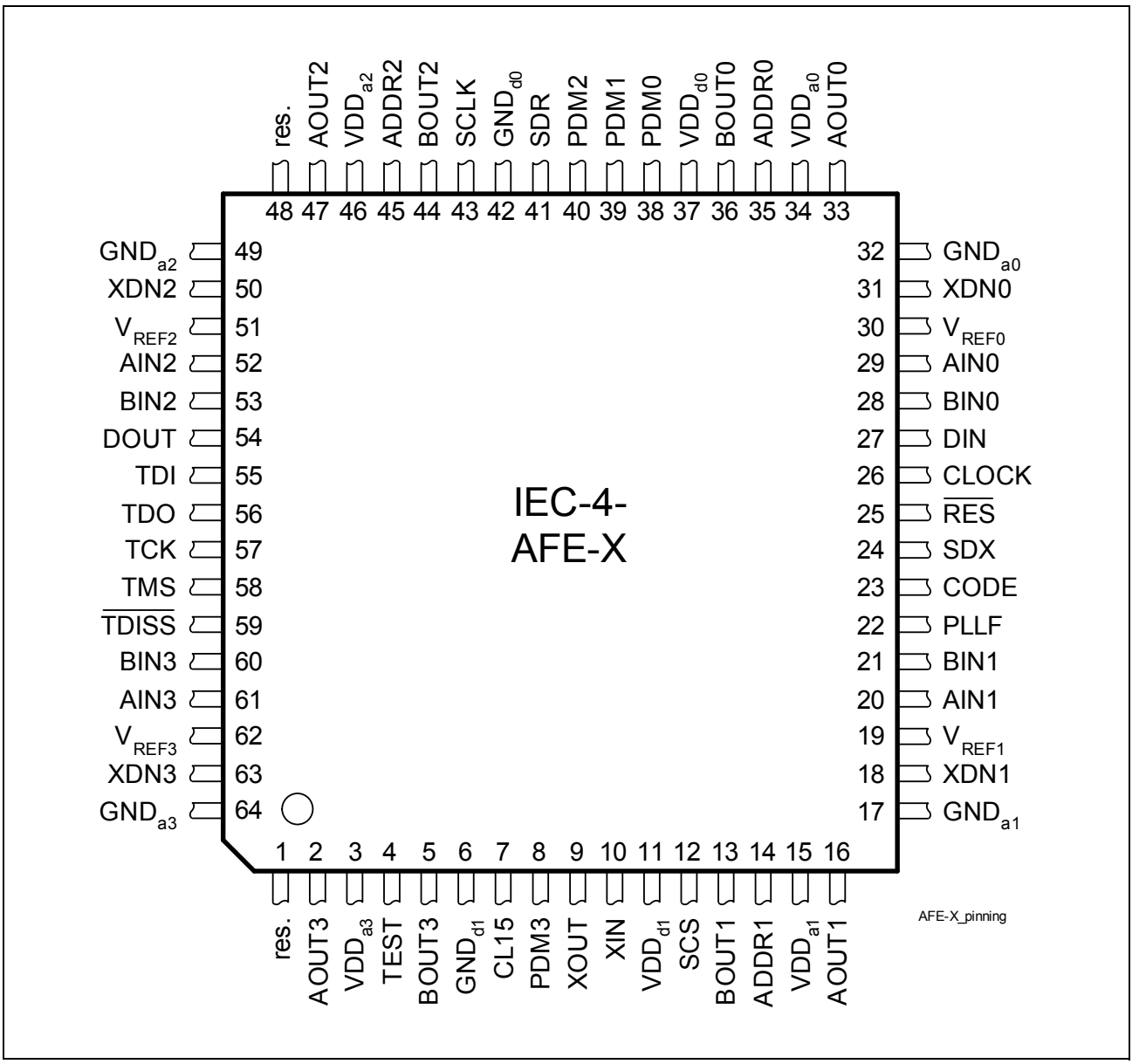

Figure 3 Pin Diagram IEC-4-AFE-X Version 3.2

2.3 Pin Description

2.3.1 General Aspects

The following abbreviations are used:

I	Input. Digital LvTTL levels
O	Output. Digital LvTTL levels
OD	Open Drain
PU	Pull Up
PD	Pull Down
N.C.	Not Connected

2.3.2 Pin Description: Changes to AFE V2.1

Some unused pins of AFE V2.1 are used for AFE-X for additional functionality.

Table 1 to Table 2 list all pins with changed functionality as compared to AFE V2.1.

Table 1 Serial Control Interface (SCI)

Pin No.	Old	New	I/O	Function
12	N.C.	SCS	I (PD)	**Tie to '1'**
43	N.C.	SCLK	I (PD)	**Serial Clock** Clock signal of the SCI
27	ADDR	DIN	I (PD)	**Serial Data Receive** Receive data line of the SCI
54	N.C.	DOUT	OD	**Serial Data Transmit** Transmit data line of the SCI

Table 2 Address Pins and Test Mode

Pin No.	Old	New	I/O	Function
35	N.C.	ADDR0	I (PD)	**Address 0** Pinstrapping of AFE-X address for SCI access
14	N.C.	ADDR1	I (PD)	**Address 1** Pinstrapping of AFE-X address for SCI access
45	N.C.	ADDR2	I (PD)	**Address 2** Pinstrapping of AFE-X address for SCI access

Table 2 Address Pins and Test Mode (cont'd)

Pin No.	Old	New	I/O	Function
4	N.C.	TEST	I (PD)	**TEST** 0: Inactive 1: IEC-4-AFE-X Version 3.2 test mode *Note: Pin TEST must be kept low.*
1	N.C.	res.	I (PD)	**Reserved** Reserved for future use. Leave open.
48	N.C.	res.	I (PD)	**Reserved** Reserved for future use. Leave open.

2.3.3 Pin Description: Complete List

Table 3 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Description
Power Supply Pins			
37	VDD_{d1}		5 V ±5% digital supply voltage
11	VDD_{d2}		
34	VDD_{a0}		5 V ±5% analog supply voltage
15	VDD_{a1}		
46	VDD_{a2}		
3	VDD_{a3}		
42	GND_{d1}		0 V digital
6	GND_{d2}		
32	GND_{a0}		0 V analog
17	GND_{a1}		
49	GND_{a2}		
64	GND_{a3}		
30	V_{REF0}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
19	V_{REF1}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions
51	V_{REF2}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions
62	V_{REF3}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions
JTAG Boundary Scan			
57	TCK	I	**Test Clock**
58	TMS	I (PU)	**Test Mode Select**
55	TDI	I (PU)	**Test Data Input**
56	TDO	O	**Test Data Output**
59	$\overline{\text{TDISS}}$	I (PU)	**JTAG Boundary Scan Disable** Active low, internal pullup (I_{TDISS} = -100 µA (typ.))

Note: case of JTAG interface disabled ($\overline{TDISS}$ = 0), pin TCK should be pulled down on board (e.g. pull-down of 47 kΩ).

Line Port Pins			
29	AIN0	I	**Differential U interface input** Line port 0
28	BIN0	I	**Differential U interface input** Line port 0
33	AOUT0	O	**Differential U interface output** Line port 0
36	BOUT0	O	**Differential U interface output** Line port 0
20	AIN1	I	**Differential U interface input** Line port 1
21	BIN1	I	**Differential U interface input** Line port 1

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
16	AOUT1	O	**Differential U interface output** Line port 1
13	BOUT1	O	**Differential U interface output** Line port 1
52	AIN2	I	**Differential U interface input** Line port 2
53	BIN2	I	**Differential U interface input** Line port 2
47	AOUT2	O	**Differential U interface output** Line port 2
44	BOUT2	O	**Differential U interface output** Line port 2
61	AIN3	I	**Differential U interface input** Line port 3
60	BIN3	I	**Differential U interface input** Line port 3
2	AOUT3	O	**Differential U interface output** Line port 3
5	BOUT3	O	**Differential U interface output** Line port 3
Digital Interface			
7	CL15	I/O	**Master Clock 15.36 MHz** All operations and the data exchange on the digital interface are based on this clock. CL 15 is set to an input at power-on. If a 15.36 MHz clock is generated by the internal PLL/oscillator or if an external clock is provided at XIN then CL15 becomes an output and issues this clock. If the pin XIN is clamped to low or high then CL15 remains an input and an other device has to provide the 15.36 MHz clock.
38	PDM0	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 0
39	PDM1	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 1

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
40	PDM2	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 2
8	PDM3	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 3
31	XDN0	N.C.	**For future use, leave pin open**
18	XDN1	N.C.	**For future use, leave pin open**
50	XDN2	N.C.	**For future use, leave pin open**
63	XDN3	N.C.	**For future use, leave pin open**
24	SDX	I	**Serial Data Transmit** Interface for the Transmit and Control Data. Up to eight[1)] lines can be multiplexed on SDX. Transmission and sampling is based on clock CL15 (15.36 MBit/s).
41	SDR	O	**Serial Data Receive** Level information for the detection of the awake tone. The four lines are multiplexed on SDR.
23	CODE	I	**Select 2B1Q or 4B3T Code** Code = low sets 2B1Q Code.
25	$\overline{\text{RES}}$	I	**Reset** Reset and power down of the entire AFE-X including PLL and all four line ports. Asynchronous signal, active low. *Note: While $\overline{\text{RES}}$=low, the PLL is not reset statically, but only during the fallig edge at pin $\overline{\text{RES}}$.*
PLL			
9	XOUT	O	**Crystal Out** 15.36 MHz crystal is connected. Leave open if not used.
10	XIN	I	**Crystal In** A synchronous 15.36 MHz clock signal or 15.36 MHz crystal is connected. Clamping XIN to either low or high sets CL15 to Input.

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
26	CLOCK	I	**Clock** 8 kHz or 2048 kHz clock as a time base of the 15.36 MHz clock. Connect to GND if not used.
22	PLLF	I (PU)	**PLL Frequency** Select corner frequency of PLL Jitter Transfer function. Internal pullup resistor (I_{PLLF} = -100 µA (typ.)).
Serial Control Interface			
12	SCS	I (PD)	**Tie to '1'**
43	SCLK	I (PD)	**Serial Clock** Clock signal of the SCI
27	DIN	I (PD)	**Serial Data Receive** Receive data line of the SCI
54	DOUT	OD	**Serial Data Transmit** Transmit data line of the SCI
Address Pins and Test Mode			
35	ADDR0	I (PD)	**Address 0** Pinstrapping of AFE-X address for SCI access
14	ADDR1	I (PD)	**Address 1** Pinstrapping of AFE-X address for SCI access
45	ADDR2	I (PD)	**Address 2** Pinstrapping of AFE-X address for SCI access
4	TEST	I (PD)	**TEST** 0: Inactive 1: IEC-4-AFE-X Version 3.2 test mode *Note: Pin TEST must be kept low.*
1	res.	I (PD)	**Reserved** Reserved for future use. Leave open.
48	res.	I (PD)	**Reserved** Reserved for future use. Leave open.

1) Only four lines are supported

3 Functional Description

Attention: ***Any warranty, whether express or implied shall be subject to the use of the chips within the procedure as outlined in the respective Data Sheet. In case the chips are used incorrectly or not used within the logic or electrical specifications, any and all warranty or other claim based on any defect or malfunction whatsoever shall be excluded.***

3.1 Block Diagram

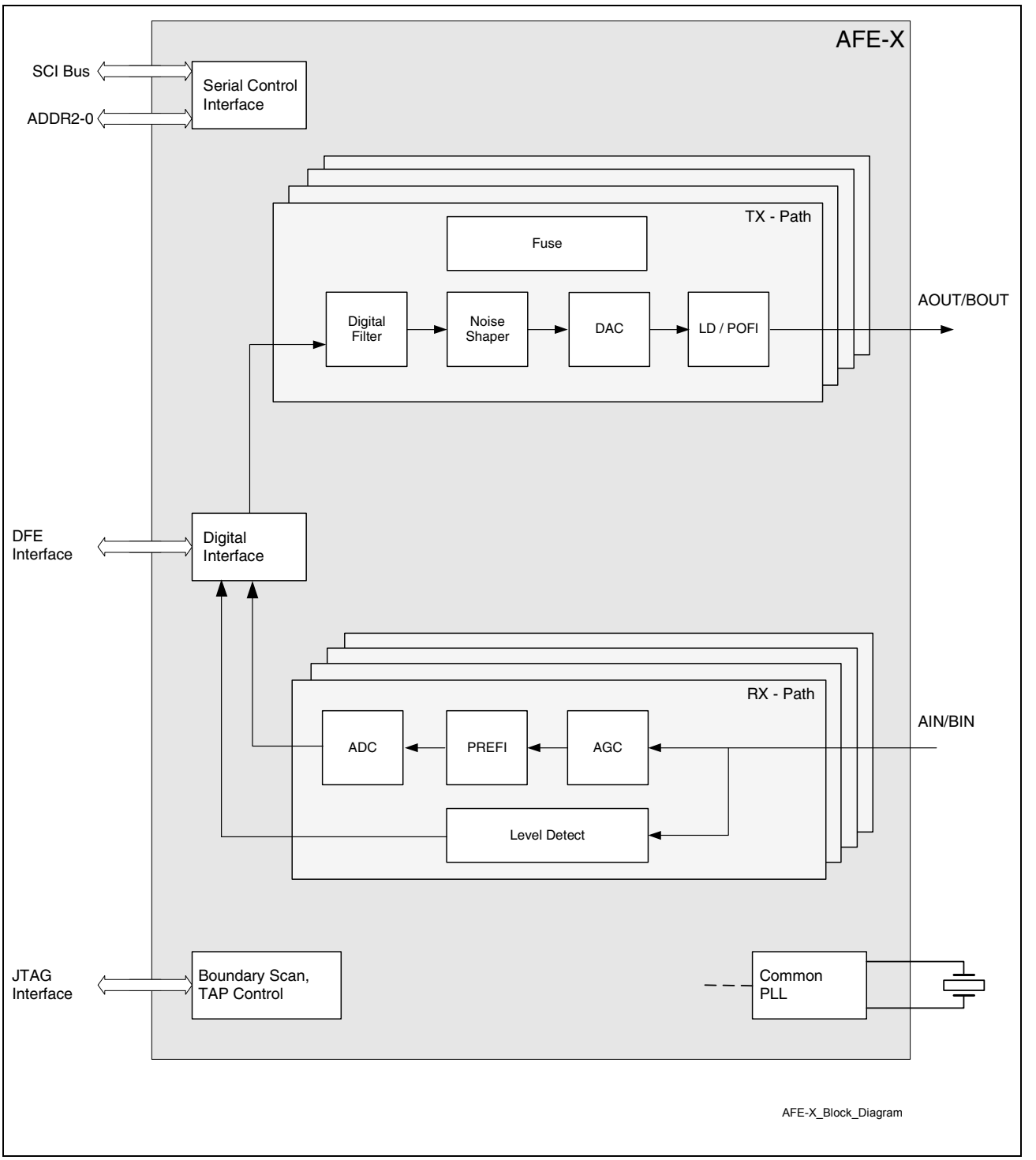

Figure 4 Block Diagram

3.2 Clock Generation

All timing signals are derived from a 15.36 MHz system clock. The 15.36 MHz clock can be provided by the IEC-4-AFE-X Version 3.2 by a crystal based PLL, which is synchronized to either an 8 kHz or a 2048 kHz clock at pin CLOCK. The frequency at pin CLOCK is detected automatically.

The PLL is set to the nominal frequency either by a POR or by a falling edge at the $\overline{\text{RES}}$ pin. When the reference clock (CLOCK) is applied, the PLL starts to synchronize.

The 15.36 MHz clock can also be provided externally at pin CL15 without making use of the internal PLL. In this mode the pin XIN must be tied to either VDD or GND. An internal power-on-reset circuitry assures that the pin CL15 is an input until a 15.36 MHz clock is detected at the output of the PLL/oscillator.

To enable error-free data transport to/from the Quad IEC DFE-T/Q, the clocks DCL and FSC from the IOM®-2-interface must be synchronous to the 15.36 MHz signal. Therefore it is recommended to use the same signal for FSC and as input to CLOCK pin at the IEC-4-AFE-X Version 3.2 when the internal PLL is used to generate the 15.36 MHz clock.

If another clock source is used for CLOCK, e.g. the 2048 kHz DCL, a common time base must be guaranteed. This is usually achieved if FSC is derived from DCL by dividing it directly by 256.

Any constant phase difference between the time bases of both clocks is possible, but the devices have currently been qualified and released only for using the same FSC signal for the Quad IEC DFE-T/Q and for IEC-4-AFE-X Version 3.2.

3.2.1 Specification of the PLL and the 15.36 MHz Master Clock (Pin CL15)

The PLL is based on a crystal connected to the pins XIN and XOUT. For synchronization of the 15.36 MHz clock up to 16 internal capacitances are connected to XIN and XOUT.

The loop filter of the PLL is of second order, therefore a sinusoidal input jitter with the angular frequency $\omega = 2\pi f$ at CLOCK is attenuated by the PLL according to the following formula:

$$H(j\omega) = [(2\delta/\omega_r)j\omega + 1] / [(j\omega/\omega_r)^2 + (2\delta/\omega_r)j\omega + 1]$$

$H(j\omega)$ is the complex jitter transfer factor

$\omega_r = 2\pi f_r$ is the angular resonance frequency of the PLL

δ is the damping factor of the PLL

The maximum phase difference between the external CLOCK and the internal reference, derived from the master clock, due to a sinusoidal input jitter with the angular frequency ω is given as $1 - H(j\omega)$. The magnitude of the jitter transfer function and of the phase difference are illustrated below:

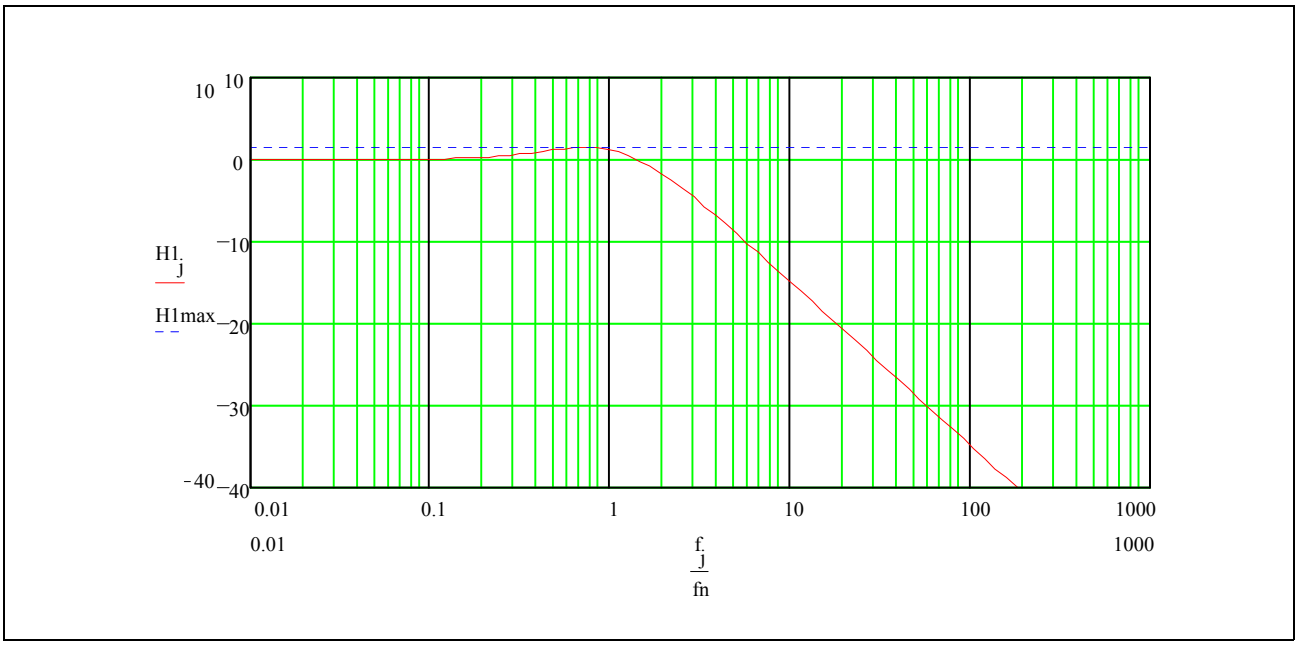

Figure 5 Jitter Transfer Gain in dB

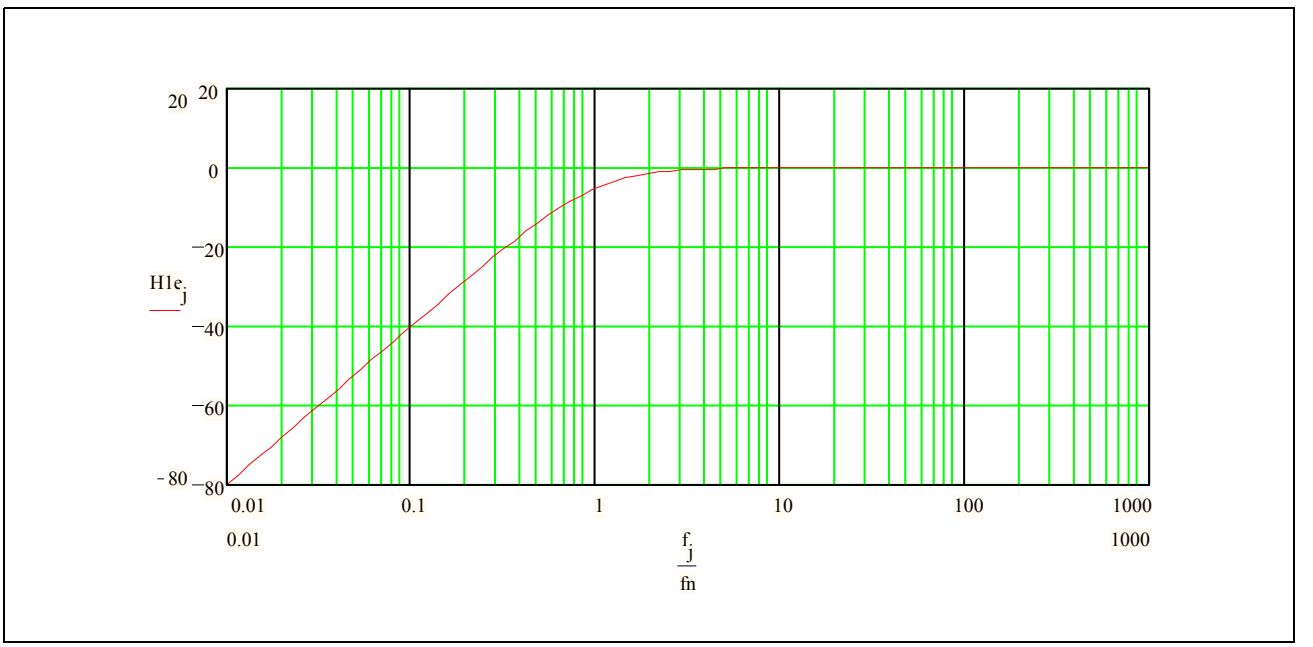

Figure 6 Maximum Phase Difference Due to Sinusoidal Input Jitter

If the input signal at pin CLOCK disappears being stuck to high or low, the PLL continues to generate the CL15 clock. In this case the PLL keeps the last setting. The accuracy of the frequency of CL15 degenerates in the long term only due to changes in temperature and ageing.

The resonance frequency can be set to two different values using the pin PLLF. PLLF tied to low sets the PLL to a low resonance frequency suited for applications in the

Access Network. PLLF tied to high or left open results in a higher resonance frequency for accelerated synchronization. The PLLF pin has an internal pull-up resistor.

The PLL automatically determines whether the frequency at pin CLOCK is 8 kHz or 2048 kHz.

Table 4 PLL Characteristics

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
f_r resonance frequency, PLLF = low	1.7	2.0	2.3	Hz
f_r resonance frequency, PLLF = high	7	8	9	Hz
Damping factor	0.7	0.9	1.2	
H_{max} maximum jitter amplification	0.9	1.45	2.2	dB
Synchronization time of the PLL after power on and applying the reference at pin CLOCK, PLLF = low			8	sec
Synchronization time of the PLL after power on and applying the reference at pin CLOCK, PLLF = high			1	sec
Output Jitter at CL15 without any jitter in the CLOCK signal (peak-to-peak); jitter frequency > 800 Hz			2	ns
Output Jitter at CL15 without any jitter in the CLOCK signal (peak-to-peak) jitter frequency < 20 Hz			80	ns
Initial accuracy after the loss of the reference clock at CLOCK			0.5	ppm
Initial accuracy after power on	-50		50	ppm
Start-up time of the oscillator with the crystal suggested below.		0.5	1	ms

Table 4 PLL Characteristics (cont'd)

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Output current at XOUT during start-up		0.5	1	mA
Output current at XOUT after synchronization		0.5	1	mA

Table 5 PLL Input Requirements

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Accuracy of the reference at CLOCK to enable synchronization	-150	0	+150	ppm
Peak-to peak Jitter of the CLOCK signal during any 125 µs period			70	ns
Peak-to-peak voltage of a sinusoidal external master clock provided at XIN	3.3			V_{pp}
Low time of the reference at CLOCK	130			ns
High time of the reference at CLOCK	130			ns
Pulse width of the 15 MHz clock	26		39	ns

3.2.2 Specification of the Crystal

A crystal (serial resonance) has to be connected to XIN and XOUT which shall meet the following specification:

Table 6 Specification of the Crystal

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Nominal frequency		15.360000		MHz
Total frequency range	-150		+150	ppm

Table 6 Specification of the Crystal (cont'd)

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Operating frequency C_{Load} = 15 pF C_{Load} = 7 pF	15.35770		 15.36230	 MHz MHz
Current		1	2	mA
Load capacitance	9.8		10.2	pF
Overall tolerance Δf/f			60	ppm
Resonance resistance R_r		30		Ω
Shunt capacitance C_0			7	pF
Motional capacitance C_1	25			fF
Overall pullability	± 210			ppm

Note that the load capacitors are integrated in the IEC-4-AFE-X Version 3.2. No additional capacitance has to be connected neither to XIN nor to XOUT. The crystal specifications shall meet the requirements given in **Table 6**.

A suitable type of crystal would be:

Vibrator:

Mode of vibration	DS	fundamental
Crystal cut	ATI	

Application hint: Parasitic capacitances at XIN and XOUT pin, e.g. due to board capacitances should be below 3 pF.

3.3 Analog Line Port

The IEC-4-AFE-X Version 3.2 chip gives access to four line ports. The signal to be transmitted is issued differentially at pins AOUT0..3 and BOUT0..3. The input is differentially sampled at AIN0..3 and BIN0..3. Each line port consists of three main function blocks (see **Figure 4**):

- The analog-to-digital converter in the receive path
- The digital-to-analog converter in the transmit path
- The output filter in the transmit path

Furthermore a line port contains some special functions. These are:

- Analog test loop-back
- Level detect function