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Data Sheet, DS 1, Feb. 2003

SBCX-X

S/T Bus Interface Circuit Extended

PEB 3081, Version 1.4

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Data Sheet

Revision History: **2003-02-04** DS 1

Previous Version: Data Sheet, DS1, V1.3, 2000-07-21

Page	Subjects (major changes since last revision)
Chapter 1	Comparison SBCX/SBCX-X
Chapter 3.3.6.2	S- Transceiver Synchronization New
Chapter 3.3.10	Test Functions extended
Chapter 3.7.1.1	CDA Handler Description extended
Chapter 3.7.5.1	TIC Bus Access Control: Note added
Chapter 5.6	IOM-2 Interface Timing: Explanation added
Chapter 5.9	S-Transceiver
Chapter 5.10	Recommended Transformer Specification: Changed
Chapter 5.11	Line Overload Protection added
Chapter 5.12	EMC/ESD added

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1 Overview

The S/T Bus Interface Circuit Extended (SBCX-X) implements the four-wire S/T interface used to link voice/data ISDN terminals, network terminators and PBX trunk lines to a central office. It is based on the SBCX PEB 2081, and provides enhanced features and functionality.

The SBCX-X provides the electrical and functional link between the analog S/T interface (compliant to the ITU recommendation I.430) and the IOM-2 interface.

It provides an S/T interface operating in TE, LT-T, LT-S, NT and intelligent NT modes, a serial control interface (SCI) for host programming, three general purpose I/O pins and one LED output which is capable to indicate the activation status of the S-interface automatically or can be programmed by the host.

The SBCX-X is produced in advanced CMOS technology.

Table 1 Comparison of the SBCX-X with the Previous Version SBCX

	SBCX-X PEB 3081	**SBCX PEB 2081**
Operating modes	TE, LT-T, LT-S, NT, Int. NT	TE, LT-T, LT-S, NT
Supply voltage	3.3 V ± 5%	5 V ± 5%
Technology	CMOS	CMOS
Package	P-MQFP-44 / P-TQFP-48	P-LCC-28 / P-DIP-28
Transceiver Transformer ratio for the transmitter receiver	 1:1 1:1	 2:1 2:1
Test Functions	- Analog loop (LP_A - bit EXLP - bit, ARL)	- Analog loop (ARL)
Microcontroller Interface	Serial interface (SCI)	Not provided
Host programming	SCI or MON channel (MONITOR slave mode)	MON channel (MONITOR slave mode)
Command structure of the register access	Header/address/data	Address/data
Crystal	7.68 MHz	7.68 MHz
Buffered 7.68 MHz output	Provided	Not provided

Table 1 Comparison of the SBCX-X with the Previous Version SBCX (cont'd)

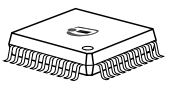
	SBCX-X PEB 3081	SBCX PEB 2081
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Not provided
Data control and manipulation	Various possibilities of data control and data manipulation (enable/disable, shifting, looping, switching)	Shifting B-channel to channel 0 and direction control
Auxiliary Interface	AUX0-2 (general purpose I/Os)	MAI0-7 (general purpose I/Os and several mode dependent functions)
IOM channel select (LT modes)	Channel select pins multiplexed on AUX0-2	X0-2
LED pin	$\overline{\text{ACL}}$ (host controlled or automatic indication of layer 1 activated state)	Not provided
Output pin for D-channel active indication	Provided	Not provided
Control input pin for D-channel inhibit	Provided	Not provided
Stop/Go bit output pin	Provided	Provided
IOM-2		
IOM-2 Interface	Double clock (DCL), bit clock (BCL), serial data strobe 1 (SDS1) serial data strobe 2 (SDS2)	Double clock (DCL), bit clock (BCL)
Monitor channel programming	Provided (MON0, 1, 2, ..., 7)	Provided (MON0 or 1)
C/I channels	CI0 (4 bit), CI1 (4/6 bit)	CI0 (4 bit), CI1 (6 bit)

Table 1 Comparison of the SBCX-X with the Previous Version SBCX (cont'd)

	SBCX-X PEB 3081	SBCX PEB 2081
Layer 1 state machine	With changes for correspondence with the actual ITU specification	
Layer 1 state machine in software	Possible	Not possible
Reset Signals	$\overline{\text{RES}}$ input signal $\overline{\text{RSTO}}$ output signal	$\overline{\text{RST}}$ input signal
Reset Sources	$\overline{\text{RES}}$ Input Watchdog C/I Code Change $\overline{\text{EAW}}$ Pin Software Reset	$\overline{\text{RST}}$ Input C/I Code Change
Interrupt Output Signals	$\overline{\text{INT}}$ low active (open drain) by default, reprogrammable to high active (push-pull)	Not provided
Pin SCLK	1.536 MHz	512 kHz

Version 1.4

1.1 Features



P-MQFP-44

P-TQFP-48

- Full duplex 2B + D S/T interface transceiver according to ITU-T I.430
- Successor of SBCX PEB 2081 in 3.3 V technology
- Conversion of the frame structure between the S/T-interface and IOM-2
- IOM-2 interface supporting TE, LT-T, LT-S, NT and intelligent NT modes
- Single and double clocks on IOM-2
- Two serial data strobe signals
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface
- Adaptively switched receive thresholds
- 3 general purpose I/O pins multiplexed with channel select pins
- Three pins for D-channel active indication, Stop/Go bit output and E-bit control on S
- One programmable timer
- Watchdog timer
- Software Reset
- One LED pin automatically indicating layer 1 activated state
- Test loops
- Sophisticated power management for restricted power mode

Type	Package
PEB 3081 H	P-MQFP-44
PEB 3081 F	P-TQFP-48

- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

1.2 Logic Symbol

The logic symbol gives an overview of the SBCX-X functions. It must be noted that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.

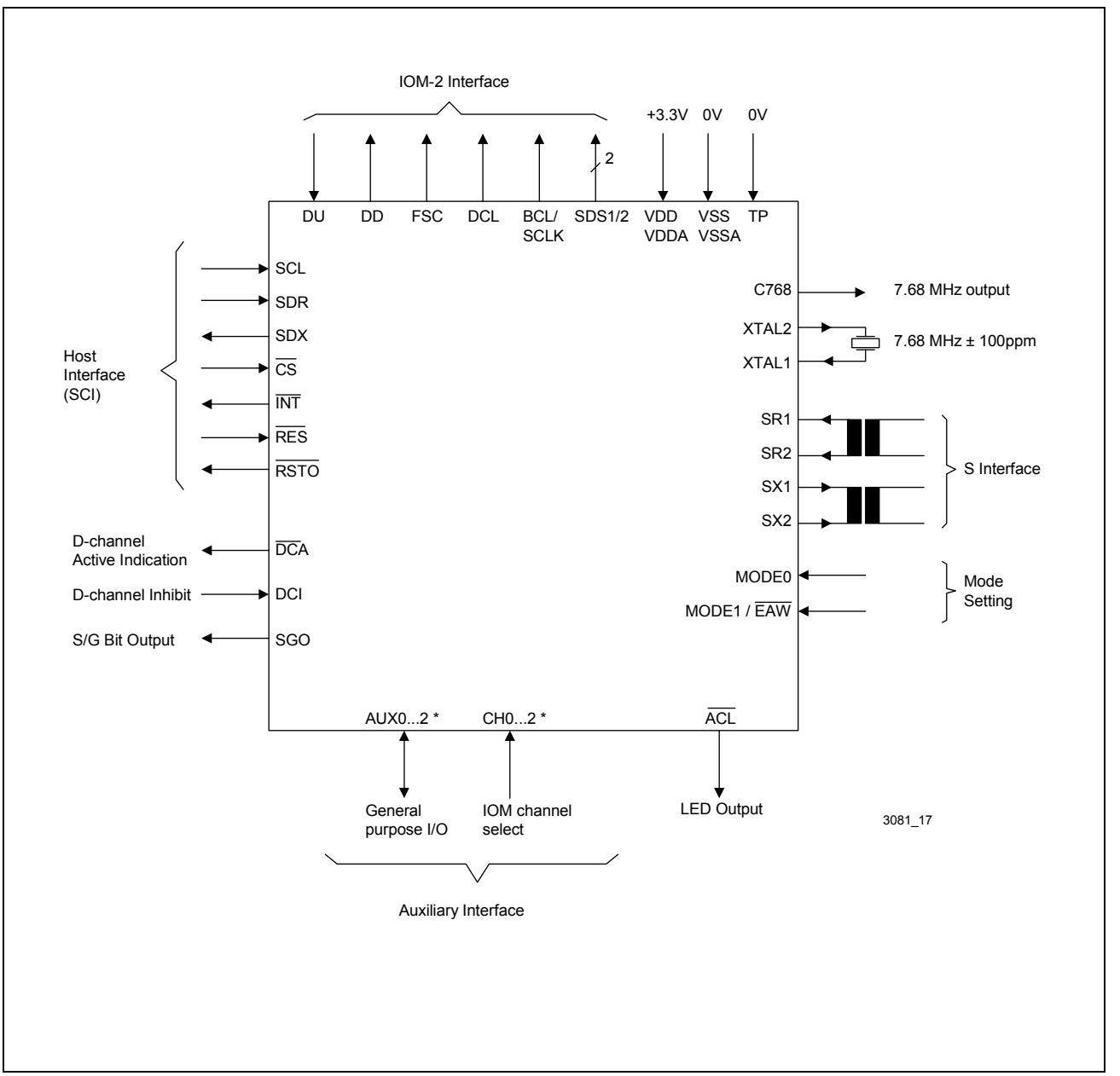


Figure 1 Logic Symbol of the SBCX-X

1.3 Typical Applications

The SBCX-X is designed for the user area of the ISDN basic access. By programming the corresponding operating mode it may be used at both ends of these interfaces.

Figure 2 illustrates the general application fields of the SBCX-X:

- ISDN terminals (TE mode)
- ISDN network termination (NT) for a link between the S/T interface and the U interface
- ISDN subscriber line termination (LT-S)
- ISDN trunk line termination (LT-T), i.e. PBX connection to central office

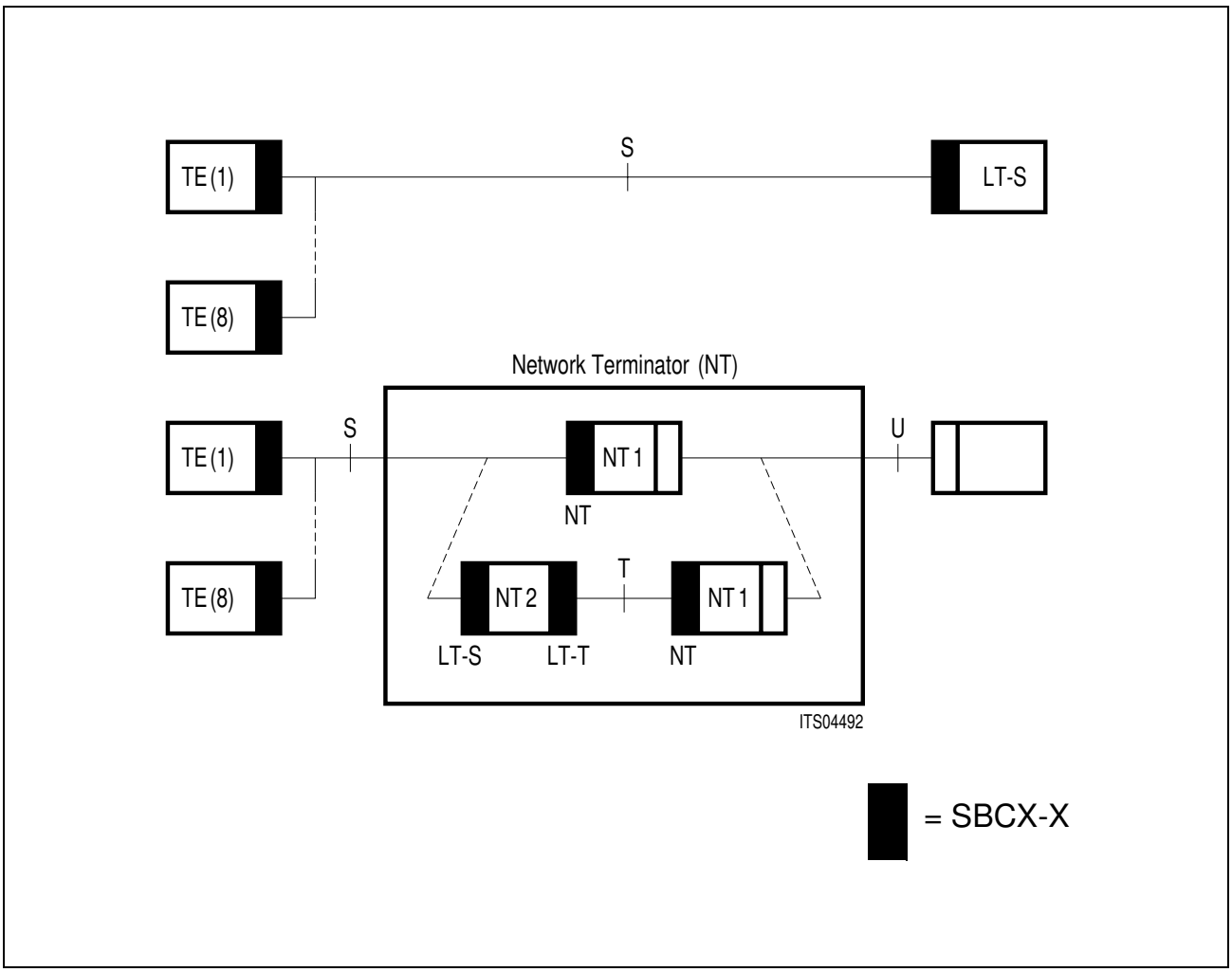


Figure 2 Applications of the SBCX-X

2 Pin Configuration

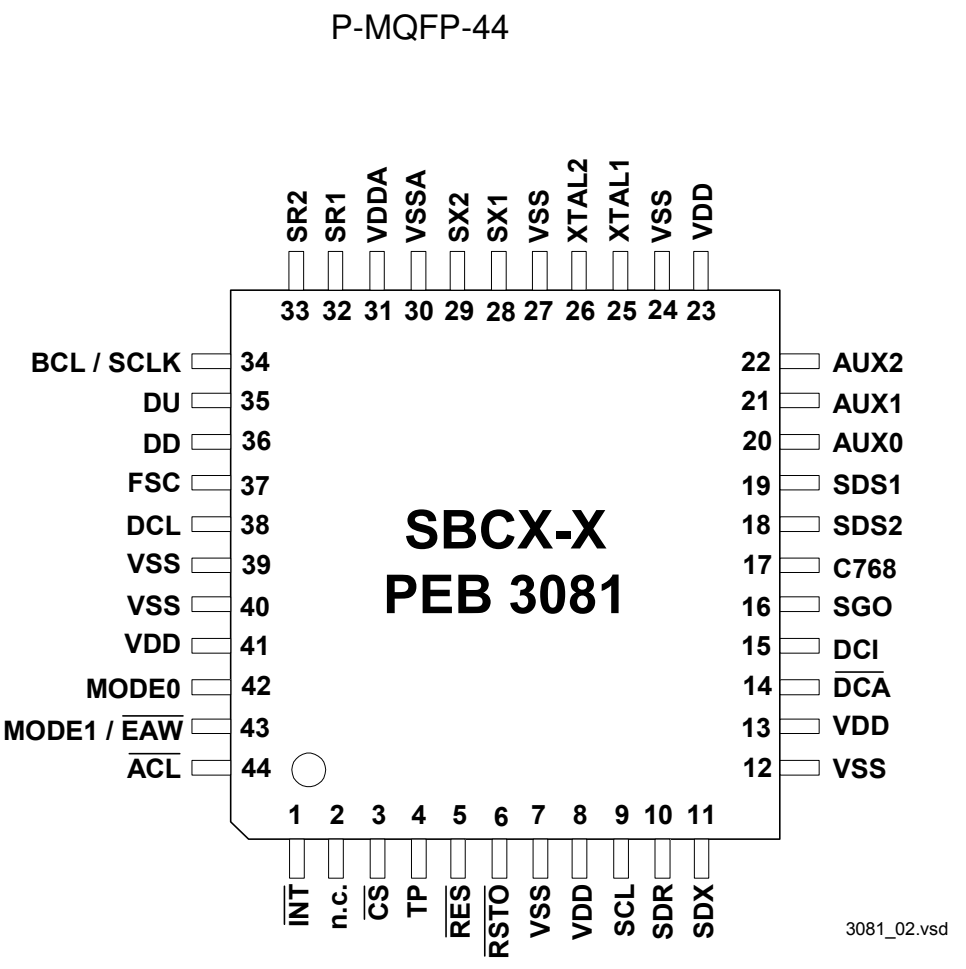


Figure 3 Pin Configuration of the SBCX-X (P-MQFP-44)

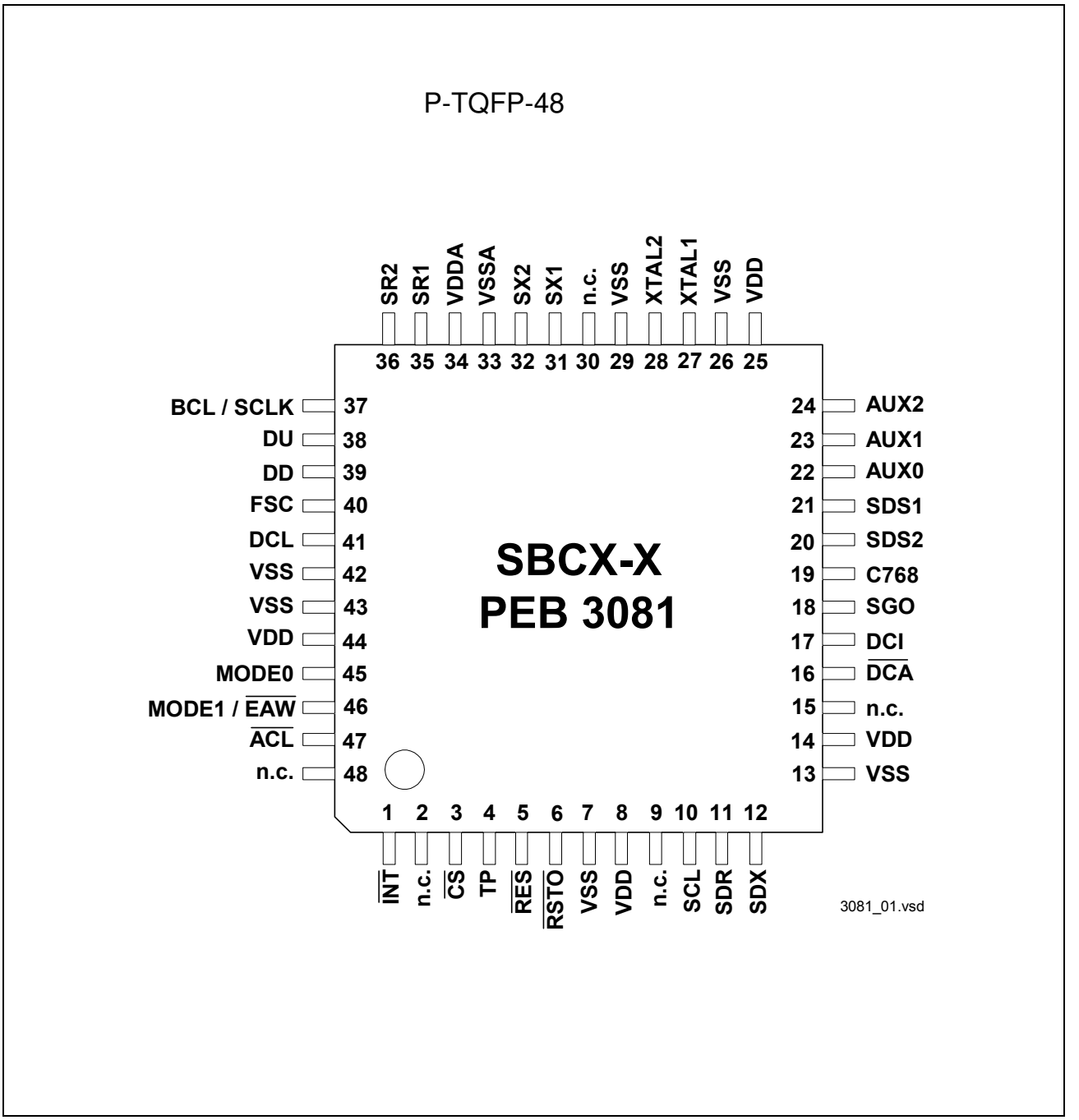


Figure 4 Pin Configuration of the SBCX-X (P-TQFP-48)

Table 2 SBCX-X Pin Definitions and Functions

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	TQFP-48			
Host Interface				
9	10	SCL	I	**SCL - Serial Clock** Clock signal of the SCI interface if a serial interface is selected.
10	11	SDR	I	**SDR - Serial Data Receive** Receive data line of the SCI interface if a serial interface is selected.
11	12	SDX	OD	**SDX - Serial Data Transmit** Transmit data line of the SCI interface if a serial interface is selected.
3	3	CS	I	**Chip Select** A low level indicates a microcontroller access to the SBCX-X.
1	1	INT	O (OD)	**Interrupt Request** $\overline{\text{INT}}$ becomes active (low) if the SBCX-X requests an interrupt (open drain characteristic). The polarity can be reprogrammed to high active with push-pull characteristic.
5	5	RES	I	**Reset** A LOW on this input forces the SBCX-X into a reset state.
IOM-2 Interface				
37	40	FSC	I/O	**Frame Sync** 8-kHz frame synchronization signal.
38	41	DCL	I/O	**Data Clock** IOM-2 interface clock signal (double clock, e.g. 1.536 MHz in TE mode).

Table 2 SBCX-X Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	**TQFP-48**			
34	37	BCL/ SCLK	O	**Bit Clock/S-Clock** **TE-Mode:** Bit clock output, identical to IOM-2 data rate (DCL/2). **LT-T Mode:** 1.536 MHz output synchronous to S-interface. **NT / LT-S Mode:** Bit clock output derived from the DCL input clock divided by 2.
36	39	DD	I/O (OD)	**Data Downstream** IOM-2 data signal in downstream direction.
35	38	DU	I/O (OD)	**Data Upstream** IOM-2 data signal in upstream direction.
19	21	SDS1	O	**Serial Data Strobe 1** Programmable strobe signal for time slot and/or D-channel indication on IOM-2.
18	20	SDS2	O	**Serial Data Strobe 2** Programmable strobe signal for time slot and/or D-channel indication on IOM-2.

Miscellaneous

28 29	31 32	SX1 SX2	O O	**S-Bus Transmitter Output (positive)** **S-Bus Transmitter Output (negative)**
32 33	35 36	SR1 SR2	I I	**S-Bus Receiver Input** **S-Bus Receiver Input**
25	27	XTAL1	I	**Crystal 1** Connection for a crystal or used as external clock input. 7.68 MHz clock or crystal required.
26	28	XTAL2	O	**Crystal 2** Connection for a crystal. Not connected if an external clock is supplied to XTAL1

Table 2 SBCX-X Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	**TQFP-48**			
20 21 22	22 23 24	AUX0 AUX1 AUX2	I/O (OD) I/O (OD) I/O (OD)	**TE-Mode:** **Auxiliary Port 0 - 2 (input/output)** These pins are individually programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. **LT-T/LT-S/NT Mode:** **CH0-2 - IOM-2 Channel Select (input)** These pins select one of eight channels on the IOM-2 interface.
42	45	MODE0	I	**Mode 0 Select** A LOW selects TE-mode and a HIGH selects LT-T / LT-S mode (see MODE1/ $\overline{\text{EAW}}$).
43	46	MODE1 EAW	I I	The pin function depends on the setting of MODE0. If MODE0=1: **Mode 1 Select** A LOW selects LT-T mode and a HIGH selects LT-S mode. If MODE0=0: **External Awake** If a falling edge on this input is detected, the SBCX-X generates an interrupt and, if enabled, a reset pulse.
6	6	RSTO	OD	**Reset Output** Low active reset output, either from a watchdog timeout or programmed by the host.
17	19	C768	O	**Clock Output** A 7.68 MHz clock is output to support other devices. This clock is not synchronous to the S interface.
14	16	DCA	O	**DCA - D-Channel Active Indication** This pin provides an output of the D-channel bits on the S-bus receive line.

Table 2 SBCX-X Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	**TQFP-48**			
15	17	DCI	I	**DCI - D-Channel Inhibit** If this bit is set to '1' the E-bits are inverted, i.e. the D-channel is blocked (only in NT/LT-S mode). This pin has the same function as the D-channel inhibit bit (see TR_MODE.DCH_INH).
16	18	SGO	O	**SGO - Stop/Go Bit Output** A S/G bit output with programmable polarity and length (TR_CONF2 register) is provided.
44	47	ACL	O	**Activation LED** This pin can either function as a programmable output or it can automatically indicate the activated state of the S interface by a logic '0'. An LED with pre-resistance may directly be connected to $\overline{\text{ACL}}$.
4	4	TP	I	**Test Pin** Must be connected to V_{SS}.
2	2, 9, 15, 30, 48	n.c.		**Not Connected**
Power Supply				
8, 13, 23, 41	8, 14, 25, 44	V_{DD}	–	**Digital Power Supply Voltage** (3.3 V ± 5 %)
31	34	V_{DDA}	–	**Analog Power Supply Voltage** (3.3 V ± 5 %)
7, 12, 24, 27, 39, 40	7, 13, 26, 29, 42, 43	V_{SS}	–	**Digital Ground** (0 V)
30	33	V_{SSA}	–	**Analog Ground** (0 V)

3 Description of Functional Blocks

3.1 General Functions and Device Architecture

Figure 5 shows the architecture of the SBCX-X containing the following functions:

- S/T-interface transceiver supporting TE, LT-T, LT-S, NT and intelligent NT modes
- Serial Control Interface (SCI)
- IOM-2 interface for terminal, linecard and NT applications, with single/double clock
- Two serial data strobe signals
- IOM handler with controller data access registers (CDA) allows flexible access to IOM timeslots for reading/writing, looping and shifting data
- Synchronous transfer interrupts (STI) allow controlled access to IOM timeslots
- MONITOR channel handler on IOM-2 for master mode, slave mode or data exchange
- C/I-Channel handler
- D-channel access mechanism
- 3-pin auxiliary port for general purpose I/O pins or channel select pins
- LED connected to pin $\overline{\text{ACL}}$ indicates S-interface activation status automatically or can be controlled by the host
- Output for D-channel active indication (output of received D-bits on S)
- Stop/Go bit output with programmable polarity and length
- D-channel inhibit input pin to control inversion of E-bits on S to block other terminals
- Level detect circuit on the S interface reduces power consumption in power down mode
- Timer for periodic or single interrupts
- Clock and timing generation
- Digital PLL to synchronize the transceiver to the S/T interface
- Buffered 7.68 MHz oscillator clock output allows connection of further devices and saves another crystal on the system board
- Reset generation (watchdog timer)

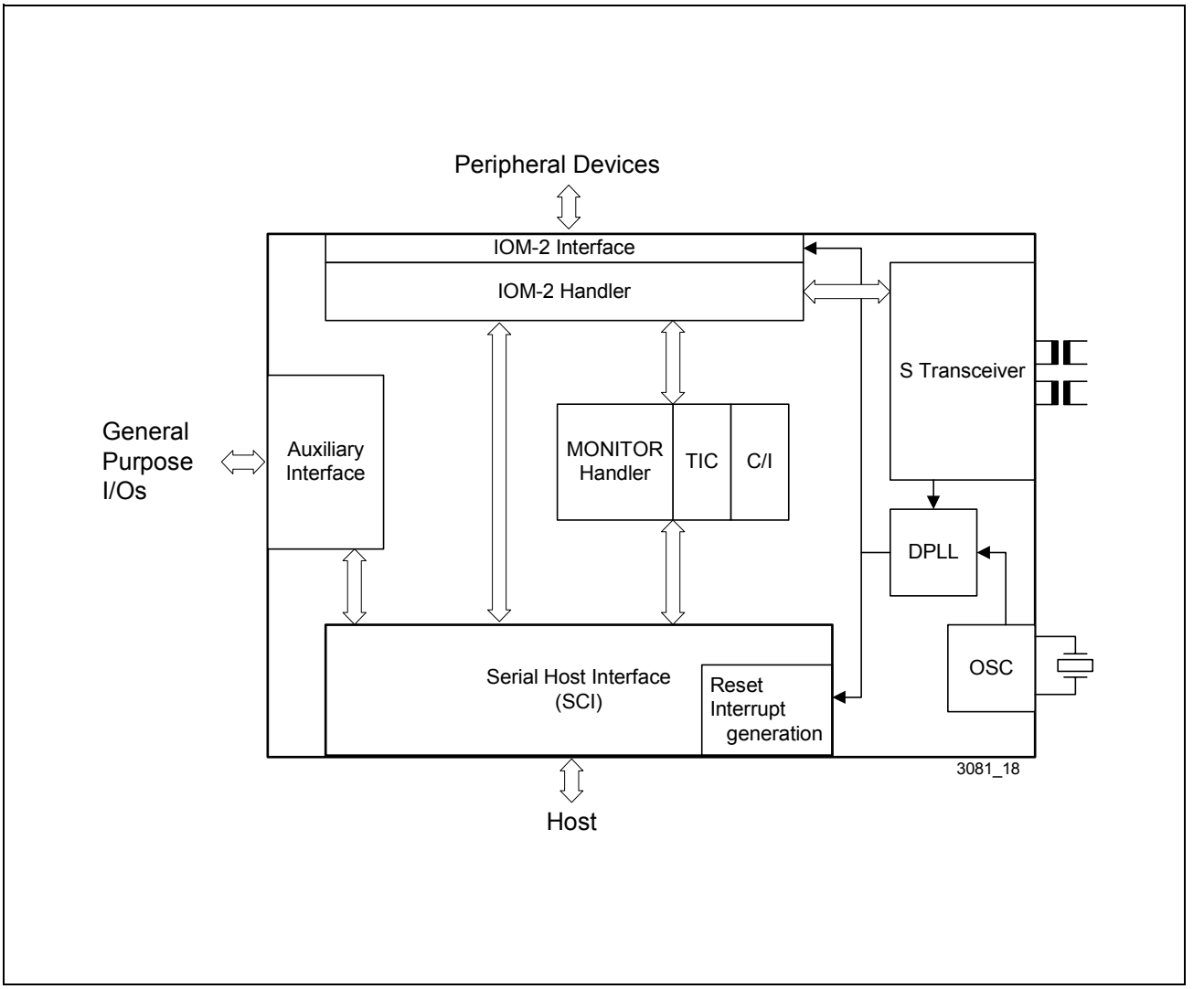


Figure 5 Functional Block Diagram of the SBCX-X

3.2 Microcontroller Interface

The SBCX-X supports a serial micrcontroller interface. For applications where no controller is connected to the SBCX-X programming is done via the IOM-2 MONITOR channel from a master device. In such applications the SBCX-X operates in the IOM-2 slave mode (refer to the corresponding chapter of the IOM-2 MONITOR handler). This mode is suitable for control functions (e.g. programming registers of the S/T transceiver), but the bandwidth is not sufficient to transfer B- and D-channel data.

The interface selection is done by pinstrapping of the chip select signal $\overline{CS}$ (see **Table 3**). The selection pins are evaluated when the reset input $\overline{RES}$ is active. For the pin levels stated in the table the following is defined:

'High': dynamic pin; value must be 'High' only during reset
V_{SS}: static pin; pin must statically be strapped to 'Low' level

Table 3 Host Interface Selection

CS	Interface Mode
'High'	Serial Control Interface (SCI)
V_{SS}	IOM-2 MONITOR Channel (Slave Mode)

The interfaces contain all circuitry necessary for the access to programmable registers. The mapping of all these registers can be found in **Chapter 4**.
The microcontroller interface also provides an interrupt request at pin $\overline{INT}$ which is low active by default but can be reprogrammed to high active, a reset input pin $\overline{RES}$ and a reset output pin $\overline{RSTO}$.
The interrupt request pin $\overline{INT}$ becomes active if the SBCX-X requests an interrupt and this can occur at any time.