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SBCX-X

S/T Bus Interface Circuit Extended
PEB 3081, Version 1.4

Wired
Communications



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Table of Contents		Page
1	Overview	11
1.1	Features	14
1.2	Logic Symbol	15
1.3	Typical Applications	16
2	Pin Configuration	17
3	Description of Functional Blocks	23
3.1	General Functions and Device Architecture	23
3.2	Microcontroller Interface	25
3.2.1	Serial Control Interface (SCI)	26
3.2.2	Programming Sequences	27
3.2.3	Interrupt Structure	29
3.2.4	Reset Generation	31
3.2.5	Timer Modes	33
3.2.6	Activation Indication via Pin ACL	35
3.3	S/T-Interface	36
3.3.1	S/T-Interface Coding	38
3.3.2	S/T-Interface Multiframeing	40
3.3.3	Data Transfer and Delay between IOM-2 and S/T	42
3.3.4	Transmitter Characteristics	45
3.3.5	Receiver Characteristics	46
3.3.6	S/T Interface Circuitry	47
3.3.6.1	External Protection Circuitry	47
3.3.6.2	S-Transceiver Synchronization	49
3.3.7	S/T Interface Delay Compensation (TE/LT-T Mode)	50
3.3.8	Level Detection Power Down	50
3.3.9	Transceiver Enable/Disable	50
3.3.10	Test Functions	51
3.4	Clock Generation	53
3.4.1	Description of the Receive PLL (DPLL)	56
3.4.2	Jitter	56
3.4.3	Oscillator Clock Output C768	57
3.5	Control of Layer-1	58
3.5.1	State Machine TE and LT-T Mode	60
3.5.1.1	State Transition Diagram (TE, LT-T)	60
3.5.1.2	States (TE, LT-T)	62
3.5.1.3	C/I Codes (TE, LT-T)	64
3.5.1.4	Infos on S/T (TE, LT-T)	66
3.5.2	State Machine LT-S Mode	67
3.5.2.1	State Transition Diagram (LT-S)	67
3.5.2.2	States (LT-S)	68
3.5.2.3	C/I Codes (LT-S)	69

Table of Contents		Page
3.5.2.4	Infos on S/T (LT-S)	70
3.5.3	State Machine NT Mode	71
3.5.3.1	State Transition Diagram (NT)	71
3.5.3.2	States (NT)	72
3.5.3.3	C/I Codes (NT)	73
3.5.4	Command / Indicate Channel Codes (C/I0) - Overview	75
3.6	Control Procedures	76
3.6.1	Example of Activation/Deactivation	76
3.6.2	Activation initiated by the Terminal	77
3.6.3	Activation initiated by the Network Termination NT	78
3.7	IOM-2 Interface	79
3.7.1	IOM-2 Handler	82
3.7.1.1	Controller Data Access (CDA)	84
3.7.2	Serial Data Strobe Signal and Strobed Data Clock	94
3.7.2.1	Serial Data Strobe Signal	94
3.7.2.2	Strobed IOM-2 Bit Clock	96
3.7.3	IOM-2 Monitor Channel	97
3.7.3.1	Handshake Procedure	98
3.7.3.2	Error Treatment	101
3.7.3.3	MONITOR Channel Programming as a Master Device	103
3.7.3.4	MONITOR Channel Programming as a Slave Device	103
3.7.3.5	MONITOR Time-Out Procedure	104
3.7.3.6	MONITOR Interrupt Logic	105
3.7.4	C/I Channel Handling	106
3.7.5	D-Channel Access Control	107
3.7.5.1	TIC Bus D-Channel Access Control	108
3.7.5.2	S-Bus Priority Mechanism for D-Channel	110
3.7.5.3	S-Bus D-Channel Control in LT-T	112
3.7.5.4	D-Channel Control in the Intelligent NT (TIC- and S-Bus)	112
3.7.6	Activation/Deactivation of IOM-2 Interface	116
3.8	Auxiliary Interface	118
4	Detailed Register Description	120
4.1	Transceiver and C/I Registers	126
4.1.1	TR_MODE2 - Transceiver Mode Register 2	126
4.1.2	CIR0 - Command/Indication Receive 0	127
4.1.3	CIX0 - Command/Indication Transmit 0	128
4.1.4	CIR1 - Command/Indication Receive 1	128
4.1.5	CIX1 - Command/Indication Transmit 1	129
4.1.6	TR_CONF0 - Transceiver Configuration Register 0	129
4.1.7	TR_CONF1 - Transceiver Configuration Register 1	131
4.1.8	TR_CONF2 - Transmitter Configuration Register 2	131
4.1.9	TR_STA - Transceiver Status Register	133

Table of Contents		Page
4.1.10	TR_CMD - Transceiver Command Register	134
4.1.11	SQRR1 - S/Q-Channel Receive Register 1	135
4.1.12	SQXR1- S/Q-Channel TX Register 1	136
4.1.13	SQRR2 - S/Q-Channel Receive Register 2	136
4.1.14	SQXR2 - S/Q-Channel TX Register 2	137
4.1.15	SQRR3 - S/Q-Channel Receive Register 3	137
4.1.16	SQXR3 - S/Q-Channel TX Register 3	137
4.1.17	ISTATR - Interrupt Status Register Transceiver	137
4.1.18	MASKTR - Mask Transceiver Interrupt	138
4.1.19	TR_MODE - Transceiver Mode Register 1	139
4.2	Auxiliary Interface Registers	140
4.2.1	ACFG1 - Auxiliary Configuration Register 1	140
4.2.2	ACFG2 - Auxiliary Configuration Register 2	140
4.2.3	AOE - Auxiliary Output Enable Register	141
4.2.4	ARX - Auxiliary Interface Receive Register	141
4.2.5	ATX - Auxiliary Interface Transmit Register	142
4.3	IOM-2 and MONITOR Handler	142
4.3.1	CDAXy - Controller Data Access Register xy	142
4.3.2	XXX_TSDPxy - Time Slot and Data Port Selection for CHxy	143
4.3.3	CDAX_CR - Control Register Controller Data Access CH1x	144
4.3.4	TR_CR - Control Register Transceiver Data (IOM_CR.CI_CS=0) ...	145
4.3.5	TRC_CR - Control Register Transceiver C/I0 (IOM_CR.CI_CS=1) ...	146
4.3.6	DCI_CR - Control Register for CI1 Handler (IOM_CR.CI_CS=0) ...	146
4.3.7	DCIC_CR - Control Register for CI0 Handler (IOM_CR.CI_CS=1) ...	147
4.3.8	MON_CR - Control Register Monitor Data	148
4.3.9	SDSx_CR - Control Register Serial Data Strobe x	149
4.3.10	IOM_CR - Control Register IOM Data	150
4.3.11	STI - Synchronous Transfer Interrupt	152
4.3.12	ASTI - Acknowledge Synchronous Transfer Interrupt	153
4.3.13	MSTI - Mask Synchronous Transfer Interrupt	153
4.3.14	SDS_CONF - Configuration Register for Serial Data Strokes	154
4.3.15	MCDA - Monitoring CDA Bits	155
4.3.16	MOR - MONITOR Receive Channel	155
4.3.17	MOX - MONITOR Transmit Channel	155
4.3.18	MOSR - MONITOR Interrupt Status Register	156
4.3.19	MOCR - MONITOR Control Register	156
4.3.20	MSTA - MONITOR Status Register	157
4.3.21	MCONF - MONITOR Configuration Register	157
4.4	Interrupt and General Configuration	158
4.4.1	ISTA - Interrupt Status Register	158
4.4.2	MASK - Mask Register	159
4.4.3	AUXI - Auxiliary Interrupt Status Register	159

Table of Contents		Page
4.4.4	AUXM - Auxiliary Mask Register	160
4.4.5	MODE1 - Mode1 Register	160
4.4.6	MODE2 - Mode2 Register	162
4.4.7	ID - Identification Register	163
4.4.8	SRES - Software Reset Register	163
4.4.9	TIMR - Timer Register	164
5	Electrical Characteristics	165
5.1	Absolute Maximum Ratings	165
5.2	DC Characteristics	166
5.3	Capacitances	166
5.4	Oscillator Specification	168
5.5	AC Characteristics	169
5.6	IOM-2 Interface Timing	169
5.7	Serial Control Interface (SCI) Timing	172
5.8	Reset	173
5.9	S-Transceiver	174
5.10	Recommended Transformer Specification	175
5.11	Line Overload Protection	176
5.12	EMC / ESD Aspects	177
6	Package Outlines	178
7	Appendix	180

List of Figures		Page
Figure 1	Logic Symbol of the SBCX-X	15
Figure 2	Applications of the SBCX-X	16
Figure 3	Pin Configuration of the SBCX-X (P-MQFP-44)	17
Figure 4	Pin Configuration of the SBCX-X (P-TQFP-48)	18
Figure 5	Functional Block Diagram of the SBCX-X	24
Figure 6	Serial Control Interface Timing	26
Figure 7	Serial Control Interface Timing	27
Figure 8	Interrupt Status and Mask Registers	30
Figure 9	Reset Generation	31
Figure 10	Timer Interrupt Status Registers	33
Figure 11	Timer Register	34
Figure 12	ACL Indication of Activated Layer 1 on TE Side	35
Figure 13	ACL Configuration	35
Figure 14	Wiring Configurations in User Premises	37
Figure 15	S/T-Interface Line Code	38
Figure 16	Frame Structure at Reference Points S and T (ITU I.430)	39
Figure 17	Data Delay between IOM-2 and S/T Interface (TE mode only)	42
Figure 18	Data Delay between IOM-2 and S/T Interface with S/G Bit Evaluation (TE mode only)	43
Figure 19	Data Delay between IOM-2 and S/T Interface with 8 IOM Channels (LT-S/NT mode only)	44
Figure 20	Data Delay between IOM-2 and S/T Interface with 3 IOM Channels and Maximum Receive Delay (LT-S/NT mode only)	44
Figure 21	Equivalent Internal Circuit of the Transmitter Stage	45
Figure 22	Equivalent Internal Circuit of the Receiver Stage	46
Figure 23	Connection of Line Transformers and Power Supply to the SBCX-X	47
Figure 24	External Circuitry for Transmitter	48
Figure 25	External Circuitry for Symmetrical Receivers	48
Figure 26	External Circuitry for Symmetrical Receivers	49
Figure 27	Disabling of S/T Transmitter	51
Figure 28	External Loop at the S/T-Interface	52
Figure 29	Clock System of the SBCX-X	53
Figure 30	Phase Relationships of SBCX-X Clock Signals	56
Figure 31	Buffered Oscillator Clock Output	57
Figure 32	Layer-1 Control	58
Figure 33	State Diagram Notation	59
Figure 34	State Transition Diagram (TE, LT-T)	61
Figure 35	State Transition Diagram of Unconditional Transitions (TE, LT-T)	62
Figure 36	State Transition Diagram (LT-S)	67
Figure 37	State Transition Diagram (NT)	71
Figure 38	Example of Activation/Deactivation Initiated by the Terminal	76

List of Figures	Page
Figure 39	Example of Activation/Deactivation initiated by the Terminal (TE). Activation/Deactivation completely under Software Control 77
Figure 40	Example of Activation/Deactivation initiated by the Network Termination (NT). Activation/Deactivation completely under Software Control 78
Figure 41	IOM [™] -2 Frame Structure in Terminal Mode. 80
Figure 42	Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode 81
Figure 43	Architecture of the IOM Handler (Example Configuration). 83
Figure 44	Data Access via CDAX1 and CDAX2 Register Pairs 85
Figure 45	Examples for Data Access via CDAXy Registers. 86
Figure 46	Data Access when Looping TSa from DU to DD 87
Figure 47	Data Access when Shifting TSa to TSb on DU (DD) 88
Figure 48	Example for Monitoring Data 89
Figure 49	Interrupt Structure of the Synchronous Data Transfer 91
Figure 50	Examples for the Synchronous Transfer Interrupt Control with one Enabled STIxy 92
Figure 51	Data Strobe Signal. 95
Figure 52	Strobed IOM-2 Bit Clock. Register SDS_CONF Programmed to 01H. 96
Figure 53	Examples of MONITOR Channel Applications in IOM-2 TE Mode . . . 97
Figure 54	MONITOR Channel Protocol (IOM-2) 99
Figure 55	Monitor Channel, Transmission Abort Requested by the Receiver . . 102
Figure 56	Monitor Channel, Transmission Abort Requested by the Transmitter 102
Figure 57	Monitor Channel, Normal End of Transmission 102
Figure 58	MONITOR Interrupt Structure 105
Figure 59	CIC Interrupt Structure. 107
Figure 60	Applications of TIC Bus in IOM-2 Bus Configuration 108
Figure 61	Structure of Last Octet of Ch2 on DU 109
Figure 62	Structure of Last Octet of Ch2 on DD 110
Figure 63	D-Channel Access Control on the S-Interface. 111
Figure 64	Data Flow for Collision Resolution Procedure in Intelligent NT 115
Figure 65	Deactivation of the IOM-2 Interface 116
Figure 66	Activation of the IOM-2 interface 117
Figure 67	Register Mapping of the SBCX-X 120
Figure 68	Oscillator Circuits 168
Figure 69	Input/Output Waveform for AC Tests. 169
Figure 70	IOM-2 Timing (TE mode) 169
Figure 71	IOM-2 Timing (LT-S, LT-T, NT mode) 170
Figure 72	Definition of Clock Period and Width 171
Figure 73	SCI Interface 172
Figure 74	Reset Signal RES 173
Figure 75	Maximum Line Input Current 176
Figure 76	Transformer Circuitry 177

List of Tables		Page
Table 1	Comparison of the SBCX-X with the Previous Version SBCX.....	11
Table 2	SBCX-X Pin Definitions and Functions	19
Table 3	Host Interface Selection.....	25
Table 4	Header Byte Code	27
Table 5	Reset Source Selection	32
Table 6	SBCX-X Timer	33
Table 7	S/Q-Bit Position Identification and Multiframe Structure	40
Table 8	Clock Modes	54
Table 9	Examples for Synchronous Transfer Interrupts	91
Table 10	CDA Register Combinations with Correct Read/Write Access	93
Table 11	Transmit Direction	98
Table 12	Receive Direction.....	98
Table 13	SBCX-X Configuration Settings in Intelligent NT Applications.....	113
Table 14	AUX Pin Functions.....	118
Table 15	IOM-2 Channel Selection.....	119

1 Overview

The S/T Bus Interface Circuit Extended (SBCX-X) implements the four-wire S/T interface used to link voice/data ISDN terminals, network terminators and PBX trunk lines to a central office. It is based on the SBCX PEB 2081, and provides enhanced features and functionality.

The SBCX-X provides the electrical and functional link between the analog S/T interface (compliant to the ITU recommendation I.430) and the IOM-2 interface.

It provides an S/T interface operating in TE, LT-T, LT-S, NT and intelligent NT modes, a serial control interface (SCI) for host programming, three general purpose I/O pins and one LED output which is capable to indicate the activation status of the S-interface automatically or can be programmed by the host.

The SBCX-X is produced in advanced CMOS technology.

Table 1 Comparison of the SBCX-X with the Previous Version SBCX

	SBCX-X PEB 3081	SBCX PEB 2081
Operating modes	TE, LT-T, LT-S, NT, Int. NT	TE, LT-T, LT-S, NT
Supply voltage	3.3 V \pm 5%	5 V \pm 5%
Technology	CMOS	CMOS
Package	P-MQFP-44 / P-TQFP-48	P-LCC-28 / P-DIP-28
Transceiver Transformer ratio for the transmitter receiver	1:1 1:1	2:1 2:1
Test Functions	- Analog loop (LP_A - bit EXLP - bit, ARL)	- Analog loop (ARL)
Microcontroller Interface	Serial interface (SCI)	Not provided
Host programming	SCI or MON channel (MONITOR slave mode)	MON channel (MONITOR slave mode)
Command structure of the register access	Header/address/data	Address/data
Crystal	7.68 MHz	7.68 MHz
Buffered 7.68 MHz output	Provided	Not provided

Table 1 Comparison of the SBCX-X with the Previous Version SBCX (cont'd)

	SBCX-X PEB 3081	SBCX PEB 2081
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Not provided
Data control and manipulation	Various possibilities of data control and data manipulation (enable/disable, shifting, looping, switching)	Shifting B-channel to channel 0 and direction control
Auxiliary Interface	AUX0-2 (general purpose I/Os)	MAI0-7 (general purpose I/Os and several mode dependent functions)
IOM channel select (LT modes)	Channel select pins multiplexed on AUX0-2	X0-2
LED pin	ACL (host controlled or automatic indication of layer 1 activated state)	Not provided
Output pin for D-channel active indication	Provided	Not provided
Control input pin for D-channel inhibit	Provided	Not provided
Stop/Go bit output pin	Provided	Provided
IOM-2		
IOM-2 Interface	Double clock (DCL), bit clock (BCL), serial data strobe 1 (SDS1) serial data strobe 2 (SDS2)	Double clock (DCL), bit clock (BCL)
Monitor channel programming	Provided (MON0, 1, 2, ..., 7)	Provided (MON0 or 1)
C/I channels	CI0 (4 bit), CI1 (4/6 bit)	CI0 (4 bit), CI1 (6 bit)

Table 1 Comparison of the SBCX-X with the Previous Version SBCX (cont'd)

	SBCX-X PEB 3081	SBCX PEB 2081
Layer 1 state machine	With changes for correspondence with the actual ITU specification	
Layer 1 state machine in software	Possible	Not possible
Reset Signals	$\overline{\text{RES}}$ input signal $\overline{\text{RSTO}}$ output signal	$\overline{\text{RST}}$ input signal
Reset Sources	$\overline{\text{RES}}$ Input Watchdog C/I Code Change $\overline{\text{EAW}}$ Pin Software Reset	$\overline{\text{RST}}$ Input C/I Code Change
Interrupt Output Signals	$\overline{\text{INT}}$ low active (open drain) by default, reprogrammable to high active (push-pull)	Not provided
Pin SCLK	1.536 MHz	512 kHz

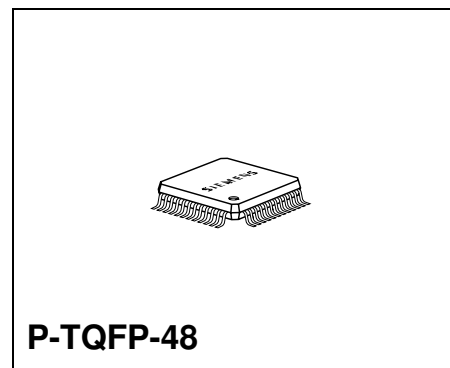
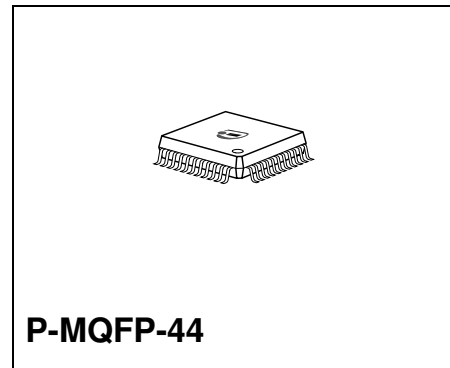
S/T Bus Interface Circuit Extended SBCX-X

PEB 3081

Version 1.4

1.1 Features

- Full duplex 2B + D S/T interface transceiver according to ITU-T I.430
- Successor of SBCX PEB 2081 in 3.3 V technology
- Conversion of the frame structure between the S/T-interface and IOM-2
- IOM-2 interface supporting TE, LT-T, LT-S, NT and intelligent NT modes
- Single and double clocks on IOM-2
- Two serial data strobe signals
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface
- Adaptively switched receive thresholds
- 3 general purpose I/O pins multiplexed with channel select pins
- Three pins for D-channel active indication, Stop/Go bit output and E-bit control on S
- One programmable timer
- Watchdog timer
- Software Reset
- One LED pin automatically indicating layer 1 activated state
- Test loops
- Sophisticated power management for restricted power mode



Type	Package
PEB 3081 H	P-MQFP-44
PEB 3081 F	P-TQFP-48

- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

1.2 Logic Symbol

The logic symbol gives an overview of the SBCX-X functions. It must be noted that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a “ * “ are multiplexed and not available in all modes.

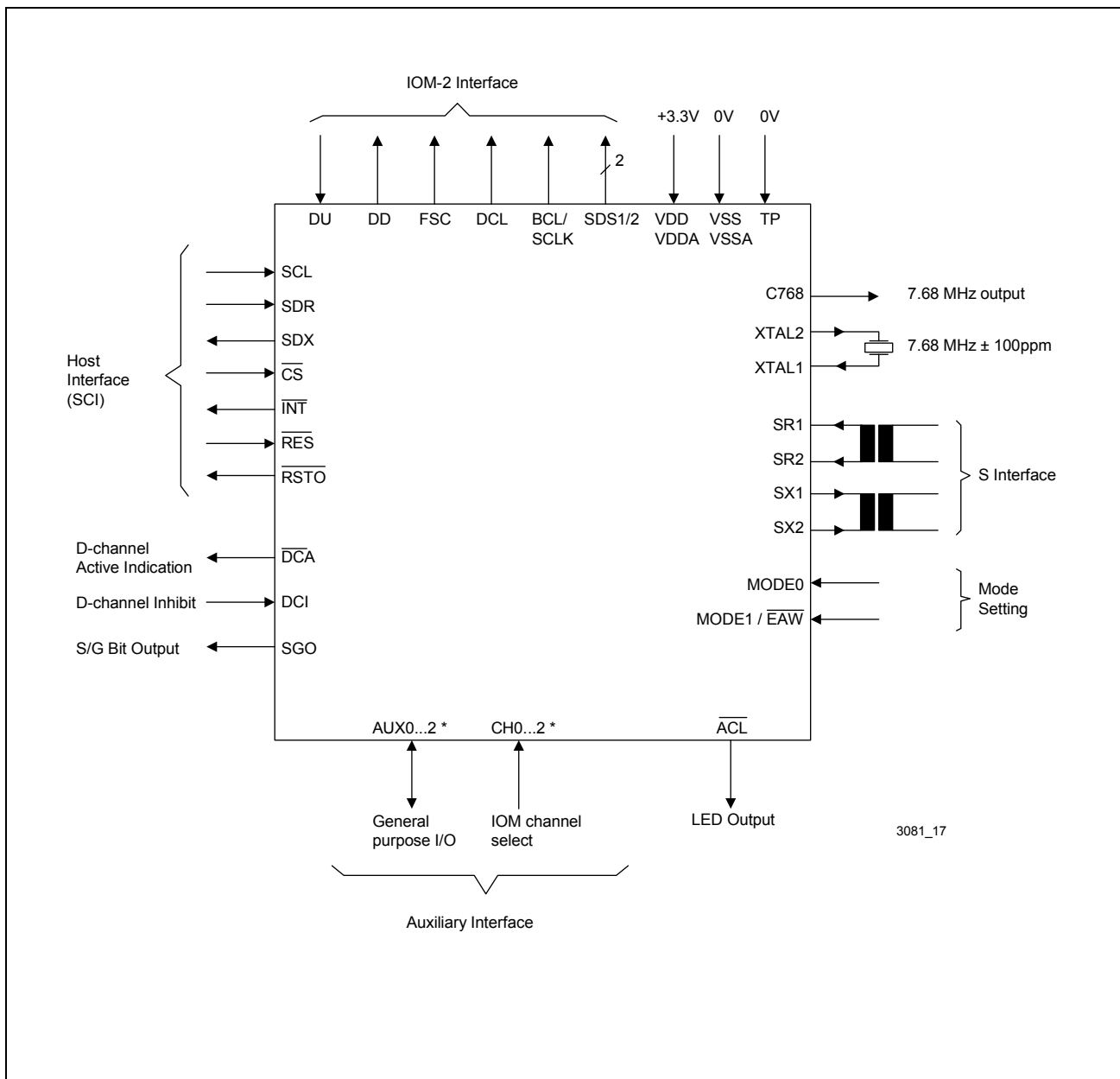


Figure 1 Logic Symbol of the SBCX-X

1.3 Typical Applications

The SBCX-X is designed for the user area of the ISDN basic access. By programming the corresponding operating mode it may be used at both ends of these interfaces.

Figure 2 illustrates the general application fields of the SBCX-X:

- ISDN terminals (TE mode)
- ISDN network termination (NT) for a link between the S/T interface and the U interface
- ISDN subscriber line termination (LT-S)
- ISDN trunk line termination (LT-T), i.e. PBX connection to central office

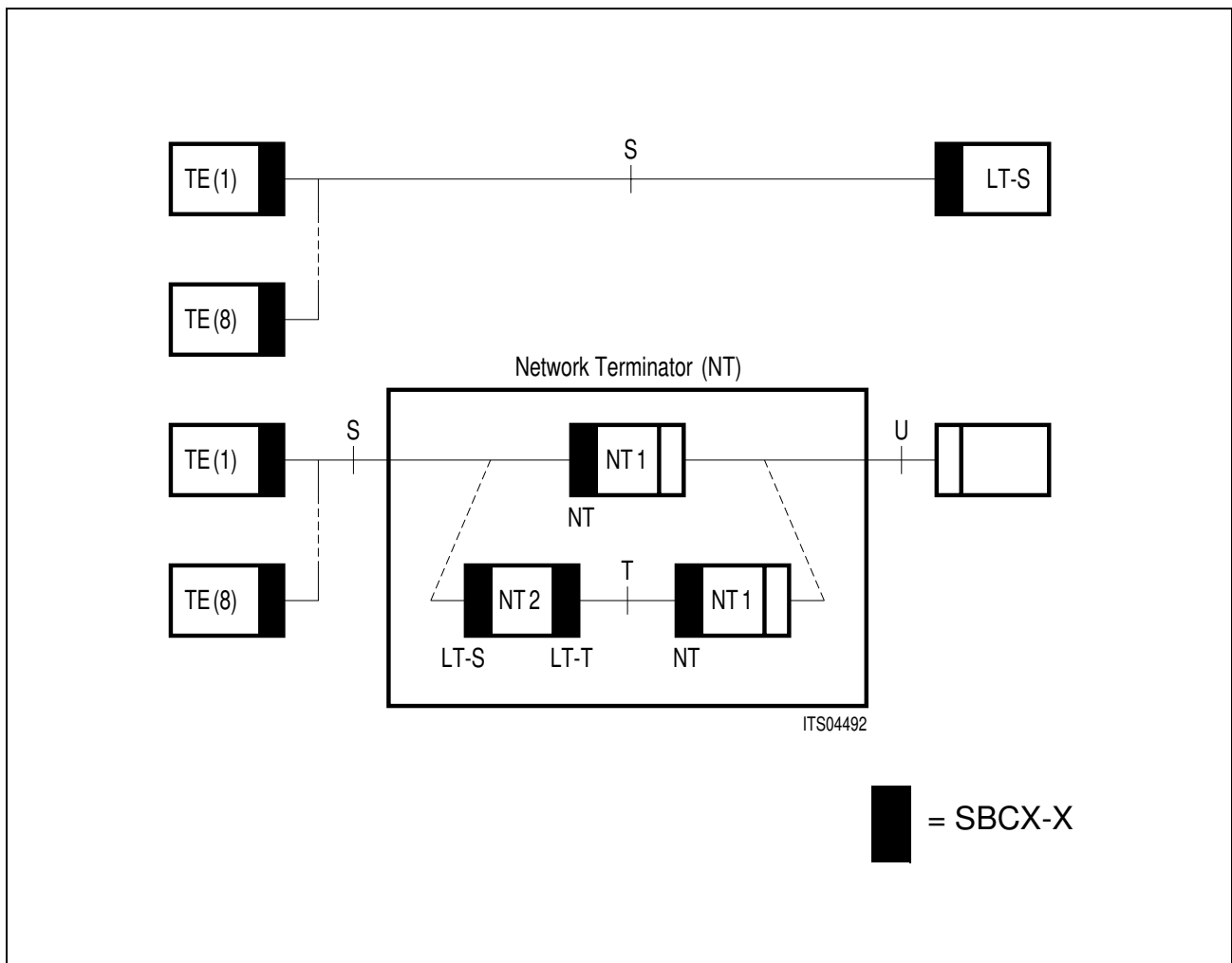


Figure 2 Applications of the SBCX-X

2 Pin Configuration

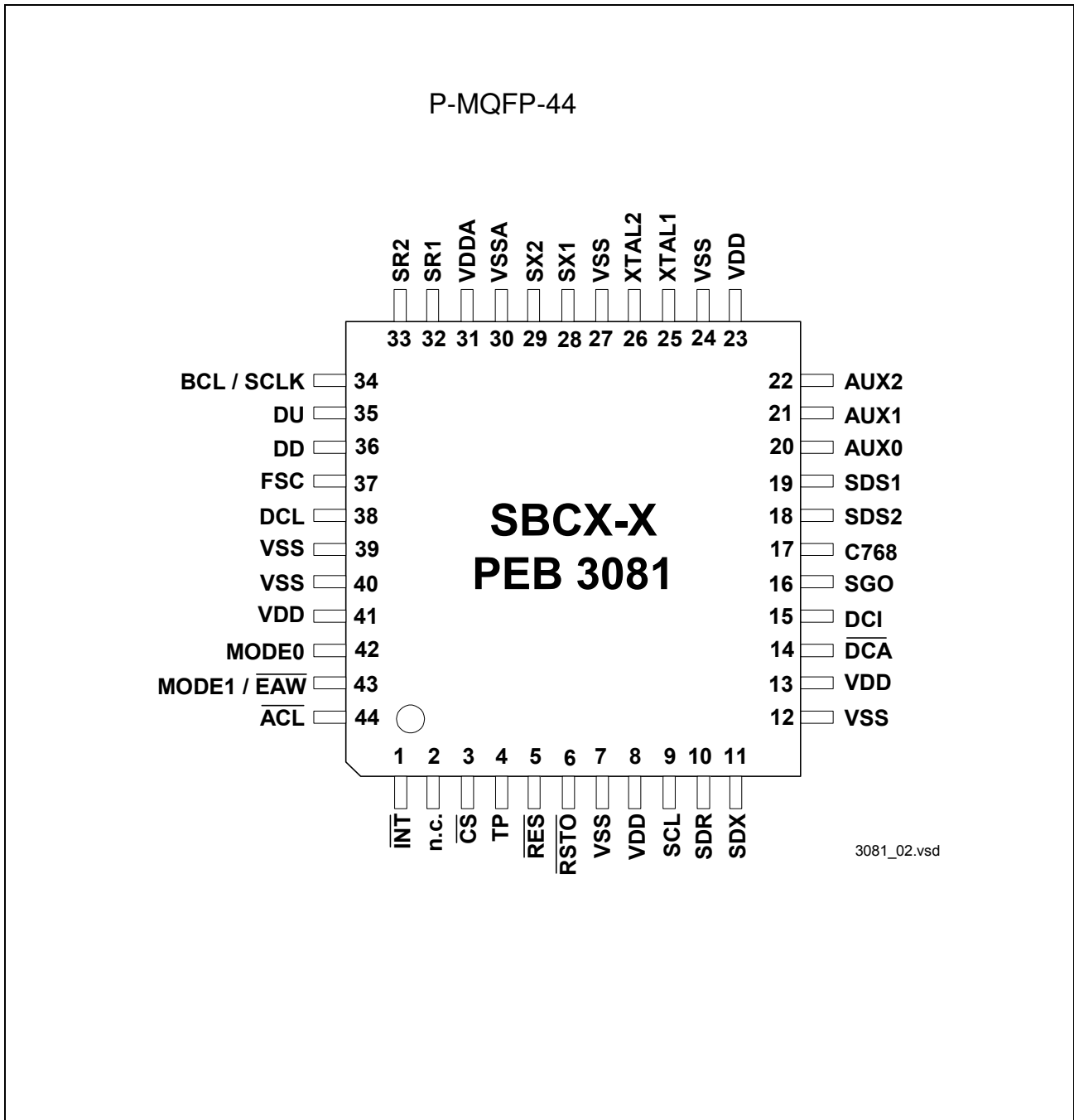


Figure 3 Pin Configuration of the SBCX-X (P-MQFP-44)

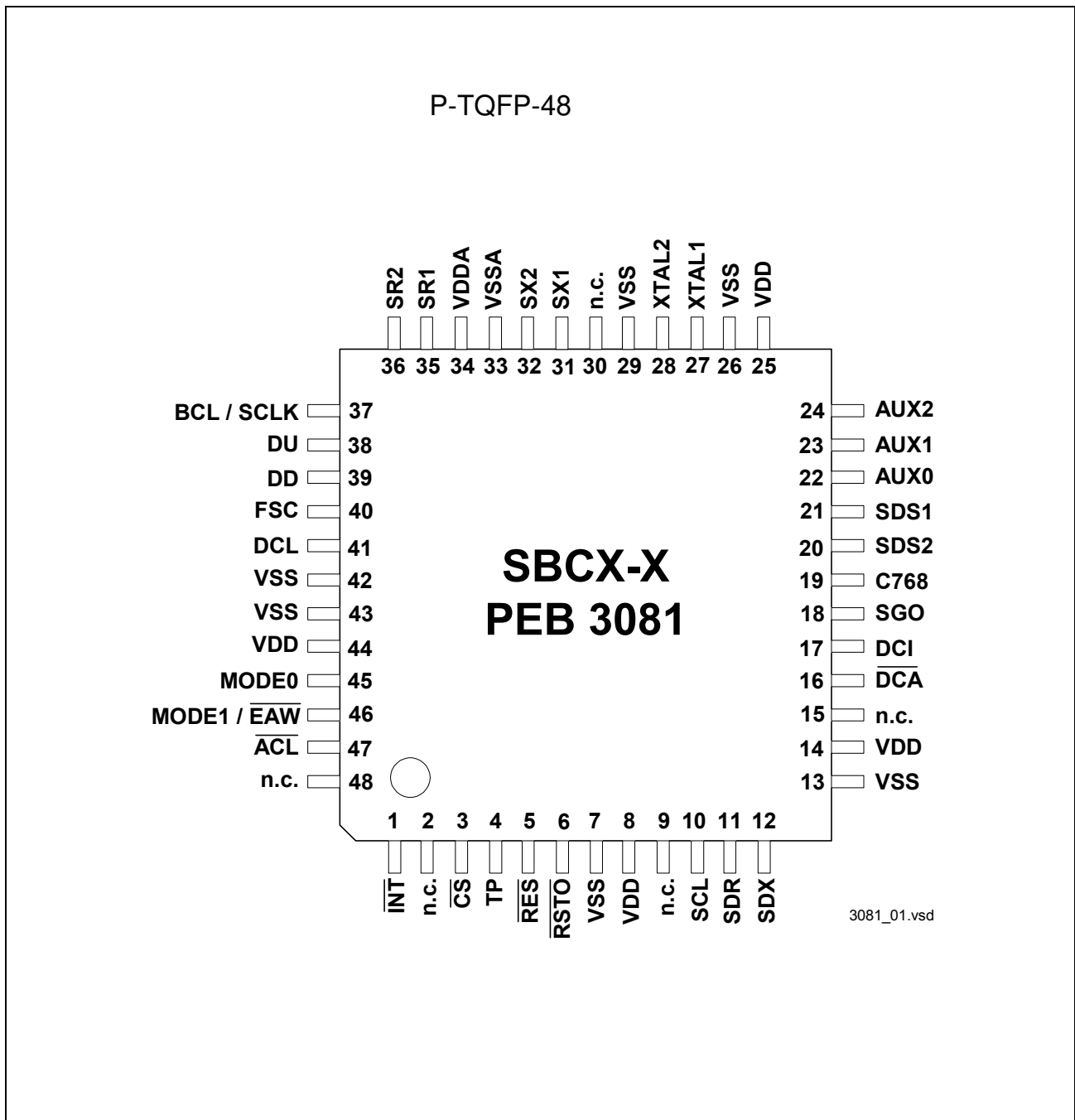


Figure 4 Pin Configuration of the SBCX-X (P-TQFP-48)

Table 2 SBCX-X Pin Definitions and Functions

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	TQFP-48			

Host Interface

9	10	SCL	I	SCL - Serial Clock Clock signal of the SCI interface if a serial interface is selected.
10	11	SDR	I	SDR - Serial Data Receive Receive data line of the SCI interface if a serial interface is selected.
11	12	SDX	OD	SDX - Serial Data Transmit Transmit data line of the SCI interface if a serial interface is selected.
3	3	CS	I	Chip Select A low level indicates a microcontroller access to the SBCX-X.
1	1	INT	O (OD)	Interrupt Request $\overline{\text{INT}}$ becomes active (low) if the SBCX-X requests an interrupt (open drain characteristic). The polarity can be reprogrammed to high active with push-pull characteristic.
5	5	RES	I	Reset A LOW on this input forces the SBCX-X into a reset state.

IOM-2 Interface

37	40	FSC	I/O	Frame Sync 8-kHz frame synchronization signal.
38	41	DCL	I/O	Data Clock IOM-2 interface clock signal (double clock, e.g. 1.536 MHz in TE mode).

Pin Configuration

Table 2 SBCX-X Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	TQFP-48			
34	37	BCL/ SCLK	O	Bit Clock/S-Clock TE-Mode: Bit clock output, identical to IOM-2 data rate (DCL/2). LT-T Mode: 1.536 MHz output synchronous to S-interface. NT / LT-S Mode: Bit clock output derived from the DCL input clock divided by 2.
36	39	DD	I/O (OD)	Data Downstream IOM-2 data signal in downstream direction.
35	38	DU	I/O (OD)	Data Upstream IOM-2 data signal in upstream direction.
19	21	SDS1	O	Serial Data Strobe 1 Programmable strobe signal for time slot and/or D-channel indication on IOM-2.
18	20	SDS2	O	Serial Data Strobe 2 Programmable strobe signal for time slot and/or D-channel indication on IOM-2.

Miscellaneous

28	31	SX1	O	S-Bus Transmitter Output (positive)
29	32	SX2	O	S-Bus Transmitter Output (negative)
32	35	SR1	I	S-Bus Receiver Input
33	36	SR2	I	S-Bus Receiver Input
25	27	XTAL1	I	Crystal 1 Connection for a crystal or used as external clock input. 7.68 MHz clock or crystal required.
26	28	XTAL2	O	Crystal 2 Connection for a crystal. Not connected if an external clock is supplied to XTAL1

Pin Configuration

Table 2 SBCX-X Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	TQFP-48			
20	22	AUX0	I/O (OD)	TE-Mode: Auxiliary Port 0 - 2 (input/output) These pins are individually programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. LT-T/LT-S/NT Mode: CH0-2 - IOM-2 Channel Select (input) These pins select one of eight channels on the IOM-2 interface.
21	23	AUX1	I/O (OD)	
22	24	AUX2	I/O (OD)	
42	45	MODE0	I	Mode 0 Select A LOW selects TE-mode and a HIGH selects LT-T / LT-S mode (see MODE1/EAW).
43	46	MODE1	I	The pin function depends on the setting of MODE0. If MODE0=1: Mode 1 Select A LOW selects LT-T mode and a HIGH selects LT-S mode. If MODE0=0: External Awake If a falling edge on this input is detected, the SBCX-X generates an interrupt and, if enabled, a reset pulse.
		EAW	I	
6	6	RSTO	OD	Reset Output Low active reset output, either from a watchdog timeout or programmed by the host.
17	19	C768	O	Clock Output A 7.68 MHz clock is output to support other devices. This clock is not synchronous to the S interface.
14	16	DCA	O	DCA - D-Channel Active Indication This pin provides an output of the D-channel bits on the S-bus receive line.

Pin Configuration

Table 2 SBCX-X Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O) Open Drain (OD)	Function
MQFP-44	TQFP-48			
15	17	DCI	I	DCI - D-Channel Inhibit If this bit is set to '1' the E-bits are inverted, i.e. the D-channel is blocked (only in NT/LT-S mode). This pin has the same function as the D-channel inhibit bit (see TR_MODE.DCH_INH).
16	18	SGO	O	SGO - Stop/Go Bit Output A S/G bit output with programmable polarity and length (TR_CONF2 register) is provided.
44	47	ACL	O	Activation LED This pin can either function as a programmable output or it can automatically indicate the activated state of the S interface by a logic '0'. An LED with pre-resistance may directly be connected to \overline{ACL} .
4	4	TP	I	Test Pin Must be connected to V_{SS} .
2	2, 9, 15, 30, 48	n.c.		Not Connected

Power Supply

8, 13, 23, 41	8, 14, 25, 44	V_{DD}	–	Digital Power Supply Voltage (3.3 V \pm 5 %)
31	34	V_{DDA}	–	Analog Power Supply Voltage (3.3 V \pm 5 %)
7, 12, 24, 27, 39, 40	7, 13, 26, 29, 42, 43	V_{SS}	–	Digital Ground (0 V)
30	33	V_{SSA}	–	Analog Ground (0 V)

3 Description of Functional Blocks

3.1 General Functions and Device Architecture

Figure 5 shows the architecture of the SBCX-X containing the following functions:

- S/T-interface transceiver supporting TE, LT-T, LT-S, NT and intelligent NT modes
- Serial Control Interface (SCI)
- IOM-2 interface for terminal, linecard and NT applications, with single/double clock
- Two serial data strobe signals
- IOM handler with controller data access registers (CDA) allows flexible access to IOM timeslots for reading/writing, looping and shifting data
- Synchronous transfer interrupts (STI) allow controlled access to IOM timeslots
- MONITOR channel handler on IOM-2 for master mode, slave mode or data exchange
- C/I-Channel handler
- D-channel access mechanism
- 3-pin auxiliary port for general purpose I/O pins or channel select pins
- LED connected to pin ACL indicates S-interface activation status automatically or can be controlled by the host
- Output for D-channel active indication (output of received D-bits on S)
- Stop/Go bit output with programmable polarity and length
- D-channel inhibit input pin to control inversion of E-bits on S to block other terminals
- Level detect circuit on the S interface reduces power consumption in power down mode
- Timer for periodic or single interrupts
- Clock and timing generation
- Digital PLL to synchronize the transceiver to the S/T interface
- Buffered 7.68 MHz oscillator clock output allows connection of further devices and saves another crystal on the system board
- Reset generation (watchdog timer)

Description of Functional Blocks

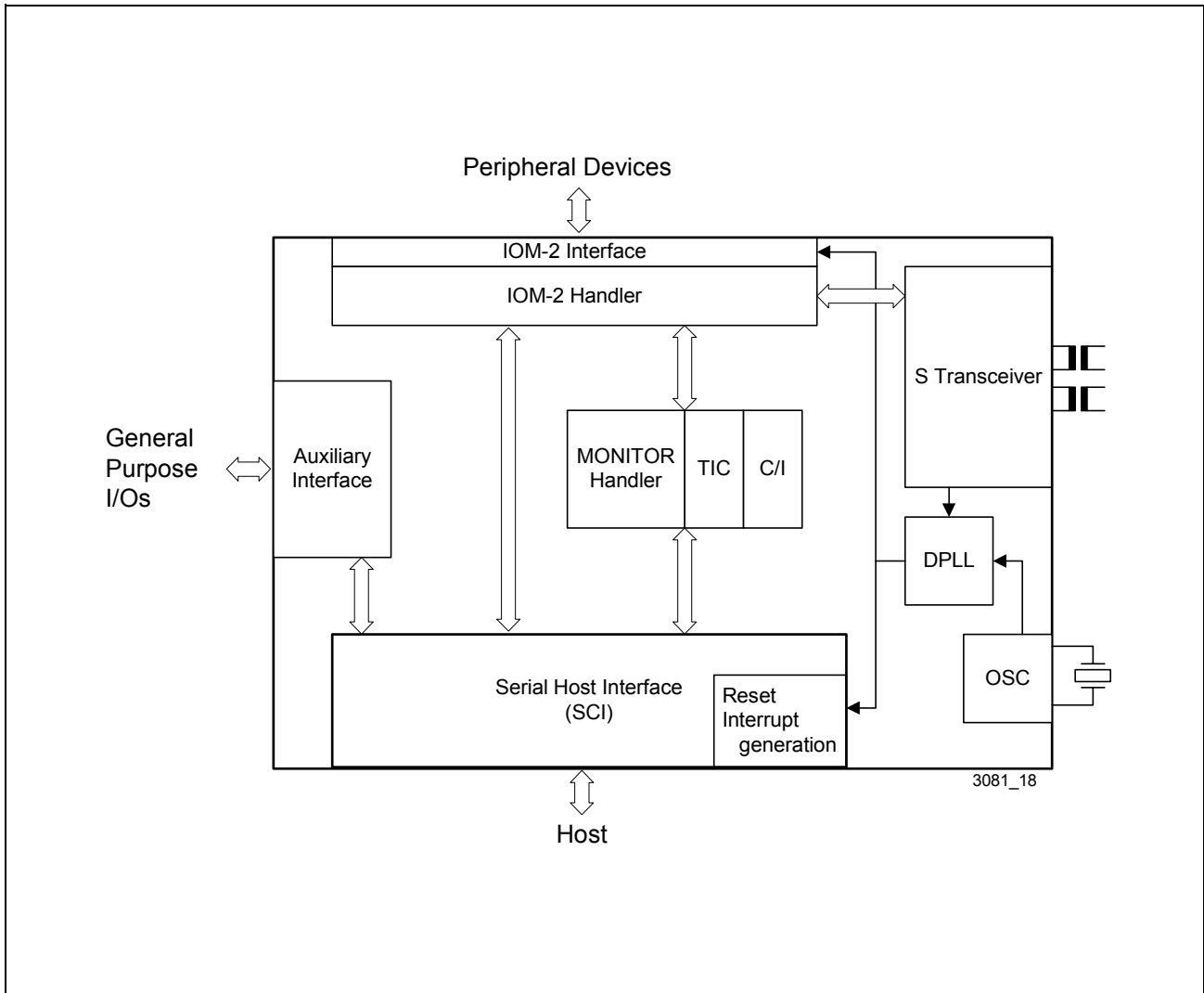


Figure 5 Functional Block Diagram of the SBCX-X

3.2 Microcontroller Interface

The SBCX-X supports a serial microcontroller interface. For applications where no controller is connected to the SBCX-X programming is done via the IOM-2 MONITOR channel from a master device. In such applications the SBCX-X operates in the IOM-2 slave mode (refer to the corresponding chapter of the IOM-2 MONITOR handler). This mode is suitable for control functions (e.g. programming registers of the S/T transceiver), but the bandwidth is not sufficient to transfer B- and D-channel data.

The interface selection is done by pinstrapping of the chip select signal \overline{CS} (see [Table 3](#)). The selection pins are evaluated when the reset input \overline{RES} is active. For the pin levels stated in the table the following is defined:

'High': dynamic pin; value must be 'High' only during reset

V_{SS} : static pin; pin must statically be strapped to 'Low' level

Table 3 Host Interface Selection

CS	Interface Mode
'High'	Serial Control Interface (SCI)
V_{SS}	IOM-2 MONITOR Channel (Slave Mode)

The interfaces contain all circuitry necessary for the access to programmable registers. The mapping of all these registers can be found in [Chapter 4](#).

The microcontroller interface also provides an interrupt request at pin \overline{INT} which is low active by default but can be reprogrammed to high active, a reset input pin \overline{RES} and a reset output pin \overline{RSTO} .

The interrupt request pin \overline{INT} becomes active if the SBCX-X requests an interrupt and this can occur at any time.