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Data Sheet, DS1, Jan. 2003

ISAC-SX

ISDN Subscriber Access Controller

PEB 3086, V 1.4

Wired Communications

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Data Sheet

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Previous Version: Data Sheet, DS1, V1.3, 2000-08-03

Page	Subjects (major changes since last revision)
Chapter 1	Comparison ISAC-S/ISAC-SX
Chapter 3.3.7.2	S- Transceiver Synchronization New
Chapter 3.3.11	Test Functions extended
Chapter 3.7.1.1	CDA Handler Description extended
Chapter 3.7.5.1	TIC Bus Access Control: Note added
Chapter 5.6	IOM-2 Interface Timing: Explanation added
Chapter 5.7.2	Parallel Microcontroller Interface Timing: Explanation added
Chapter 5.10	S-Transceiver
Chapter 5.11	Recommended Transformer Specification: Changed
Chapter 5.12	Line Overload Protection added
Chapter 5.13	EMC/ESD added

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1 Overview

The ISDN Subscriber Access Controller ISAC-SX integrates a D-channel HDLC controller and a four wire S/T interface used to link voice/data terminals to the ISDN. It is based on the ISAC-S PEB 2086, and provides enhanced features and functionality.

It includes the S-transceiver (Layer 1), an HDLC controller for the D-channel and one B-channel protocol controller (HDLC or transparent) with reduced features dedicated for firmware download via the B-channel.

The system integration is simplified by several configurations of the parallel microcontroller interface selected via pin strapping. They include multiplexed and demultiplexed interface selection as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations. The ISAC-SX also provides a serial control interface (SCI).

The FIFO size of the cyclic D-channel buffer is 64 bytes per direction with programmable block size (threshold). Besides TE mode the S-transceiver supports other terminal relevant operation modes like line termination subscriber side (LT-S), line termination trunk side (LT-T) and NT applications (NT, Intelligent NT mode).

An auxiliary I/O port has been added with interrupt capabilities on two input lines. These programmable I/O lines may be used to connect peripheral components to the ISAC-SX which need software control or have to forward status information to the host.

Three programmable LED outputs can be used to indicate certain status information, one of them is capable to indicate the activation status of the S-interface automatically.

The ISAC-SX is produced in advanced CMOS technology.

Table 1 Comparison of the ISAC-SX with the Previous Version ISAC-S

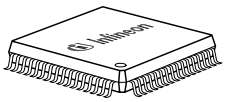
	ISAC-SX PEB 3086	ISAC-S PEB 2086
Operating modes	TE, LT-T, LT-S, NT, Int. NT	TE, LT-T, LT-S, NT
Supply voltage	3.3 V ± 5%	5 V ± 5%
Technology	CMOS	CMOS
Package	P-MQFP-64 / P-TQFP-64	P-MQFP-64 / P-LCC-44
Transceiver Transformer ratio for the transmitter receiver	 1:1 1:1	 2:1 2:1
Test Functions	- Dig. loop via Layer 2 (TLP) - Layer 1 disable (DIS_TR) - Analog loop (LP_A- bit EXLP- bit, ARL)	- Dig. loop via Layer 2(TLP) - Layer 1 disable (DIS_TR) - Analog loop (ARL)
Microcontroller Interface	Serial interface (SCI) 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux direct/ indirect Addressing	Not provided 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux
Command structure of the register access (SCI)	Header/address/data	Address/data
Crystal	7.68 MHz	7.68 MHz
Buffered 7.68 MHz output	Provided	Not provided
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Restricted access to B- and IC-channel
Data control and manipulation	Various possibilities of data control and data manipulation (enable/ disable, shifting, looping, switching)	B- and IC-channel looping
IOM-2		

	ISAC-SX PEB 3086	ISAC-S PEB 2086
IOM-2 Interface	Double clock (DCL), bit clock (BCL), serial data strobe 1 (SDS1) serial data strobe 2 (SDS2)	Double clock (DCL), bit clock (BCL), serial data strobe (SDS)
Monitor channel programming	Provided (MON0, 1, 2, ..., 7)	Provided (MON0 or 1)
C/I channels	CI0 (4bit), CI1 (4/6bit)	CI0 (4bit), CI1 (6bit)
Layer 1 state machine	With changes for correspondence with the actual ITU specification	
Layer 1 state machine in software	Possible	Not possible
Support of IDSL (144kBit/s)	Provided (HDLC controller access, SDS1/2 signals active)	Not provided
D-channel HDLC support	D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode	D-channel timeslot; auto mode, non-auto mode, transparent mode 1-3
D-channel FIFO size	64 bytes cyclic buffer per direction with programmable FIFO thresholds	2x32 bytes buffer per direction
FW download support	One B-channel controller	Not provided
HDLC support (B-channel)	D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode	Not provided
FIFO size (B-channel)	128 bytes cyclic buffer per direction with programmable FIFO thresholds (8 or 16 bytes)	Not provided
Reset Signals	$\overline{\text{RES}}$ input signal $\overline{\text{RSTO}}$ output signal	RST input/output signal

	ISAC-SX PEB 3086	ISAC-S PEB 2086
Reset Sources	$\overline{\text{RES}}$ Input Watchdog C/I Code Change $\overline{\text{EAW}}$ Pin Software Reset	RST Input Watchdog C/I Code Change EAW Pin
Interrupt Output Signals	$\overline{\text{INT}}$ low active (open drain) by default, reprogrammable to high active (push-pull)	Low active $\overline{\text{INT}}$
Pin SCLK	1.536 MHz	512 kHz

V 1.4

1.1 Features



P-MQFP-64-1

P-TQFP-64-1

- Full duplex 2B + D S/T interface transceiver according to ITU-T I.430
- Successor of ISAC-S PEB 2086 in 3.3 V technology
- 8-bit parallel microcontroller interface, Motorola and Siemens/Intel bus type multiplexed or non-multiplexed, direct-/indirect register addressing
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Various types of protocol support (Non-auto mode, transparent mode, extended transparent mode)
- One D-channel HDLC controller with 64 byte FIFOs per direction
- One B-channel HDLC controller with reduced functionality (e.g. for firmware upgrades)
- IOM-2 interface in TE, LT-T, LT-S and NT mode, single/double clocks and two strobe signals
- D-channel priority handler on IOM-2 for intelligent NT applications
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Conversion of the frame structure between the S/T-interface and IOM-2
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface
- Adaptively switched receive thresholds

Type	Package
PEB 3086 H	P-MQFP-64-1
PEB 3086 F	P-TQFP-64-1

- Auxiliary Interface with general purpose I/O pins and LED drivers
- Two programmable timers
- Watchdog timer
- Software Reset
- Multiframe Synchronization
- Test loops
- Sophisticated power management for restricted power mode
- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

1.2 Logic Symbol

The logic symbol gives an overview of the ISAC-SX functions. It must be noted that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.

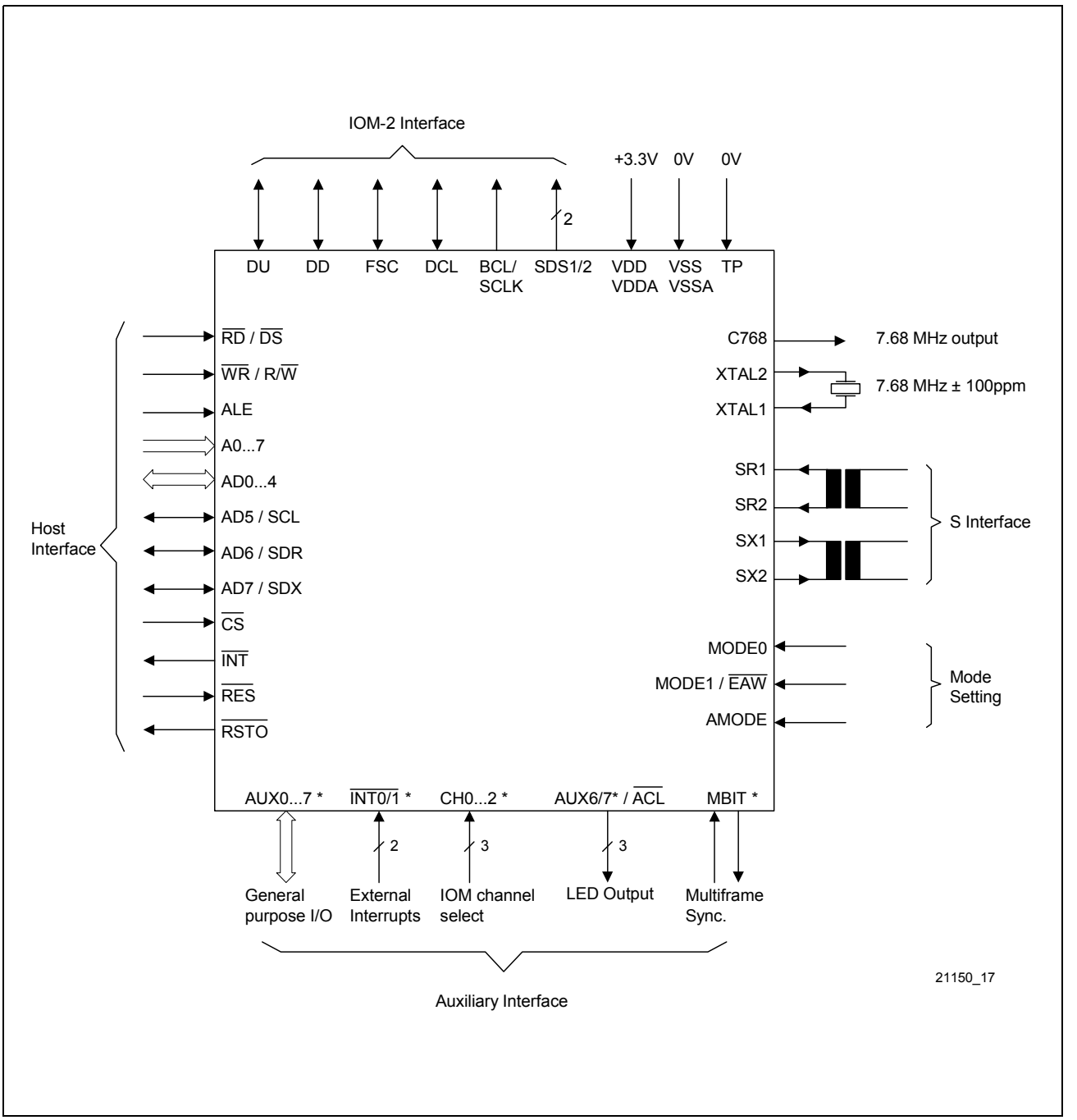


Figure 1 Logic Symbol of the ISAC-SX

1.3 Typical Applications

The ISAC-SX is designed for the user area of the ISDN basic access, especially for subscriber terminal equipment and for exchange equipment with S interface.
Figure 2 illustrates the general application fields of the ISAC-SX.

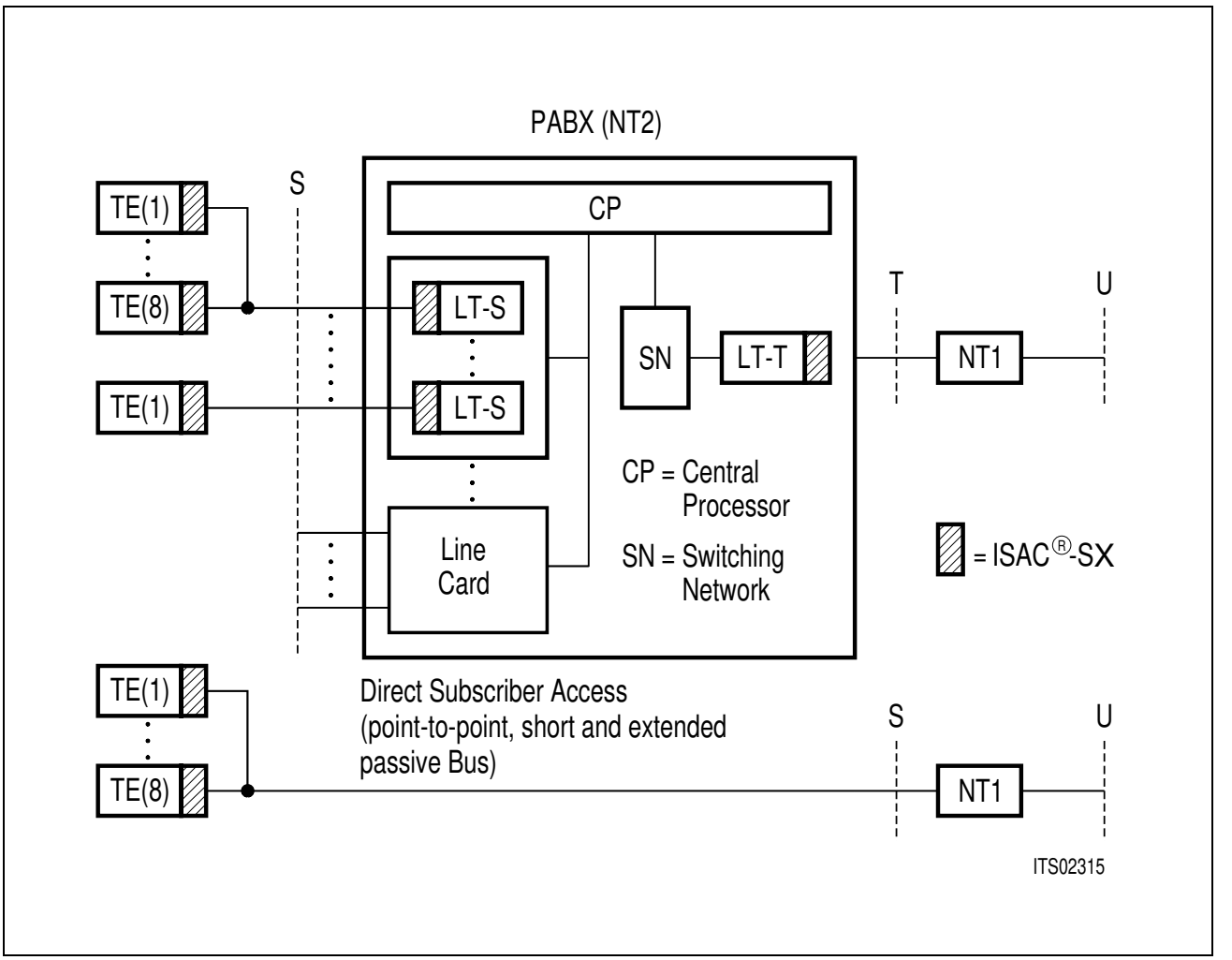


Figure 2 Applications of the ISAC-SX

2 Pin Configuration

P-MQFP-64-1
P-TQFP-64-1

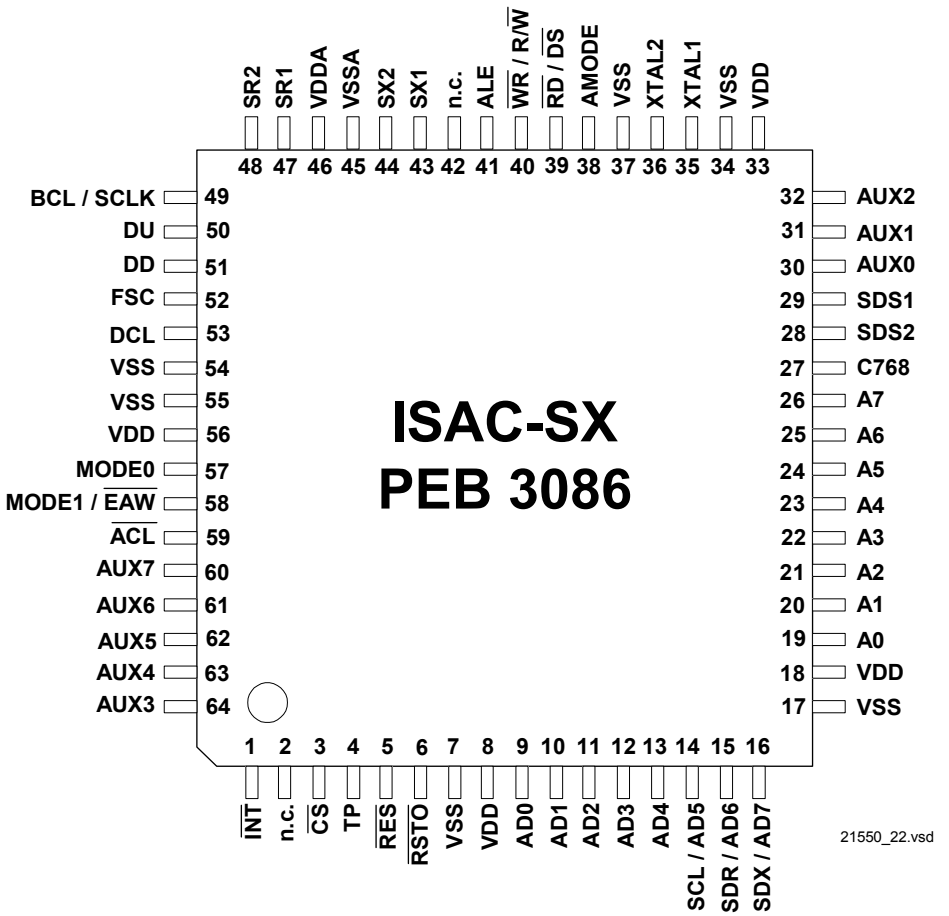


Figure 3 Pin Configuration of the ISAC-SX

Table 2 ISAC-SX Pin Definitions and Functions

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
Host Interface			
19 20 21 22 23 24 25 26	A0 A1 A2 A3 A4 A5 A6 A7	I I I I I I I I	• **Non-Multiplexed Bus Mode:** **Address Bus** Address bus transfers addresses from the microcontroller to the ISAC-SX. For indirect address mode only A0 is valid (A1-A7 to be connected to VDD). • **Multiplexed Bus Mode:** Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD.
9 10 11 12 13	AD0 AD1 AD2 AD3 AD4	I/O I/O I/O I/O I/O	• **Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the microcontroller to the ISAC-SX and data between the microcontroller and the ISAC-SX. • **Non-Multiplexed Bus Mode:** **Data bus** Transfers data between the microcontroller and the ISAC-SX.
14	AD5 SCL	I/O I	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD5 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D5 if the parallel interface is selected. **SCI - Serial Clock** Clock signal of the SCI interface if a serial interface is selected.

Table 2 ISAC-SX Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
15	AD6	I/O	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD6 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D6 if the parallel interface is selected.
	SDR	I	**SCI - Serial Data Receive** Receive data line of the SCI interface if a serial interface is selected.
16	AD7	I/O	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD7 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D7 if the parallel interface is selected.
	SDX	OD	**SCI - Serial Data Transmit** Transmit data line of the SCI interface if a serial interface is selected.
39	$\overline{RD}$	I	**Read** Indicates a read access to the registers (Siemens/ Intel bus mode).
	$\overline{DS}$	I	**Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
40	$\overline{WR}$	I	**Write** Indicates a write access to the registers (Siemens/ Intel bus mode).
	R/$\overline{W}$	I	**Read/Write** A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).

Table 2 ISAC-SX Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
41	ALE	I	**Address Latch Enable** A HIGH on this line indicates an address on the external address/data bus (multiplexed bus type only). ALE also selects the microcontroller interface bus type (multiplexed or non multiplexed).
3	$\overline{CS}$	I	**Chip Select** A low level indicates a microcontroller access to the ISAC-SX.
1	$\overline{INT}$	OD (O)	**Interrupt Request** $\overline{INT}$ becomes active low (open drain) if the ISAC-SX requests an interrupt. The polarity can be reprogrammed to high active with push-pull characteristic.
5	$\overline{RES}$	I	**Reset** A LOW on this input forces the ISAC-SX into a reset state.
38	AMODE	I	**Address Mode** Selects between direct (0) and indirect (1) register access mode.
IOM-2 Interface			
52	FSC	I/O	**Frame Sync** 8-kHz frame synchronization signal.
53	DCL	I/O	**Data Clock** IOM-2 interface clock signal (double clock) (e.g 1.536 MHz in TE mode).

Table 2 ISAC-SX Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
49	BCL/ SCLK	O	**Bit Clock/S-Clock** **TE-Mode:** Bit clock output, identical to IOM-2 data rate (DCL/ 2). **LT-T Mode:** 1.536 MHz output synchronous to S-interface. **NT / LT-S Mode:** Bit clock output derived from the DCL input clock divided by 2.
51	DD	I/O (OD)	**Data Downstream** IOM-2 data signal in downstream direction.
50	DU	I/O (OD)	**Data Upstream** IOM-2 data signal in upstream direction.
29	SDS1	O	**Serial Data Strobe 1** Programmable strobe signal for time slot and/or D-channel indication on IOM-2.
28	SDS2	O	**Serial Data Strobe 2** Programmable strobe signal for time slot and/or D-channel indication on IOM-2.
Auxiliary Interface			
30 31 32	AUX0 AUX1 AUX2	I/O (OD) I/O (OD) I/O (OD)	• **TE-Mode:** **Auxiliary Port 0 - 2 (input/output)** These pins are individually programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. • **LT-T/LT-S/NT Mode:** **CH0-2 - IOM-2 Channel Select (input)** These pins select one of eight channels on the IOM-2 interface.
64	AUX3	I/O (OD)	**Auxiliary Port 3 (input/output)** This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.