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ISAC-SX

ISDN Subscriber Access
Controller

PEB 3086, V 1.4

Wired
Communications



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Table of Contents		Page
1	Overview	13
1.1	Features	17
1.2	Logic Symbol	19
1.3	Typical Applications	20
2	Pin Configuration	21
3	Description of Functional Blocks	30
3.1	General Functions and Device Architecture	30
3.2	Microcontroller Interfaces	32
3.2.1	Serial Control Interface (SCI)	33
3.2.1.1	Programming Sequences	34
3.2.2	Parallel Microcontroller Interface	37
3.2.3	Interrupt Structure	39
3.2.4	Reset Generation	41
3.2.5	Timer Modes	43
3.2.6	Activation Indication via Pin ACL	45
3.3	S/T-Interface	46
3.3.1	S/T-Interface Coding	48
3.3.2	S/T-Interface Multiframe	50
3.3.3	Multiframe Synchronization (M-Bit)	52
3.3.4	Data Transfer and Delay between IOM-2 and S/T	55
3.3.5	Transmitter Characteristics	58
3.3.6	Receiver Characteristics	59
3.3.7	S/T Interface Circuitry	60
3.3.7.1	External Protection Circuitry	60
3.3.7.2	S-Transceiver Synchronization	62
3.3.8	S/T Interface Delay Compensation (TE/LT-T mode)	63
3.3.9	Level Detection Power Down	63
3.3.10	Transceiver Enable/Disable	64
3.3.11	Test Functions	64
3.4	Clock Generation	66
3.4.1	Description of the Receive PLL (DPLL)	69
3.4.2	Jitter	69
3.4.3	Oscillator Clock Output C768	70
3.5	Control of Layer-1	71
3.5.1	State Machine TE and LT-T Mode	73
3.5.1.1	State Transition Diagram (TE, LT-T)	73
3.5.1.2	States (TE, LT-T)	75
3.5.1.3	C/I Codes (TE, LT-T)	77
3.5.1.4	Infos on S/T (TE, LT-T)	79
3.5.2	State Machine LT-S Mode	80
3.5.2.1	State Transition Diagram (LT-S)	80

Table of Contents		Page
3.5.2.2	States (LT-S)	81
3.5.2.3	C/I Codes (LT-S)	82
3.5.2.4	Infos on S/T (LT-S)	83
3.5.3	State Machine NT Mode	84
3.5.3.1	State Transition Diagram (NT)	84
3.5.3.2	States (NT)	85
3.5.3.3	C/I Codes (NT)	86
3.5.4	Command/ Indicate Channel Codes (C/I0) - Overview	88
3.6	Control Procedures	89
3.6.1	Example of Activation/Deactivation	89
3.6.2	Activation initiated by the Terminal	90
3.6.3	Activation initiated by the Network Termination NT	91
3.7	IOM-2 Interface	92
3.7.1	IOM-2 Handler	95
3.7.1.1	Controller Data Access (CDA)	97
3.7.2	Serial Data Strobe Signal and Strobed Data Clock	107
3.7.2.1	Serial Data Strobe Signal	107
3.7.2.2	Strobed IOM-2 Bit Clock	109
3.7.3	IOM-2 Monitor Channel	110
3.7.3.1	Handshake Procedure	111
3.7.3.2	Error Treatment	114
3.7.3.3	MONITOR Channel Programming as a Master Device	116
3.7.3.4	MONITOR Channel Programming as a Slave Device	117
3.7.3.5	Monitor Time-Out Procedure	118
3.7.3.6	MONITOR Interrupt Logic	119
3.7.4	C/I Channel Handling	119
3.7.5	D-Channel Access Control	121
3.7.5.1	TIC Bus D-Channel Access Control	121
3.7.5.2	S-Bus Priority Mechanism for D-Channel	123
3.7.5.3	S-Bus D-Channel Control in LT-T	126
3.7.5.4	D-Channel Control in the Intelligent NT (TIC- and S-Bus)	126
3.7.6	Activation/Deactivation of IOM-2 Interface	130
3.8	Auxiliary Interface	133
3.8.1	Mode Dependent Functions	133
3.8.2	Message Transfer Modes	136
3.8.3	Data Reception	137
3.8.3.1	Structure and Control of the Receive FIFO	137
3.8.3.2	Receive Frame Structure	144
3.8.4	Data Transmission	146
3.8.4.1	Structure and Control of the Transmit FIFO	146
3.8.4.2	Transmit Frame Structure	151
3.8.5	Access to IOM-2 Channels	151

Table of Contents		Page
3.8.6	Extended Transparent Mode	151
3.8.7	HDLC Controller Interrupts	153
3.9	Test Functions	154
4	Detailed Register Description	156
4.1	D-channel HDLC Control and C/I Registers	164
4.1.1	RFIFOD - Receive FIFO D-Channel	164
4.1.2	XFIFOD - Transmit FIFO D-Channel	164
4.1.3	ISTAD - Interrupt Status Register D-Channel	165
4.1.4	MASKD - Mask Register D-Channel	166
4.1.5	STARD - Status Register D-Channel	167
4.1.6	CMDRD - Command Register D-Channel	167
4.1.7	MODED - Mode Register	168
4.1.8	EXMD1- Extended Mode Register D-Channel 1	170
4.1.9	TIMR1 - Timer 1 Register	172
4.1.10	SAP1 - SAPI1 Register	172
4.1.11	SAP2 - SAPI2 Register	173
4.1.12	RBCLD - Receive Frame Byte Count Low D-Channel	173
4.1.13	RBCHD - Receive Frame Byte Count High D-Channel	173
4.1.14	TEI1 - TEI1 Register 1	174
4.1.15	TEI2 - TEI2 Register	174
4.1.16	RSTAD - Receive Status Register D-Channel	175
4.1.17	TMD -Test Mode Register D-Channel	177
4.1.18	CIR0 - Command/Indication Receive 0	177
4.1.19	CIX0 - Command/Indication Transmit 0	178
4.1.20	CIR1 - Command/Indication Receive 1	179
4.1.21	CIX1 - Command/Indication Transmit 1	179
4.2	Transceiver Registers	180
4.2.1	TR_CONF0 - Transceiver Configuration Register 0	180
4.2.2	TR_CONF1 - Transceiver Configuration Register 1	181
4.2.3	TR_CONF2 - Transmitter Configuration Register 2	181
4.2.4	TR_STA - Transceiver Status Register	183
4.2.5	TR_CMD - Transceiver Command Register	184
4.2.6	SQRR1 - S/Q-Channel Receive Register 1	185
4.2.7	SQXR1- S/Q-Channel TX Register 1	186
4.2.8	SQRR2 - S/Q-Channel Receive Register 2	186
4.2.9	SQXR2 - S/Q-Channel TX Register 2	186
4.2.10	SQRR3 - S/Q-Channel Receive Register 3	187
4.2.11	SQXR3 - S/Q-Channel TX Register 3	187
4.2.12	ISTATR - Interrupt Status Register Transceiver	187
4.2.13	MASKTR - Mask Transceiver Interrupt	188
4.2.14	TR_MODE - Transceiver Mode Register 1	188
4.3	Auxiliary Interface Registers	190

Table of Contents		Page
4.3.1	ACFG1 - Auxiliary Configuration Register 1	190
4.3.2	ACFG2 - Auxiliary Configuration Register 2	190
4.3.3	AOE - Auxiliary Output Enable Register	192
4.3.4	ARX - Auxiliary Interface Receive Register	192
4.3.5	ATX - Auxiliary Interface Transmit Register	193
4.4	IOM-2 and MONITOR Handler	194
4.4.1	CDAXy - Controller Data Access Register xy	194
4.4.2	XXX_TSDPxxy - Time Slot and Data Port Selection for CHxy	195
4.4.3	CDAX_CR - Control Register Controller Data Access CH1x	196
4.4.4	TR_CR - Control Register Transceiver Data (IOM_CR.CI_CS=0) ...	197
4.4.5	BCH_CR - Control Register B-Channel Controller Data	198
4.4.6	DCI_CR - Control Register for D and CI1 Handler (IOM_CR.CI_CS=0)	199
4.4.7	MON_CR - Control Register Monitor Data	201
4.4.8	SDSx_CR - Control Register Serial Data Strobe x	202
4.4.9	IOM_CR - Control Register IOM Data	203
4.4.10	STI - Synchronous Transfer Interrupt	205
4.4.11	ASTI - Acknowledge Synchronous Transfer Interrupt	206
4.4.12	MSTI - Mask Synchronous Transfer Interrupt	206
4.4.13	SDS_CONF - Configuration Register for Serial Data Strobes	207
4.4.14	MCDA - Monitoring CDA Bits	207
4.4.15	MOR - MONITOR Receive Channel	208
4.4.16	MOX - MONITOR Transmit Channel	208
4.4.17	MOSR - MONITOR Interrupt Status Register	208
4.4.18	MOCR - MONITOR Control Register	209
4.4.19	MSTA - MONITOR Status Register	210
4.4.20	MCONF - MONITOR Configuration Register	210
4.5	Interrupt and General Configuration	211
4.5.1	ISTA - Interrupt Status Register	211
4.5.2	MASK - Mask Register	212
4.5.3	AUXI - Auxiliary Interrupt Status Register	212
4.5.4	AUXM - Auxiliary Mask Register	213
4.5.5	MODE1 - Mode1 Register	213
4.5.6	MODE2 - Mode2 Register	215
4.5.7	ID - Identification Register	216
4.5.8	SRES - Software Reset Register	216
4.5.9	TIMR2 - Timer 2 Register	217
4.6	B-Channel Registers	218
4.6.1	ISTAB - Interrupt Status Register B-Channel	218
4.6.2	MASKB - Mask Register B-Channel	219
4.6.3	STARB - Status Register B-Channel	219
4.6.4	CMDRB - Command Register B-channel	220

Table of Contents		Page
4.6.5	MODEB - Mode Register	221
4.6.6	EXMB - Extended Mode Register B-Channel	222
4.6.7	RAH1 - RAH1 Register	223
4.6.8	RAH2 - RAH2 Register	223
4.6.9	RBCLB - Receive Frame Byte Count Low B-Channel	224
4.6.10	RBCHB - Receive Frame Byte Count High B-Channel	224
4.6.11	RAL1 - RAL1 Register 1	225
4.6.12	RAL2 - RAL2 Register	225
4.6.13	RSTAB - Receive Status Register B-Channel	226
4.6.14	TMB - Test Mode Register B-Channel	227
4.6.15	RFIFOB - Receive FIFO B-Channel	228
4.6.16	XFIFOB - Transmit FIFO B-Channel	228
5	Electrical Characteristics	229
5.1	Absolute Maximum Ratings	229
5.2	DC Characteristics	230
5.3	Capacitances	231
5.4	Oscillator Specification	232
5.5	AC Characteristics	233
5.6	IOM-2 Interface Timing	234
5.7	Microcontroller Interface Timing	237
5.7.1	Serial Control Interface (SCI) Timing	237
5.7.2	Parallel Microcontroller Interface Timing	238
5.8	Multiframe Synchronisation Timing	242
5.9	Reset	243
5.10	S-Transceiver	244
5.11	Recommended Transformer Specification	245
5.12	Line Overload Protection	246
5.13	EMC / ESD Aspects	247
6	Package Outlines	248
7	Appendix	250

List of Figures		Page
Figure 1	Logic Symbol of the ISAC-SX	19
Figure 2	Applications of the ISAC-SX	20
Figure 3	Pin Configuration of the ISAC-SX	21
Figure 4	Functional Block Diagram of the ISAC-SX.....	31
Figure 5	Serial Control Interface Timing	33
Figure 6	Serial Control Interface Timing	34
Figure 7	Direct/Indirect Register Address Mode	38
Figure 8	Interrupt Status and Mask Registers	39
Figure 9	Reset Generation.....	41
Figure 10	Timer Interrupt Status Registers	43
Figure 11	Timer 1 Register	44
Figure 12	Timer 2 Register	44
Figure 13	ACL Indication of Activated Layer 1.....	45
Figure 14	ACL Configuration	45
Figure 15	Wiring Configurations in User Premises	47
Figure 16	S/T -Interface Line Code	48
Figure 17	Frame Structure at Reference Points S and T (ITU I.430).....	49
Figure 18	Multiframe Synchronization Using the M-Bit	52
Figure 19	Sampling Time in LT-S / NT mode (M-Bit input)	53
Figure 20	Frame Relationship in LT-S / NT mode (M-Bit input).....	53
Figure 21	Frame Relationship in TE / LT-T mode (M-Bit output).....	54
Figure 22	Data Delay between IOM-2 and S/T Interface (TE mode only)	55
Figure 23	Data Delay between IOM-2 and S/T Interface with S/G Bit Evaluation (TE mode only)	56
Figure 24	Data Delay between IOM-2 and S/T Interface with 8 IOM Channels (LT-S/NT mode only)	57
Figure 25	Data Delay between IOM-2 and S/T Interface with 3 IOM Channels and Maximum Receive Delay(LT-S/NT mode only).....	57
Figure 26	Equivalent Internal Circuit of the Transmitter Stage	58
Figure 27	Equivalent Internal Circuit of the Receiver Stage	59
Figure 28	Connection of Line Transformers and Power Supply to the ISAC-SX.	60
Figure 29	External Circuitry for Transmitter	61
Figure 30	External Circuitry for Symmetrical Receivers.....	62
Figure 31	External Circuitry for Symmetrical Receivers.....	63
Figure 32	Disabling of S/T Transmitter	64
Figure 33	External Loop at the S/T-Interface.....	65
Figure 34	Clock System of the ISAC-SX	66
Figure 35	Phase Relationships of ISAC-SX Clock Signals	69
Figure 36	Buffered Oscillator Clock Output	70
Figure 37	Layer-1 Control	71
Figure 38	State Diagram Notation	72
Figure 39	State Transition Diagram (TE, LT-T)	74

List of Figures	Page
Figure 40	State Transition Diagram of Unconditional Transitions (TE, LT-T) . . . 75
Figure 41	State Transition Diagram (LT-S) 80
Figure 42	State Transition Diagram (NT) 84
Figure 43	Example of Activation/Deactivation Initiated by the Terminal 89
Figure 44	Example of Activation/Deactivation initiated by the Terminal (TE). Activation/Deactivation completely under Software Control 90
Figure 45	Example of Activation/Deactivation initiated by the Network Termination (NT). Activation/Deactivation completely under Software Control 91
Figure 46	IOM [®] -2 Frame Structure in Terminal Mode 93
Figure 47	Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode 94
Figure 48	Architecture of the IOM Handler (Example Configuration). 96
Figure 49	Data Access via CDAX1 and CDAX2 register pairs 98
Figure 50	Examples for Data Access via CDAXy Registers. 99
Figure 51	Data Access when Looping T _{Sa} from DU to DD 100
Figure 52	Data Access when Shifting T _{Sa} to T _{Sb} on DU (DD) 101
Figure 53	Example for Monitoring Data 102
Figure 54	Interrupt Structure of the Synchronous Data Transfer. 104
Figure 55	Examples for the Synchronous Transfer Interrupt Control with one enabled ST _{Ixy} 105
Figure 56	Data Strobe Signal. 108
Figure 57	Strobed IOM-2 Bit Clock. Register SDS_CONF Programmed to 01H 109
Figure 58	Examples of MONITOR Channel Applications in IOM -2 TE Mode . . 110
Figure 59	MONITOR Channel Protocol (IOM-2) 112
Figure 60	Monitor Channel, Transmission Abort requested by the Receiver. . . 115
Figure 61	Monitor Channel, Transmission Abort requested by the Transmitter. 115
Figure 62	Monitor Channel, Normal End of Transmission 116
Figure 63	MONITOR Interrupt Structure 119
Figure 64	CIC Interrupt Structure. 121
Figure 65	Applications of TIC Bus in IOM-2 Bus Configuration 122
Figure 66	Structure of Last Octet of Ch2 on DU 123
Figure 67	Structure of Last Octet of Ch2 on DD 124
Figure 68	D-Channel Access Control on the S-Interface. 125
Figure 69	Data Flow for Collision Resolution Procedure in Intelligent NT 129
Figure 70	Deactivation of the IOM-2 Interface 130
Figure 71	Activation of the IOM-2 interface 131
Figure 72	RFIFO Operation 140
Figure 73	Data Reception Procedures. 142
Figure 74	Reception Sequence Example. 143
Figure 75	Receive Data Flow. 144
Figure 76	Data Transmission Procedure 149
Figure 77	Transmission Sequence Example 150

List of Figures		Page
Figure 78	Transmit Data Flow	151
Figure 79	Interrupt Status Registers of the HDLC Controllers	153
Figure 80	Layer 2 Test Loops	154
Figure 81	Register Mapping of the ISAC-SX	156
Figure 82	Oscillator Circuits	232
Figure 83	Input/Output Waveform for AC Tests	233
Figure 84	IOM-2 Timing (TE mode)	234
Figure 85	IOM-2 Timing (LT-S, LT-T, NT mode)	235
Figure 86	Definition of Clock Period and Width	236
Figure 87	SCI Interface	237
Figure 88	Microprocessor Read Cycle	238
Figure 89	Microprocessor Write Cycle	238
Figure 90	Multiplexed Address Timing	239
Figure 91	Non-Multiplexed Address Timing	239
Figure 92	Microprocessor Read Timing	240
Figure 93	Microprocessor Write Cycle	240
Figure 94	Non-Multiplexed Address Timing	241
Figure 95	Sampling Time in LT-S/NT Mode (M-Bit Input)	242
Figure 96	Reset Signal RES	243
Figure 97	Maximum Line Input Current	246
Figure 98	Transformer Circuitry	247

List of Tables		Page
Table 1	Comparison of the ISAC-SX with the Previous Version ISAC-S	14
Table 2	ISAC-SX Pin Definitions and Functions	22
Table 3	Host Interface Selection	32
Table 4	Header Byte Code	34
Table 5	Bus Operation Modes	37
Table 6	Reset Source Selection	42
Table 7	ISAC-SX Timers	43
Table 8	S/Q-Bit Position Identification and Multiframe Structure	50
Table 9	Clock Modes	67
Table 10	Examples for Synchronous Transfer Interrupts	104
Table 11	CDA Register Combinations with Correct Read/Write Access	106
Table 12	Transmit Direction	111
Table 13	Receive Direction	111
Table 14	ISAC-SX Configuration Settings in Intelligent NT Applications	127
Table 15	AUX Pin Functions	133
Table 16	IOM-2 Channel Selection	134
Table 17	HDLC Controller Address Range	135
Table 18	Receive Byte Count with RBC11...0 in the RBCHx/RBCLx Registers	139
Table 19	Receive Information at RME Interrupt	145
Table 20	XPR Interrupt (availability of XFIFOx) after XTF, XME Commands. .	147

1 Overview

The ISDN Subscriber Access Controller ISAC-SX integrates a D-channel HDLC controller and a four wire S/T interface used to link voice/data terminals to the ISDN. It is based on the ISAC-S PEB 2086, and provides enhanced features and functionality.

It includes the S-transceiver (Layer 1), an HDLC controller for the D-channel and one B-channel protocol controller (HDLC or transparent) with reduced features dedicated for firmware download via the B-channel.

The system integration is simplified by several configurations of the parallel microcontroller interface selected via pin strapping. They include multiplexed and demultiplexed interface selection as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations. The ISAC-SX also provides a serial control interface (SCI).

The FIFO size of the cyclic D-channel buffer is 64 bytes per direction with programmable block size (threshold). Besides TE mode the S-transceiver supports other terminal relevant operation modes like line termination subscriber side (LT-S), line termination trunk side (LT-T) and NT applications (NT, Intelligent NT mode).

An auxiliary I/O port has been added with interrupt capabilities on two input lines. These programmable I/O lines may be used to connect peripheral components to the ISAC-SX which need software control or have to forward status information to the host.

Three programmable LED outputs can be used to indicate certain status information, one of them is capable to indicate the activation status of the S-interface automatically.

The ISAC-SX is produced in advanced CMOS technology.

Table 1 Comparison of the ISAC-SX with the Previous Version ISAC-S

	ISAC-SX PEB 3086	ISAC-S PEB 2086
Operating modes	TE, LT-T, LT-S, NT, Int. NT	TE, LT-T, LT-S, NT
Supply voltage	3.3 V \pm 5%	5 V \pm 5%
Technology	CMOS	CMOS
Package	P-MQFP-64 / P-TQFP-64	P-MQFP-64 / P-LCC-44
Transceiver Transformer ratio for the transmitter receiver	1:1 1:1	2:1 2:1
Test Functions	- Dig. loop via Layer 2 (TLP) - Layer 1 disable (DIS_TR) - Analog loop (LP_A- bit EXLP- bit, ARL)	- Dig. loop via Layer 2(TLP) - Layer 1 disable (DIS_TR) - Analog loop (ARL)
Microcontroller Interface	Serial interface (SCI) 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux direct/ indirect Addressing	Not provided 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux
Command structure of the register access (SCI)	Header/address/data	Address/data
Crystal	7.68 MHz	7.68 MHz
Buffered 7.68 MHz output	Provided	Not provided
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Restricted access to B- and IC-channel
Data control and manipulation	Various possibilities of data control and data manipulation (enable/disable, shifting, looping, switching)	B- and IC-channel looping
IOM-2		

	ISAC-SX PEB 3086	ISAC-S PEB 2086
IOM-2 Interface	Double clock (DCL), bit clock (BCL), serial data strobe 1 (SDS1) serial data strobe 2 (SDS2)	Double clock (DCL), bit clock (BCL), serial data strobe (SDS)
Monitor channel programming	Provided (MON0, 1, 2, ..., 7)	Provided (MON0 or 1)
C/I channels	C10 (4bit), C11 (4/6bit)	C10 (4bit), C11 (6bit)
Layer 1 state machine	With changes for correspondence with the actual ITU specification	
Layer 1 state machine in software	Possible	Not possible
Support of IDSL (144kBit/s)	Provided (HDLC controller access, SDS1/2 signals active)	Not provided
D-channel HDLC support	D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode	D-channel timeslot; auto mode, non-auto mode, transparent mode 1-3
D-channel FIFO size	64 bytes cyclic buffer per direction with programmable FIFO thresholds	2x32 bytes buffer per direction
FW download support	One B-channel controller	Not provided
HDLC support (B-channel)	D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode	Not provided
FIFO size (B-channel)	128 bytes cyclic buffer per direction with programmable FIFO thresholds (8 or 16 bytes)	Not provided
Reset Signals	$\overline{\text{RES}}$ input signal RSTO output signal	RST input/output signal

	ISAC-SX PEB 3086	ISAC-S PEB 2086
Reset Sources	$\overline{\text{RES}}$ Input Watchdog C/I Code Change $\overline{\text{EAW}}$ Pin Software Reset	RST Input Watchdog C/I Code Change EAW Pin
Interrupt Output Signals	$\overline{\text{INT}}$ low active (open drain) by default, reprogrammable to high active (push-pull)	Low active $\overline{\overline{\text{INT}}}$
Pin SCLK	1.536 MHz	512 kHz

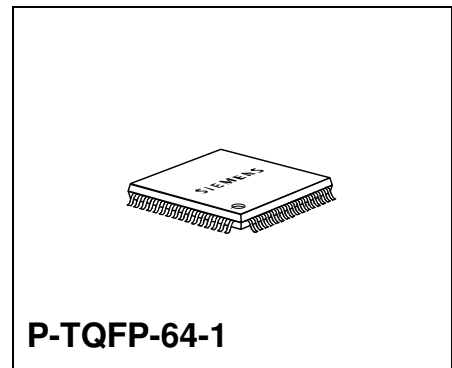
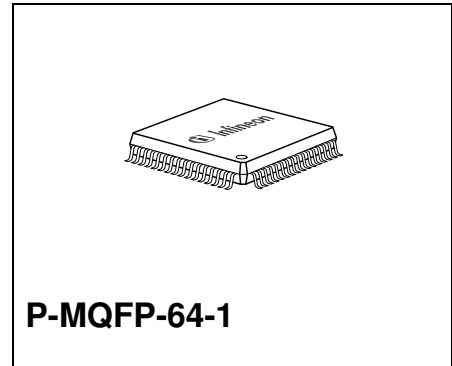
ISAC-SX ISDN Subscriber Access Controller

PEB 3086

V 1.4

1.1 Features

- Full duplex 2B + D S/T interface transceiver according to ITU-T I.430
- Successor of ISAC-S PEB 2086 in 3.3 V technology
- 8-bit parallel microcontroller interface, Motorola and Siemens/Intel bus type multiplexed or non-multiplexed, direct-/indirect register addressing
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Various types of protocol support (Non-auto mode, transparent mode, extended transparent mode)
- One D-channel HDLC controller with 64 byte FIFOs per direction
- One B-channel HDLC controller with reduced functionality (e.g. for firmware upgrades)
- IOM-2 interface in TE, LT-T, LT-S and NT mode, single/double clocks and two strobe signals
- D-channel priority handler on IOM-2 for intelligent NT applications
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Conversion of the frame structure between the S/T-interface and IOM-2
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface
- Adaptively switched receive thresholds



Type	Package
PEB 3086 H	P-MQFP-64-1
PEB 3086 F	P-TQFP-64-1

- Auxiliary Interface with general purpose I/O pins and LED drivers
- Two programmable timers
- Watchdog timer
- Software Reset
- Multiframe Synchronization
- Test loops
- Sophisticated power management for restricted power mode
- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

1.2 Logic Symbol

The logic symbol gives an overview of the ISAC-SX functions. It must be noted that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a “ * “ are multiplexed and not available in all modes.

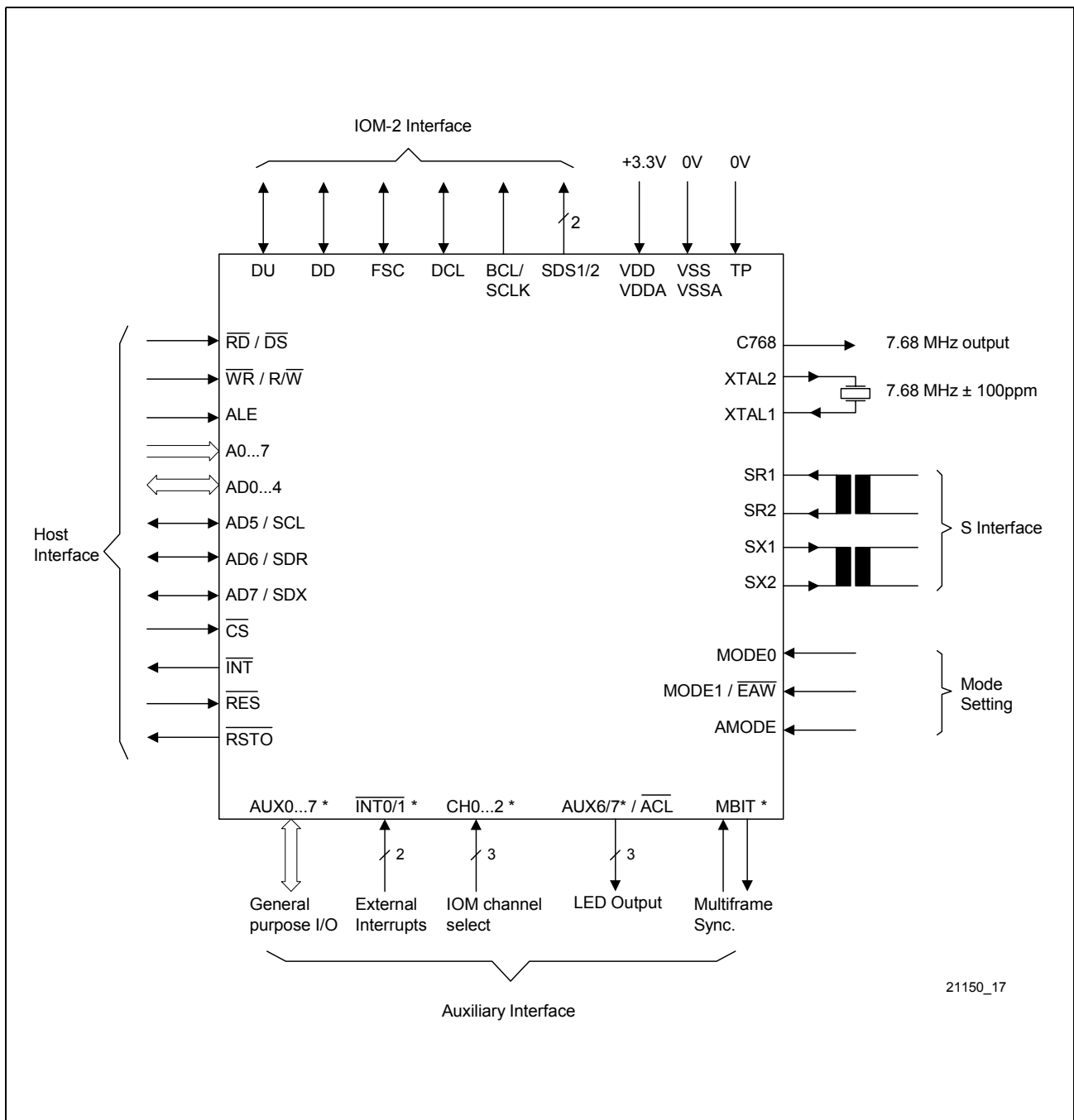


Figure 1 Logic Symbol of the ISAC-SX

1.3 Typical Applications

The ISAC-SX is designed for the user area of the ISDN basic access, especially for subscriber terminal equipment and for exchange equipment with S interface.

Figure 2 illustrates the general application fields of the ISAC-SX.

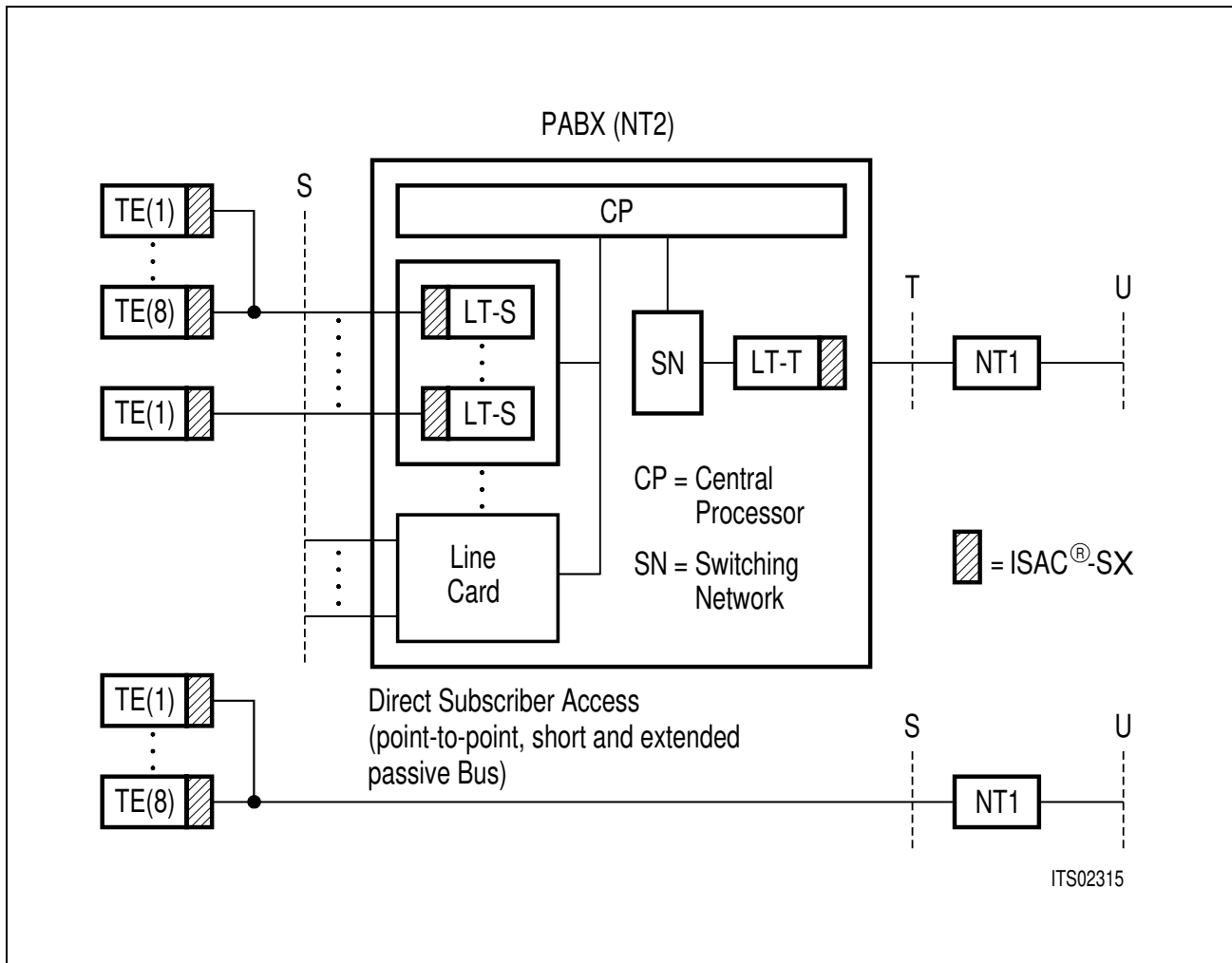


Figure 2 Applications of the ISAC-SX

2 Pin Configuration

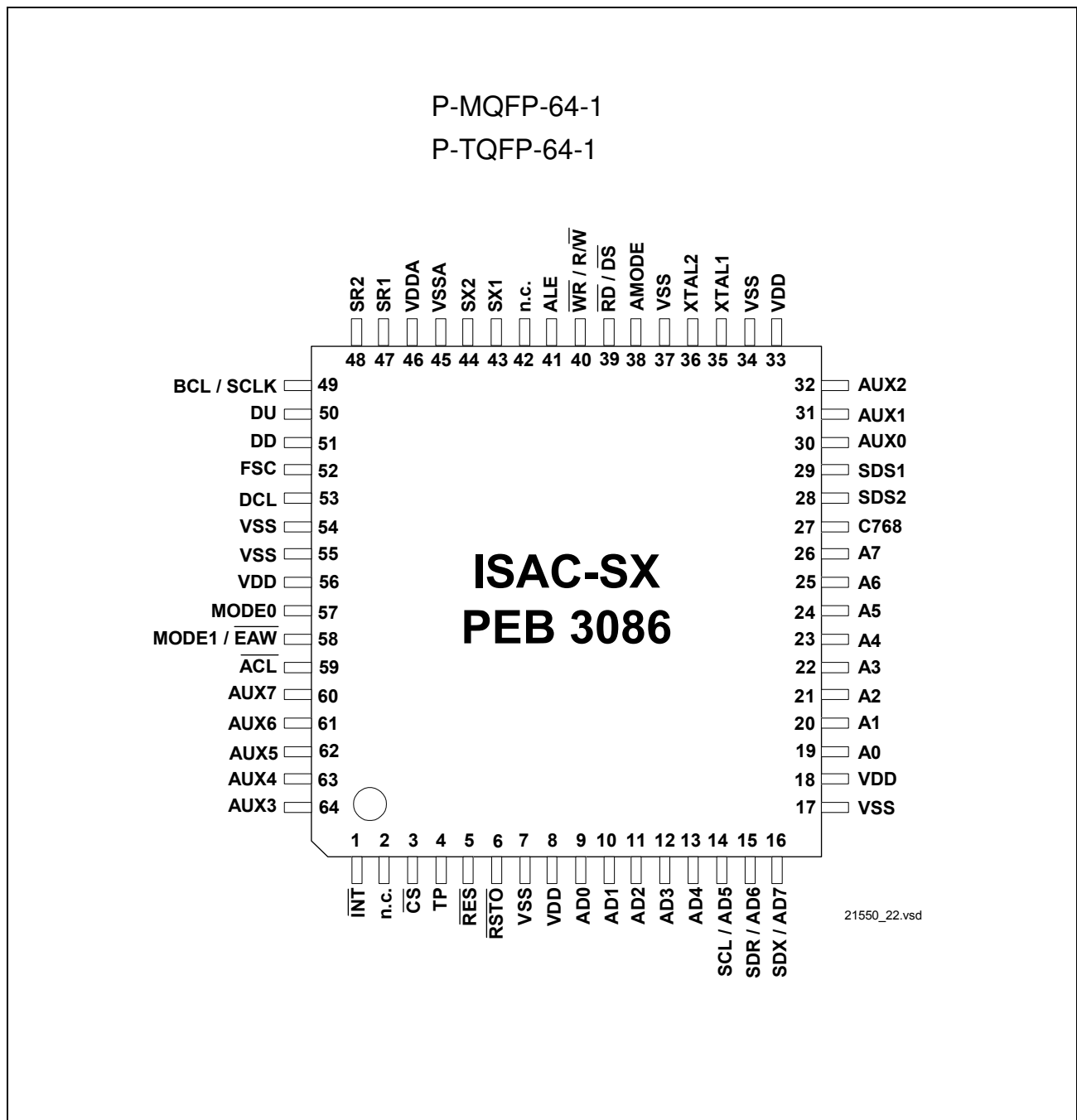


Figure 3 Pin Configuration of the ISAC-SX

Table 2 ISAC-SX Pin Definitions and Functions

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
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Host Interface

19	A0	I	<ul style="list-style-type: none"> • Non-Multiplexed Bus Mode: Address Bus Address bus transfers addresses from the microcontroller to the ISAC-SX. For indirect address mode only A0 is valid (A1-A7 to be connected to VDD). • Multiplexed Bus Mode: Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD.
20	A1	I	
21	A2	I	
22	A3	I	
23	A4	I	
24	A5	I	
25	A6	I	
26	A7	I	
9	AD0	I/O	<ul style="list-style-type: none"> • Multiplexed Bus Mode: Address/data bus Transfers addresses from the microcontroller to the ISAC-SX and data between the microcontroller and the ISAC-SX. • Non-Multiplexed Bus Mode: Data bus Transfers data between the microcontroller and the ISAC-SX.
10	AD1	I/O	
11	AD2	I/O	
12	AD3	I/O	
13	AD4	I/O	
14	AD5	I/O	<ul style="list-style-type: none"> • Multiplexed Bus Mode: Address/data bus Address/data line AD5 if the parallel interface is selected. • Non-Multiplexed Bus Mode: Data bus Data line D5 if the parallel interface is selected.
	SCL	I	

Table 2 ISAC-SX Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
15	AD6 SDR	I/O I	<ul style="list-style-type: none"> • Multiplexed Bus Mode: Address/data bus Address/data line AD6 if the parallel interface is selected. • Non-Multiplexed Bus Mode: Data bus Data line D6 if the parallel interface is selected. SCI - Serial Data Receive Receive data line of the SCI interface if a serial interface is selected.
16	AD7 SDX	I/O OD	<ul style="list-style-type: none"> • Multiplexed Bus Mode: Address/data bus Address/data line AD7 if the parallel interface is selected. • Non-Multiplexed Bus Mode: Data bus Data line D7 if the parallel interface is selected. SCI - Serial Data Transmit Transmit data line of the SCI interface if a serial interface is selected.
39	\overline{RD} \overline{DS}	I I	Read Indicates a read access to the registers (Siemens/ Intel bus mode). Data Strobe The rising edge marks the end of a valid read or write operation (Motorola bus mode).
40	\overline{WR} R/ \overline{W}	I I	Write Indicates a write access to the registers (Siemens/ Intel bus mode). Read/Write A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).

Table 2 ISAC-SX Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
41	ALE	I	Address Latch Enable A HIGH on this line indicates an address on the external address/data bus (multiplexed bus type only). ALE also selects the microcontroller interface bus type (multiplexed or non multiplexed).
3	\overline{CS}	I	Chip Select A low level indicates a microcontroller access to the ISAC-SX.
1	\overline{INT}	OD (O)	Interrupt Request \overline{INT} becomes active low (open drain) if the ISAC-SX requests an interrupt. The polarity can be reprogrammed to high active with push-pull characteristic.
5	\overline{RES}	I	Reset A LOW on this input forces the ISAC-SX into a reset state.
38	AMODE	I	Address Mode Selects between direct (0) and indirect (1) register access mode.

IOM-2 Interface

52	FSC	I/O	Frame Sync 8-kHz frame synchronization signal.
53	DCL	I/O	Data Clock IOM-2 interface clock signal (double clock) (e.g 1.536 MHz in TE mode).

Pin Configuration
Table 2 ISAC-SX Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
49	BCL/ SCLK	O	Bit Clock/S-Clock TE-Mode: Bit clock output, identical to IOM-2 data rate (DCL/2). LT-T Mode: 1.536 MHz output synchronous to S-interface. NT / LT-S Mode: Bit clock output derived from the DCL input clock divided by 2.
51	DD	I/O (OD)	Data Downstream IOM-2 data signal in downstream direction.
50	DU	I/O (OD)	Data Upstream IOM-2 data signal in upstream direction.
29	SDS1	O	Serial Data Strobe 1 Programmable strobe signal for time slot and/or D-channel indication on IOM-2.
28	SDS2	O	Serial Data Strobe 2 Programmable strobe signal for time slot and/or D-channel indication on IOM-2.

Auxiliary Interface

30 31 32	AUX0 AUX1 AUX2	I/O (OD) I/O (OD) I/O (OD)	<ul style="list-style-type: none"> • TE-Mode: Auxiliary Port 0 - 2 (input/output) These pins are individually programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. • LT-T/LT-S/NT Mode: CH0-2 - IOM-2 Channel Select (input) These pins select one of eight channels on the IOM-2 interface.
64	AUX3	I/O (OD)	Auxiliary Port 3 (input/output) This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.