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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# DuSLIC

Dual Channel Subscriber Line  
Interface Concept

PEB 3264, Version 1.4

PEB 3265, Version 1.5

PEB 4264/-2, Version 1.1/1.2

PEB 4364, Version 1.1/1.2

PEB 4265/-2, Version 1.1/1.2

PEB 4365, Version 1.2

PEB 4266, Version 1.2

Wired  
Communications



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## Preliminary Data Sheet

Revision History: 2003-07-11

DS3

Previous Version: DS2

Page	Subjects (major changes since last revision)
Title	Product name corrected to <i>Dual Channel Subscriber Line Interface Concept</i>
all	PEB 3265 version changed from 1.2 to 1.5
all	PEB 4264/-2 and PEB 4265/-2: version 1.2 added
all	PEB 4266 version changed from 1.1 to 1.2
all	PEB 3264 version changed from 1.2 to 1.4
all	Bit VRTLIM renamed to VTRLIM
all	Bit VRTLIM-M renamed to VTRLIM-M
all	New SLICs TSLIC-E and TSLIC-S added
all	New SLICOFI-2 (Version 1.5 only) package P-TQFP-64-1 added
all	New package P-VQFN-48-4 for SLIC-S/-S2, SLIC-E/-E2 and SLIC-P added
all	Former chapter 2 "Pin Descriptions" removed. See updated device data sheets.
<b>Page 18</b>	<b>“Overview” on Page 18:</b> Chapter reworked, tables for codec and SLIC chips added.
<b>Page 23</b>	<b>“Features” on Page 23:</b> ITU-T Recommendation G.712 added
<b>Page 25</b>	<b>“Logic Symbols” on Page 25:</b> Logic symbol for SLIC-E/-E2 Version 1.2 added.
<b>Page 32</b>	<b>“Block Diagram SLICOFI-2/-2S” on Page 32:</b> block diagrams of SLIC devices removed.
<b>Page 33</b>	<b>Figure 10 "Signal Paths – DC Feeding" on Page 33:</b> $C_{ITA}$ ( $C_{ITB}$ ) renamed to $C_{ITACA}$ ( $C_{ITACB}$ ).
<b>Page 38</b>	<b>Table 4 "DC Characteristics" on Page 38:</b> $V_{LIM}$ changed from 50 V to 72 V.
<b>Page 42</b>	<b>Figure 19 "Signal Paths – AC Transmission" on Page 42:</b> $C_{ITA}$ ( $C_{ITB}$ ) renamed to $C_{ITACA}$ ( $C_{ITACB}$ ).
<b>Page 50</b>	<b>“Internal Balanced Ringing via SLICs” on Page 50:</b> $V_{DRO,RT}$ renamed to $V_{DRO,TR}$ , $V_{RT,RMS}$ renamed to $V_{TR,RMS}$ , $V_{RT0,RMS}$ renamed to $V_{TR0,RMS}$
<b>Page 61</b>	<b>Figure 30 "Bellcore On-Hook Caller ID Physical Layer Transmission" on Page 61:</b> note added.
<b>Page 61</b>	<b>“Caller ID Buffer Handling of SLICOFI-2” on Page 61:</b> description for listing item (9) changed
<b>Page 64</b>	<b>“Non Linear Processor (NLP) in DuSLIC-E/-E2/-P” on Page 64</b> added.

<b>Page 66</b>	<b>“MIPS Requirements for EDSP Capabilities” on Page 66</b> updated with NLP examples.
<b>Page 68</b>	<b>“Three-party Conferencing in DuSLIC-E/-E2/-P” on Page 68</b> : sentence about Multi-party Conferencing added
<b>Page 84</b>	<b>“Hardware and Power On Reset” on Page 84</b> : reset routine duration changed to 1.5 ms.
<b>Page 85</b>	<b>Figure 36 "DuSLIC Reset Sequence" on Page 85</b> : textual description changed.
<b>Page 86</b>	<b>Table 17, “Default DC and AC Values” on Page 86</b> : L <sub>X</sub> and L <sub>R</sub> changed.
<b>Page 88</b>	<b>“Recommended Procedure for Reading the Interrupt Registers” on Page 88</b> added.
<b>Page 90</b>	<b>“Power Management and Operating Modes” on Page 90</b> : Power dissipation values and description updated.
<b>Page 94</b>	<b>“Integrated Test and Diagnostic Functions (ITDF)” on Page 94</b> : ITDF is now also available for SLICOFI-2S.
<b>Page 94</b>	<b>Figure 3.8.1.2 "DuSLIC Line Testing" on Page 94</b> : description on line testing capability modified.
<b>Page 97</b>	<b>“Using the Level Metering Integrator” on Page 97</b> : timing for LM-OK bit added.
<b>Page 99</b>	<b>Figure 44, “Timing LM-OK Bit” on Page 99</b> : 1 ms delay time for SLICOFI-2 Version 1.5 added.
<b>Page 101</b>	<b>Table 20 "KINTDC Setting Table" on Page 101</b> : description about DuSLICOS settings added below.
<b>Page 113</b>	<b>“Capacitance Measurements” on Page 113</b> : note on offset calibration added at the end of the chapter.
<b>Page 116</b>	<b>“Line Capacitance Measurements Ring and Tip to GND” on Page 116</b> : description of last list item in section "Calculating parameter values" modified, description in table of section "Program Sequence" modified
<b>Page 137</b>	<b>Chapter 4.2.3, Operation with IOM-2 TE Devices (1.536 MHz)</b> added.
<b>Page 139</b>	<b>“TIP/RING Interface” on Page 139</b> : content removed - see device data sheets for detailed information.
<b>Page 144</b>	<b>“SOP Command” on Page 144</b> : note on empty register bits added
<b>Page 151</b>	Register <b>XCR</b> : Description for bit ASYNCH-R changed
<b>Page 152</b>	Register <b>INTREG1</b> , bits HOOK and GNDK: description changes
<b>Page 154</b>	Register <b>INTREG2</b> : reset value changed from 20 <sub>H</sub> to 4F <sub>H</sub> , description for bit RSTAT modified
<b>Page 167</b>	Register <b>BCR1</b> , bit SLEEP-EN: note added
<b>Page 170</b>	Register <b>BCR2</b> : description added for bits UTDX-SRC and PDOT-DIS
<b>Page 177</b>	Register <b>BCR5</b> , bit DTMF-SRC: description added
<b>Page 179</b>	Register <b>DSCR</b> , bit PTG: description added
<b>Page 203</b>	<b>“COP Command” on Page 203</b> : note on empty register bits added

<b>Page 205</b>	<b>Table 35 "CRAM Coefficients" on Page 205:</b> TTX Slope extended by nibbles 6 and 7
<b>Page 207</b>	<b>"POP Command" on Page 207:</b> note on the necessity of immediate programming added
<b>Page 207</b>	<b>"Sequence for POP Register Programming" on Page 207</b> added (because added NLP coefficients)
<b>Page 208</b>	<b>"POP Register Overview" on Page 208:</b> NLP coefficients added
<b>Page 213</b>	<b>"POP Register Description" on Page 213:</b> NLP coefficients added
<b>Page 233</b>	<b>Table 53 "Range of DeltaPLEC" on Page 233:</b> "0x80 - no detection" added.
<b>Page 248</b>	Register <b>CIS/LEC-MODE</b> : description added for bit UTDX-SUM and note on bit 3 added.
<b>Page 258</b>	<b>"Recommended NLP Coefficients" on Page 258</b> added
<b>Page 266</b>	<b>"SOP Command" on Page 266:</b> note on empty register bits added
<b>Page 273</b>	Register XCR: Description for bit ASYNCH-R changed
<b>Page 278</b>	Register <b>LMRES1</b> : bits added.
<b>Page 278</b>	Register <b>LMRES2</b> : bits added.
<b>Page 287</b>	Register <b>BCR1</b> : bits added.
<b>Page 295</b>	Register <b>DSCR</b> , bit PTG: description added
<b>Page 297</b>	Register <b>LMCR1</b> : bits added.
<b>Page 299</b>	Register <b>LMCR2</b> : bits added.
<b>Page 301</b>	Register <b>LMCR3</b> : bits added.
<b>Page 315</b>	<b>"COP Command" on Page 315:</b> note on empty register bits added
<b>Page 318</b>	<b>Table 73 "CRAM Coefficients" on Page 318:</b> TTX slope extended by nibbles 6 and 7
<b>Page 325</b>	<b>"Electrical Characteristics" on Page 325:</b> SLIC and <i>SLICOFI-2x</i> data removed - for detailed information see device data sheets.
<b>Page 326</b>	<b>Table 76, "AC Transmission" on Page 326:</b> Symbol $V_{RT}$ renamed to $V_{TR}$
<b>Page 331</b>	AC Transmission Characteristics: Values for Distortion and associated figures changed
<b>Page 342</b>	<b>"Input/Output Waveform for AC Tests" on Page 342</b> added.
<b>Page 344</b>	PCM interface timings <b>"Single-Clocking Mode" on Page 344</b> and <b>"Double-Clocking Mode" on Page 346:</b> FSC hold time ( $t_{FSC\_h}$ ) renamed to FSC hold time 1 ( $t_{FSC\_h1}$ ), FSC hold time 2 ( $t_{FSC\_h2}$ ) added, formula of max. value for TCA/B delay time off ( $t_{dTCoFF}$ ) modified
<b>Page 349</b>	IOM-2 interface timings <b>"Single-Clocking Mode" on Page 349</b> and <b>"Double-Clocking Mode" on Page 351:</b> FSC hold time ( $t_{FSC\_h}$ ) renamed to FSC hold time 1 ( $t_{FSC\_h1}$ ), FSC hold time 2 ( $t_{FSC\_h2}$ ) added, parameters and timing of pin DU modified Period PCLK ( $t_{PCLK}$ ) for double clocking: formula for typ. value modified.

<b>Page 353</b>	<b>Figure 90, “Internal (balanced and unbalanced) Ringing with SLIC-P” on Page 353:</b> pin TS2/CS changed to TS2/ $\overline{\text{CS}}$ , illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added, arrangement of diodes D1 and D2 modified.
<b>Page 355</b>	<b>Table 79, “External Components in Application Circuit DuSLIC-E/-E2/-S/-S2/-P” on Page 355:</b> tolerance of $R_{\text{STAB}}$ and $R_{\text{PROT}}$ changed to 1%, footnote added.
<b>Page 357</b>	<b>Figure 92, “External Unbalanced Ringing with SLIC-E/-E2 or SLIC-S/-S2” on Page 357:</b> pin TS2/CS changed to TS2/ $\overline{\text{CS}}$ , illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added
<b>Page 359</b>	<b>Figure 94, “External Unb. Ringing (Long Loops) with SLIC-E/-E2 or SLIC-S/-S2” on Page 359:</b> pin TS2/CS changed to TS2/ $\overline{\text{CS}}$ , illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added
<b>Page 363</b>	<b>Figure 97, “SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x)” on Page 363:</b> note on SLIC clockwise pin counting added, security warning for all SLIC packages added

<b>Table of Contents</b>		<b>Page</b>
<b>1</b>	<b>Overview</b> .....	18
1.1	Features .....	23
1.2	Typical Applications .....	24
1.3	Logic Symbols .....	25
<b>2</b>	<b>Functional Description</b> .....	29
2.1	Functional Overview .....	29
2.1.1	Basic Functions of all DuSLIC Chip Sets .....	29
2.1.2	Additional Functions of the DuSLIC-E/-E2/-P Chip Sets .....	30
2.2	Block Diagram SLICOFI-2/-2S .....	32
2.3	DC Feeding .....	33
2.3.1	DC Characteristic Feeding Zones .....	34
2.3.2	Constant Current Zone .....	35
2.3.3	Resistive Zone .....	36
2.3.4	Constant Voltage Zone .....	37
2.3.5	Programmable Voltage and Current Range: DC Characteristics .....	38
2.3.6	SLIC Power Dissipation .....	39
2.3.7	Necessary Voltage Reserve .....	40
2.3.8	Extended Battery Feeding .....	41
2.4	AC Transmission Characteristics .....	42
2.4.1	Transmit Path .....	43
2.4.2	Receive Path .....	43
2.4.3	Matching .....	44
2.5	Ringling .....	45
2.5.1	Ringer Load .....	45
2.5.2	Ring Trip .....	45
2.5.3	Ringling Methods .....	46
2.5.4	DuSLIC Ringling Options .....	47
2.5.5	Internal Balanced Ringling via SLICs .....	50
2.5.6	Internal Unbalanced Ringling with SLIC-P .....	51
2.5.7	External Unbalanced Ringling .....	52
2.6	Signaling (Supervision) .....	52
2.7	Metering .....	54
2.7.1	Metering by 12/16 kHz Sinusoidal Bursts .....	54
2.7.2	Metering by Polarity Reversal .....	55
2.7.2.1	Soft Reversal .....	55
2.8	DuSLIC Enhanced Signal Processing Capabilities .....	56
2.8.1	DTMF Generation and Detection .....	57
2.8.2	Caller ID Generation in DuSLIC-E/-E2/-P .....	59
2.8.2.1	Caller ID Buffer Handling of SLICOFI-2 .....	61
2.8.3	Line Echo Cancellation in DuSLIC-E/-E2/-P .....	63
2.8.4	Non Linear Processor (NLP) in DuSLIC-E/-E2/-P .....	64
2.8.5	Universal Tone Detection in DuSLIC-E/-E2/-P .....	65



<b>Table of Contents</b>		<b>Page</b>
2.8.6	MIPS Requirements for EDSP Capabilities .....	66
2.9	Message Waiting Indication in DuSLIC-E/-E2/-P .....	67
2.10	Three-party Conferencing in DuSLIC-E/-E2/-P .....	68
2.10.1	Conferencing Modes .....	69
2.11	16 kHz Mode on PCM Highways .....	71
<b>3</b>	<b>Operational Description</b> .....	<b>74</b>
3.1	Overview of all DuSLIC Operating Modes .....	74
3.2	Operating Modes for the DuSLIC-S/-S2/-SE/-SE2 Chip Set .....	78
3.3	Operating Modes for the DuSLIC-E/-E2/-ES/-ES2 Chip Set .....	80
3.4	Operating Modes for the DuSLIC-P Chip Set .....	82
3.5	Reset Mode and Reset Behavior .....	84
3.5.1	Hardware and Power On Reset .....	84
3.5.2	Software Reset .....	86
3.6	Interrupt Handling .....	88
3.6.1	Recommended Procedure for Reading the Interrupt Registers .....	88
3.7	Power Management and Operating Modes .....	90
3.7.1	<i>SLICOFI-2x</i> Power Dissipation .....	91
3.7.2	SLIC Power Dissipation .....	91
3.7.2.1	Power Down Modes .....	91
3.7.2.2	Active Modes .....	92
3.7.2.3	Ringing Mode .....	93
3.8	Integrated Test and Diagnostic Functions (ITDF) .....	94
3.8.1	Introduction .....	94
3.8.1.1	Conventional Line Testing .....	94
3.8.1.2	DuSLIC Line Testing .....	94
3.8.2	Diagnostics .....	95
3.8.2.1	Line Test Capabilities .....	95
3.8.2.2	Integrated Signal Sources .....	95
3.8.2.3	Result Register Data Format .....	97
3.8.2.4	Using the Level Metering Integrator .....	97
3.8.2.5	DC Level Metering .....	100
3.8.2.6	AC Level Meter .....	105
3.8.2.7	Level Meter Threshold .....	108
3.8.2.8	Current Offset Error Compensation .....	110
3.8.2.9	Loop Resistance Measurements .....	111
3.8.2.10	Line Resistance Tip/GND and Ring/GND .....	113
3.8.2.11	Capacitance Measurements .....	113
3.8.2.12	Line Capacitance Measurements Ring and Tip to GND .....	116
3.8.2.13	Foreign- and Ring Voltage Measurements .....	116
3.9	Signal Path and Test Loops .....	119
3.9.1	AC Test Loops .....	119
3.9.2	DC Test Loops .....	121

<b>Table of Contents</b>		<b>Page</b>
<b>4</b>	<b>Interfaces</b> .....	122
4.1	PCM Interface with a Serial Microcontroller Interface .....	122
4.1.1	PCM Interface .....	122
4.1.2	Control of the Active PCM Channels .....	126
4.1.3	Serial Microcontroller Interface .....	127
4.2	The IOM-2 Interface .....	129
4.2.1	IOM-2 Interface Monitor Transfer Protocol .....	133
4.2.2	SLICOFI-2x Identification Command .....	137
4.2.3	Operation with IOM-2 TE Devices (1.536 MHz) .....	137
4.3	TIP/RING Interface .....	139
<b>5</b>	<b>SLICOFI-2x Command Structure and Programming</b> .....	140
5.1	Overview of Commands .....	143
5.2	SLICOFI-2 Command Structure and Programming .....	144
5.2.1	SOP Command .....	144
5.2.1.1	SOP Register Overview .....	144
5.2.1.2	SOP Register Description .....	149
5.2.2	COP Command .....	203
5.2.2.1	CRAM Programming Ranges .....	206
5.2.3	POP Command .....	207
5.2.3.1	Sequence for POP Register Programming .....	207
5.2.3.2	POP Register Overview .....	208
5.2.3.3	POP Register Description .....	213
5.2.3.4	Recommended NLP Coefficients .....	258
5.2.4	IOM-2 Interface Command/Indication Byte .....	260
5.2.5	Programming Examples of the SLICOFI-2 .....	262
5.2.5.1	Microcontroller Interface .....	262
5.2.5.2	IOM-2 Interface .....	263
5.3	SLICOFI-2S Command Structure and Programming .....	266
5.3.1	SOP Command .....	266
5.3.1.1	SOP Register Overview .....	266
5.3.1.2	SOP Register Description .....	271
5.3.2	COP Command .....	315
5.3.2.1	CRAM Programming Ranges .....	319
5.3.3	IOM-2 Interface Command/Indication Byte .....	320
5.3.4	Programming Examples of the SLICOFI-2S .....	322
5.3.4.1	Microcontroller Interface .....	322
5.3.4.2	IOM-2 Interface .....	323
<b>6</b>	<b>Electrical Characteristics</b> .....	325
6.1	AC Transmission DuSLIC .....	325
6.1.1	Frequency Response .....	334
6.1.2	Gain Tracking (Receive or Transmit) .....	335

<b>Table of Contents</b>		<b>Page</b>
6.1.3	Group Delay .....	336
6.1.4	Out-of-Band Signals at Analog Output (Receive) .....	336
6.1.5	Out-of-Band Signals at Analog Input (Transmit) .....	338
6.1.6	Total Distortion Measured with Sine Wave .....	339
6.2	DC Characteristics .....	341
6.3	DuSLIC Power Up .....	342
6.4	DuSLIC Timing Characteristics .....	342
6.4.1	Input/Output Waveform for AC Tests .....	342
6.4.2	MCLK/FSC Timing .....	343
6.4.3	PCM Interface Timing .....	344
6.4.3.1	Single-Clocking Mode .....	344
6.4.3.2	Double-Clocking Mode .....	346
6.4.4	Microcontroller Interface Timing .....	348
6.4.5	IOM-2 Interface Timing .....	349
6.4.5.1	Single-Clocking Mode .....	349
6.4.5.2	Double-Clocking Mode .....	351
<b>7</b>	<b>Application Circuits</b> .....	<b>352</b>
7.1	Internal Ringing (Balanced/Unbalanced) .....	352
7.1.1	Circuit Diagrams Internal Ringing (Balanced & Unbalanced) .....	353
7.1.2	Bill of Materials .....	355
7.2	External Unbalanced Ringing with DuSLIC-E/-E2/-S/-S2/-P .....	356
7.2.1	Circuit Diagrams External Unbalanced Ringing .....	357
7.3	DuSLIC Layout Recommendations .....	361
<b>8</b>	<b>Package Outlines</b> .....	<b>363</b>
<b>9</b>	<b>Terminology</b> .....	<b>369</b>
<b>10</b>	<b>Index</b> .....	<b>371</b>

<b>List of Figures</b>		<b>Page</b>
Figure 1	DuSLIC Chip Set . . . . .	22
Figure 2	Logic Symbol: SLICOFI-2/-2S . . . . .	25
Figure 3	Logic Symbol: SLIC-S/SLIC-S2 (V1.1, V1.2), SLIC-E/SLIC-E2 (V1.1)	26
Figure 4	Logic Symbol: SLIC-E/SLIC-E2 (V1.2) . . . . .	26
Figure 5	Logic Symbol: SLIC-P . . . . .	27
Figure 6	Logic Symbol: TSLIC-S/TSLIC-E . . . . .	28
Figure 7	Line Circuit Functions in the DuSLIC-S/-S2 . . . . .	31
Figure 8	Line Circuit Functions in the DuSLIC-E/-E2/-P . . . . .	31
Figure 9	Block Diagram: SLICOFI-2/-2S (PEB 3265, PEB 3264) . . . . .	32
Figure 10	Signal Paths – DC Feeding . . . . .	33
Figure 11	DC Feeding Characteristic . . . . .	34
Figure 12	Constant Current Zone . . . . .	35
Figure 13	Resistive Zone . . . . .	36
Figure 14	Constant Voltage Zone . . . . .	37
Figure 15	DC Characteristics . . . . .	38
Figure 16	Power Dissipation . . . . .	39
Figure 17	TTX Voltage Reserve Schematic . . . . .	40
Figure 18	DC Feeding Characteristics (ACTH, ACTR) . . . . .	41
Figure 19	Signal Paths – AC Transmission . . . . .	42
Figure 20	Signal Flow in Voice Channel (A) . . . . .	43
Figure 21	Nyquist Diagram . . . . .	44
Figure 22	Typical Ringer Loads of 1 and 5 REN used in USA . . . . .	45
Figure 23	External Ringing Zero Crossing Synchronization . . . . .	49
Figure 24	Balanced Ringing via SLIC-E/-E2, SLIC-S and SLIC-P . . . . .	50
Figure 25	Unbalanced Ringing Signal . . . . .	51
Figure 26	Teletax Injection and Metering . . . . .	54
Figure 27	Soft Reversal (Example for Open Loop) . . . . .	55
Figure 28	DuSLIC AC Signal Path . . . . .	56
Figure 29	DuSLIC EDSP Signal Path . . . . .	56
Figure 30	Bellcore On-Hook Caller ID Physical Layer Transmission . . . . .	61
Figure 31	Line Echo Cancellation Unit Block Diagram . . . . .	63
Figure 32	UTD Functional Block Diagram . . . . .	65
Figure 33	MWI Circuitry with Glow Lamp . . . . .	67
Figure 34	Timing Diagram . . . . .	68
Figure 35	Conference Block for One DuSLIC Channel . . . . .	69
Figure 36	DuSLIC Reset Sequence . . . . .	85
Figure 37	Reading Interrupt Registers . . . . .	89
Figure 38	Typical SLIC Power Dissipation . . . . .	92
Figure 39	DuSLIC Line Testing . . . . .	94
Figure 40	Level Metering Block Diagram . . . . .	96
Figure 41	Single Measurement Sequence (AC & DC Level Metering) . . . . .	97
Figure 42	Continuous Measurement Sequence (DC Level Metering) . . . . .	98

<b>List of Figures</b>		<b>Page</b>
Figure 43	Continuous Measurement Sequence (AC Level Metering) . . . . .	98
Figure 44	Timing LM-OK Bit. . . . .	99
Figure 45	Example Resistance Measurement . . . . .	111
Figure 46	Differential Resistance Measurement . . . . .	112
Figure 47	Capacitance Measurement . . . . .	114
Figure 48	Foreign Voltage Measurement Principle . . . . .	117
Figure 49	AC Test Loops DuSLIC-E/-E2/-P/-ES/-ES2. . . . .	119
Figure 50	AC Test Loops DuSLIC-S/-S2/-SE/-SE2 . . . . .	120
Figure 51	DC Test Loops DuSLIC . . . . .	121
Figure 52	General PCM Interface Timing . . . . .	123
Figure 53	Setting the Slopes in Register PCMC1 . . . . .	125
Figure 54	Serial Microcontroller Interface Write Access . . . . .	128
Figure 55	Serial Microcontroller Interface Read Access . . . . .	128
Figure 56	IOM-2 I/F Timing for up to 16 Voice Channels (Per 8 kHz Frame) . . . . .	130
Figure 57	IOM-2 Interface Timing (DCL = 4096 kHz, Per 8 kHz Frame) . . . . .	131
Figure 58	IOM-2 Interface Timing (DCL = 2048 kHz, Per 8 kHz Frame) . . . . .	131
Figure 59	IOM-2 Interface Monitor Transfer Protocol . . . . .	133
Figure 60	State Diagram of the <i>SLICOFI-2x</i> Monitor Transmitter . . . . .	135
Figure 61	State Diagram of the <i>SLICOFI-2x</i> Monitor Receiver . . . . .	136
Figure 62	PCM/mC Mode used for IOM-2 TE Interface at 1.536 MHz. . . . .	138
Figure 63	Example for Switching Between Different Ring Offset Voltages . . . . .	187
Figure 64	Example for UTD Recognition Timing . . . . .	256
Figure 65	Example for UTD Tone End Detection Timing. . . . .	258
Figure 66	Waveform of Programming Example SOP-Write to Channel 0 . . . . .	262
Figure 67	Waveform of Programming Example SOP Read from Channel 0 . . . . .	263
Figure 68	Example for Switching Between Different Ring Offset Voltages . . . . .	303
Figure 69	Waveform of Programming Example SOP Write to Channel 0 . . . . .	322
Figure 70	Waveform of Programming Example SOP Read from Channel 0 . . . . .	322
Figure 71	Signal Definitions Transmit, Receive . . . . .	325
Figure 72	Overload Compression . . . . .	333
Figure 73	Frequency Response Transmit . . . . .	334
Figure 74	Frequency Response Receive. . . . .	334
Figure 75	Gain Tracking Receive. . . . .	335
Figure 76	Gain Tracking Transmit . . . . .	335
Figure 77	Group Delay Distortion Receive and Transmit. . . . .	336
Figure 78	Out-of-Band Signals at Analog Output (Receive) . . . . .	337
Figure 79	Out-of-Band Signals at Analog Input (Transmit) . . . . .	338
Figure 80	Total Distortion Transmit (LX = 0 dBr) . . . . .	339
Figure 81	Total Distortion Receive (LR = -7 dBr) . . . . .	339
Figure 82	Total Distortion Receive (LR = 0 dBr) . . . . .	340
Figure 83	Waveform for AC Tests . . . . .	342
Figure 84	MCLK/FSC-Timing. . . . .	343

<b>List of Figures</b>		<b>Page</b>
Figure 85	PCM Interface Timing – Single-Clocking Mode . . . . .	344
Figure 86	PCM Interface Timing – Double-Clocking Mode . . . . .	346
Figure 87	Microcontroller Interface Timing. . . . .	348
Figure 88	IOM-2 Interface Timing – Single-Clocking Mode . . . . .	349
Figure 89	IOM-2 Interface Timing – Double-Clocking Mode . . . . .	351
Figure 90	Internal (balanced and unbalanced) Ringing with SLIC-P . . . . .	353
Figure 91	Internal (balanced) Ringing with SLIC-E/-E2 or SLIC-S/-S2 . . . . .	354
Figure 92	External Unbalanced Ringing with SLIC-E/-E2 or SLIC-S/-S2. . . . .	357
Figure 93	External Unbalanced Ringing with SLIC-P . . . . .	358
Figure 94	External Unb. Ringing (Long Loops) with SLIC-E/-E2 or SLIC-S/-S2 . . . . .	359
Figure 95	External Unbalanced Ringing (Long Loops) with SLIC-P . . . . .	360
Figure 96	DuSLIC Layout Recommendation . . . . .	362
Figure 97	SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x) . . . . .	363
Figure 98	SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB426x). . . . .	364
Figure 99	TSLIC-S (PEB 4364) . . . . .	365
Figure 100	TSLIC-E (PEB 4365) . . . . .	366
Figure 101	<i>SLICOFI-2x</i> (PEB 3265, PEB 3264) . . . . .	367
Figure 102	<i>SLICOFI-2x</i> (PEB 3265, PEB 3264) . . . . .	368

<b>List of Tables</b>	<b>Page</b>
Table 1	Codec Feature Overview . . . . . 19
Table 2	SLIC Feature Overview . . . . . 19
Table 3	DuSLIC Chip Sets Presented in this Data Sheet . . . . . 20
Table 4	DC Characteristics . . . . . 38
Table 5	Ringing Options with SLIC-S, SLIC-E/-E2 and SLIC-P . . . . . 47
Table 6	Performance Characteristics of the DTMF Decoder Algorithm . . . . . 58
Table 7	FSK Modulation Characteristics. . . . . 60
Table 8	MIPS Requirements. . . . . 66
Table 9	Conferencing Modes: Receive Channels. . . . . 69
Table 10	Conferencing Modes: Transmit Channels . . . . . 70
Table 11	Possible Modes in PCM/∞C Interface Mode: Receive Channels . . . . . 72
Table 12	Possible Modes in PCM/∞C Interface Mode: Transmit Channels . . . . . 72
Table 13	Overview of all DuSLIC Operating Modes . . . . . 74
Table 14	DuSLIC-S/-S2/-SE/-SE2 Operating Modes . . . . . 78
Table 15	DuSLIC-E/-E2/-ES/-ES2 Operating Modes . . . . . 80
Table 16	DuSLIC-P Operating Modes . . . . . 82
Table 17	Default DC and AC Values . . . . . 86
Table 18	Level Metering Result Value Range . . . . . 97
Table 19	Selecting DC Level Meter Path . . . . . 100
Table 20	KINTDC Setting Table . . . . . 101
Table 21	NSamples Setting Table . . . . . 102
Table 22	Level Meter Results with and without Integrator Function . . . . . 103
Table 23	Selecting AC Level Meter Path . . . . . 105
Table 24	KINTAC Setting Table . . . . . 106
Table 25	KTG Setting Table . . . . . 108
Table 26	Threshold Setting Table. . . . . 109
Table 27	Measurement Input Selection . . . . . 117
Table 28	<i>SLICOFI-2x</i> PCM Interface Configuration . . . . . 124
Table 29	Active PCM Channel Configuration Bits . . . . . 126
Table 30	IOM-2 Time Slot Assignment. . . . . 132
Table 31	M2, M1, M0: General Operating Mode . . . . . 141
Table 32	Valid DTMF Keys (Bit DTMF-KEY4 = 1) . . . . . 155
Table 33	DTMF Keys . . . . . 179
Table 34	Typical Usage for the three Ring Offsets . . . . . 187
Table 35	CRAM Coefficients. . . . . 205
Table 36	CRAM Programming Ranges . . . . . 206
Table 37	Range of $T_{POW-LPF}$ . . . . . 215
Table 38	Range of $T_{wist_{acc}}$ . . . . . 216
Table 39	Range of $T_{POW-LPS}$ . . . . . 217
Table 40	Range of PowBN-LEV-X . . . . . 218
Table 41	Range of PowBN-LEV-R . . . . . 220
Table 42	Range of TBN-INC. . . . . 221

<b>List of Tables</b>	<b>Page</b>
Table 43	Range of TBN-DEC . . . . . 223
Table 44	Ranges of GDTMF[dB] dependent on “e” . . . . . 224
Table 45	Example for DTMF-GAIN Calculation . . . . . 224
Table 46	Range of PowBN-MAX . . . . . 225
Table 47	Range for DeltaBN-ADJ . . . . . 226
Table 48	Range of ERLRE-MIN . . . . . 227
Table 49	Range of ERLRE-EST . . . . . 228
Table 50	Range of SSD-LEV-X . . . . . 230
Table 51	Range of PowLECR . . . . . 231
Table 52	Range of SSD-LEV-R . . . . . 232
Table 53	Range of DeltaPLEC . . . . . 233
Table 54	Range of DeltaSD-LEV-BN . . . . . 234
Table 55	Examples for DeltaQ . . . . . 235
Table 56	Range of DeltaSD-LEV-RE . . . . . 236
Table 57	Ranges of GLEC-XI[dB] Dependent on “e” . . . . . 237
Table 58	Example for LEC-GAIN-XI Calculation . . . . . 237
Table 59	Range of tSD-OT-DT . . . . . 238
Table 60	Ranges of GLEC-RI[dB] Dependent on “e” . . . . . 239
Table 61	Example for LEC-GAIN-RI Calculation . . . . . 239
Table 62	Range of TERL-LIN-LP . . . . . 240
Table 63	Ranges of GLEC-X0[dB] Dependent on “e” . . . . . 241
Table 64	Example for LEC-GAIN-X0 Calculation . . . . . 241
Table 65	Range of TERL-LEC-LP . . . . . 242
Table 66	Range of DeltaCT-LEV-RE . . . . . 243
Table 67	Range of LevCIS . . . . . 245
Table 68	UTD Inband/Outband Attenuation . . . . . 254
Table 69	Recommended NLP Coefficients . . . . . 259
Table 70	M2, M1, M0: General Operating Mode . . . . . 260
Table 71	DTMF Keys . . . . . 295
Table 72	Typical Usage for the three Ring Offsets . . . . . 303
Table 73	CRAM Coefficients . . . . . 318
Table 74	CRAM Programming Ranges . . . . . 319
Table 75	M2, M1, M0: General Operating Mode . . . . . 320
Table 76	AC Transmission . . . . . 326
Table 77	Group Delay Absolute Values: Signal level 0 dBm0 . . . . . 336
Table 78	DC Characteristics . . . . . 341
Table 79	External Components in Application Circuit DuSLIC-E/-E2/-S/-S2/-P 355



## Preface

This Preliminary Data Sheet describes the family of DuSLIC chip sets. Each chip set comprises a dual channel *SLICOFI-2x* codec and two single- or one dual-channel SLICs. For more DuSLIC related documents, please see our webpage at <http://www.infineon.com/duslic>.

To simplify matters, the following synonyms are used:

*SLICOFI-2x*: Synonym used for all codec versions SLICOFI-2/-2S

SLIC: Synonym used for all SLIC versions SLIC-S/-S2, TSLIC-S, SLIC-E/-E2,

TSLIC-E and SLIC-P.

***Attention: The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4364) and SLIC-E (PEB 4365) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in the specification, also TSLIC-S and TSLIC-E can be deployed.***

## Organization of this Document

- **Chapter 1, Overview**  
A general description of the chip set, the key features, and some typical applications.
- **Chapter 2, Functional Description**  
The main functions of the chip set are presented with functional block diagrams.
- **Chapter 3, Operational Description**  
A brief description of the operating modes, the power management, and the integrated test and diagnostic functions.
- **Chapter 4, Interfaces**  
Connection information including standard IOM-2 and PCM interface timing frames and pins.
- **Chapter 5, SLICOFI-2x Command Structure and Programming**  
A general description of the *SLICOFI-2x* command structure.
- **Chapter 6, Electrical Characteristics**  
Parameters, symbols, and limit values are provided for the chip set.
- **Chapter 7, Application Circuits**  
External components and layout recommendations are identified. Illustrations of balanced ringing, unbalanced ringing, and protection circuits are included.
- **Chapter 8, Package Outlines**  
Illustrations and dimensions of the package outlines.

- **Chapter 9, Terminology**  
List of abbreviations and descriptions of symbols.
- **Chapter 10, Index**

## 1 Overview

DuSLIC is a family of communications chip sets. Each chip set comprises one dual-channel *SLICOFI-2x* codec and two single-channel SLICs or one dual-channel TSLIC. It is a highly flexible codec/SLIC solution for an analog line circuit and is easily programmable via software. Users can now serve different markets with a single hardware design that meets all standards worldwide.

The key benefits of the DuSLIC family include:

### Integrated DSP Features

- Line echo cancellation (up to 8 ms)
- DTMF
- Caller-ID
- Full V.90 performance

### Integrated Ringing

- Balanced ringing up to 85 Vrms
- Unbalanced ringing up to 50 Vrms
- Full support for external ringing

### Smallest Footprint

- Only 121 mm<sup>2</sup> per channel
- Minimum external components

### System Features

- Test & diagnostic functions (complete AC & DC)
- Time-slot assignment on two PCM highways

### Proven Technology

- A single hardware design meets/exceeds worldwide requirements.
- 15+ years experience.
- Several million lines deployed worldwide.

The DuSLIC family allows any combination of the codec and SLIC chips shown in [Table 1](#) and [Table 2](#).

**Table 1      Codec Feature Overview**

<b>Features</b>	<b>SLICOFI-2</b>	<b>SLICOFI-2S</b>
Number of Voice Channels	2	2
DTMF Detection	Yes	No
Line Echo Cancellation (up to 8 ms)	Yes	No
Caller-ID Generation	Yes	No
Integrated Test and Diagnostics (Linetesting)	Yes	Yes
Modem (V.90) transmission	Yes	Yes
Modem tone detection	Yes	No
Metering pulses (TTX)	up to 2.5 Vrms	up to 1.2 Vrms
PCM/Serial Controller Interface	Yes	Yes
IOM2 Interface	Yes	Yes
Internal Ring Support	Yes	Yes
External Ringing Support	Yes	Yes
Supply Voltage	3.3 V	3.3 V

**Table 2      SLIC Feature Overview**

<b>Features</b>	<b>SLIC-S/ TSLIC-S<sup>1)</sup></b>	<b>SLIC-S2<sup>2)</sup></b>	<b>SLIC-E/ TSLIC-E<sup>3)</sup></b>	<b>SLIC-E2<sup>4)</sup></b>	<b>SLIC-P</b>
Maximum DC Feeding	32 mA	50 mA	32 mA	50 mA	32 mA
Maximum Ringing Voltage (balanced)	45 Vrms	45 Vrms	85 Vrms	85 Vrms	85 Vrms
Maximum Ringing Voltage (unbalanced)	–	–	–	–	50 Vrms
Longitudinal Balance	53 dB	60 dB	53 dB	60 dB	53 dB
Supply Voltages (negative/positive)	2/1	2/1	2/1	2/1	3/0
Supply Voltage	3.3 V... 5 V	3.3 V... 5 V	5.0 V	5.0 V	3.3 V
External Ring Support	Yes	Yes	Yes	Yes	Yes

**Table 2 SLIC Feature Overview (cont'd)**

Features	SLIC-S/ TSLIC-S <sup>1)</sup>	SLIC-S2 <sup>2)</sup>	SLIC-E/ TSLIC-E <sup>3)</sup>	SLIC-E2 <sup>4)</sup>	SLIC-P
Technology	90 V	90 V	170 V	170 V	170 V
On-Hook Transmission	Yes	Yes	Yes	Yes	Yes
Current Limitation	105 mA	105 mA	105 mA	105 mA	60/90 mA
Target Application	Low Cost CPE	Linecard (external ringing)	CPE	Linecard	Low Power CPE

- 1) Same specifications as SLIC-S, but two voice channels
- 2) Chip marked as PEB 4264 – packaging unit labeled with PEB 4264-2.
- 3) Same specifications as SLIC-E, but two voice channels
- 4) Chip marked as PEB 4265 – packaging unit labeled with PEB 4265-2.

To allow the most cost effective and feature optimized design the following table presents the available SLIC and Codec combinations. The choice of different combinations meets world wide design requirements.

**Table 3 DuSLIC Chip Sets Presented in this Data Sheet**

Chip Set	DuSLIC-S/ -S2	DuSLIC- SE/-SE2	DuSLIC- ES/-ES2	DuSLIC-E/ -E2	DuSLIC-P
Marketing Name	SLICOFI-2S/ SLIC-S/-S2 (TSLIC-S) <sup>1)</sup>	SLICOFI-2S/ SLIC-E/-E2 (TSLIC-E) <sup>2)</sup>	SLICOFI-2/ SLIC-S/-S2 (TSLIC-S) <sup>1)</sup>	SLICOFI-2/ SLIC-E/-E2 (TSLIC-E) <sup>2)</sup>	SLICOFI-2/ SLIC-P
Product ID	PEB 3264/ PEB 4264/-2 (PEB 4364)	PEB 3264/ PEB 4265/-2 (PEB 4365)	PEB 3265/ PEB 4264/-2 (PEB 4364)	PEB 3265/ PEB 4265/-2 (PEB 4365)	PEB 3265/ PEB 4266

- 1) Single channel SLIC-S or dual channel TSLIC-S package
  - 2) Single channel SLIC-E or dual channel TSLIC-E package
- The DuSLIC chip sets presented in this Data Sheet are differentiated in terms of the DSP features and ringing voltage :
    - DuSLIC-S (Standard)
    - DuSLIC-SE (Standard Codec, Enhanced SLIC)
    - DuSLIC-ES (Enhanced Codec, Standard SLIC)
    - DuSLIC-E (Enhanced)
    - DuSLIC-P (Power Management).

- For both the DuSLIC-S and DuSLIC-E there are also long-haul versions, offering increased longitudinal balance (60 dB) :
  - DuSLIC-E2 (using SLIC-E2)
  - DuSLIC-S2 (using SLIC-S2)

### Usage of Codecs and SLICs

The DuSLIC-S and DuSLIC-S2 chip sets use the SLICOFI-2S (PEB 3264) codec offering full basic POTS functionality, including programmable AC and DC characteristics, integrated ringing and Integrated Test & Diagnostic Functions (ITDF) etc.

The DuSLIC-E, DuSLIC-E2, and DuSLIC-P chip sets use the same SLICOFI-2 (PEB 3265) codec with full EDSP (Enhanced Digital Signal Processor) features such as DTMF detection, Caller ID generation, Universal Tone Detection (UTD) and Line Echo Cancellation (LEC).

These codecs (SLICOFI-2 and SLICOFI-2S) are manufactured using an advanced 0.35  $\mu\text{m}$  3.3 V CMOS process.

The main criteria for choosing the appropriate SLIC device, are the ringing voltage and longitudinal balance.

- SLIC-S and SLIC-S2 offer balanced ringing (up to 45 Vrms)
- SLIC-E and SLIC-E2 offer balanced ringing (up to 85 Vrms)
- SLIC-P offers both balanced (85Vrms) and unbalanced ringing (50 Vrms)  
*Note: the above ring voltages are achievable with 20 Vdc offset. Smaller dc offset will increase the maximum achievable ring voltage*

The SLIC-S2 and SLIC-E2 are optimized for longhaul applications, and offer a minimum of 60 dB longitudinal balance.

All Infineon SLICs are manufactured in our well-proven 90 V and 170 V Smart Power Technology (SPT) processes.

### Dual-channel SLICs : TSLIC-S & TSLIC-E

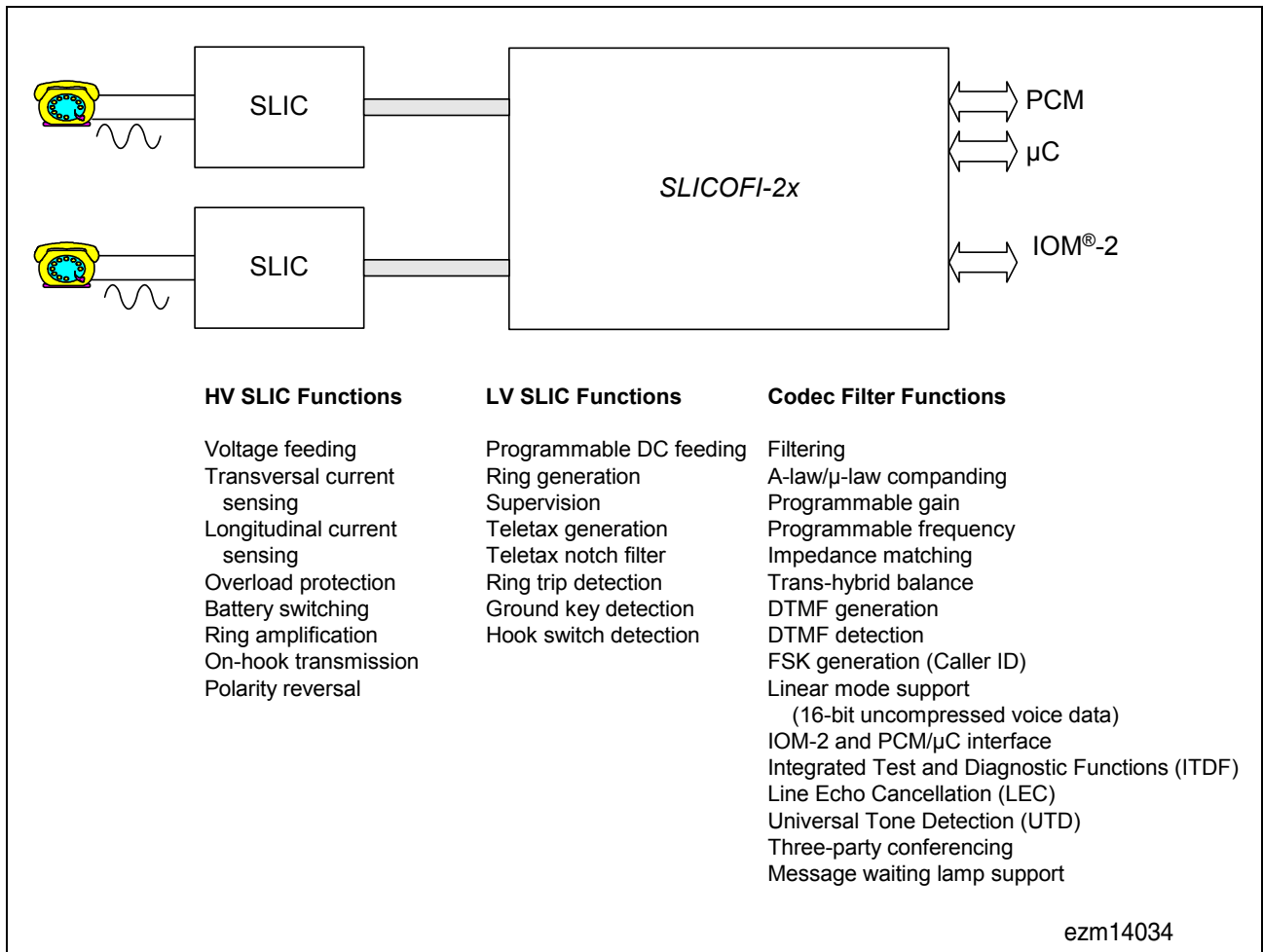
The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4264) and SLIC-E (PEB 4265) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in this and other DuSLIC documentation, also TSLIC-S and TSLIC-E can be deployed.

### DuSLIC Architecture

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC functions and low-voltage SLIC functions.

The low-voltage functions are handled in the *SLICOFI-2x* device. The partitioning of the functions is shown in [Figure 1](#).

For further information see [Chapter 2.1](#).



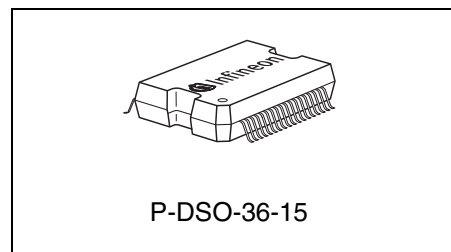
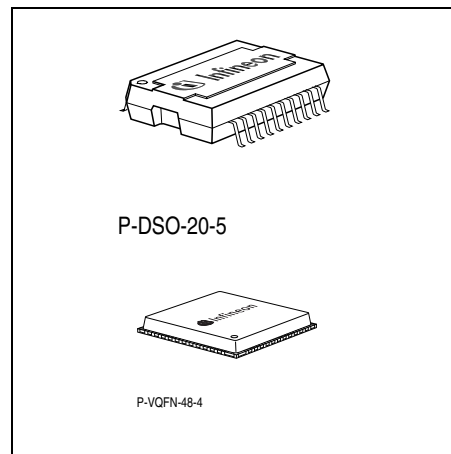
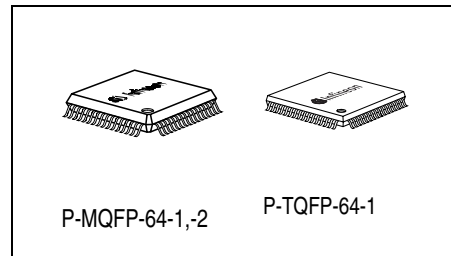
**Figure 1 DuSLIC Chip Set**

## Dual Channel Subscriber Line Interface Concept DuSLIC

PEB 3264  
PEB 3265  
PEB 4264/-2  
PEB 4364  
PEB 4265/-2  
PEB 4365  
PEB 4266

### 1.1 Features

- Fully programmable dual-channel codec
- Programmable AC and DC characteristics
- Integrated Test and Diagnostic Functions (ITDF)
- Programmable integrated ringing : Balanced (85 Vrms) and/or Unbalanced (50 Vrms)
- Programmable Teletax (TTX) generation
- Programmable battery feeding with capability for driving longer loops
- Ground start/loop start signaling supported
- Polarity reversal (hard or soft)
- On-hook transmission
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID generator (FSK or DTMF)
- Universal Tone Detection (UTD) - fax/modem detection
- Integrated Line Echo Cancellation (LEC) up to 8 ms
- Optimized filter structure for modem transmission
- Three-party conferencing (in PCM/ $\mu$ C mode)
- Message waiting lamp support (PBX)
- Power optimized architecture
- Power management capability (integrated battery switches)



Type	Package
PEB 3264	P-MQFP-64-1 or P-TQFP-64-1
PEB 3265	P-MQFP-64-1 or P-TQFP-64-1
PEB 4264/-2	P-DSO-20-5 or P-VQFN-48-4
PEB 4364	P-DSO-36-15
PEB 4265/-2	P-DSO-20-5 or P-VQFN-48-4
PEB 4365	P-DSO-36-15
PEB 4266	P-DSO-20-5 or P-VQFN-48-4



- 8 kHz and 16 kHz PCM Transmission
- IOM-2 or PCM/ $\mu$ C Interface selectable
- G.711 A-law /  $\mu$ -law companding
- Specifications: ITU-T G.712, Q.552, LSSGR, TR57

## 1.2 Typical Applications

DuSLIC offers an optimized solution for various applications. The following main applications can be highlighted:

- Access Networks
  - Central Office (CO)
  - Next-Generation Digital Subscriber Line Access Module (NG-DSLAM)
  - Digital Loop Carrier (DLC)
  - Wireless Local Loop (WLL)
  - Fiber in the Loop (FITL)
  - Digital Added Main Line (DAML) / PCM-x
  - Multi-dwelling / Multi-tenant units (MDU / MTU)
- Customer Premises Equipment
  - Private Branch Exchange (PBX)
  - Integrated Access Device (IAD)
  - Voice over Packet (VoDSL, VoIP, VoATM, etc.)
  - ISDN Intelligent Network Termination (iNT)
  - ISDN Terminal Adapter (TA)
  - Cable Modem
  - xDSL NT
  - Router

### 1.3 Logic Symbols

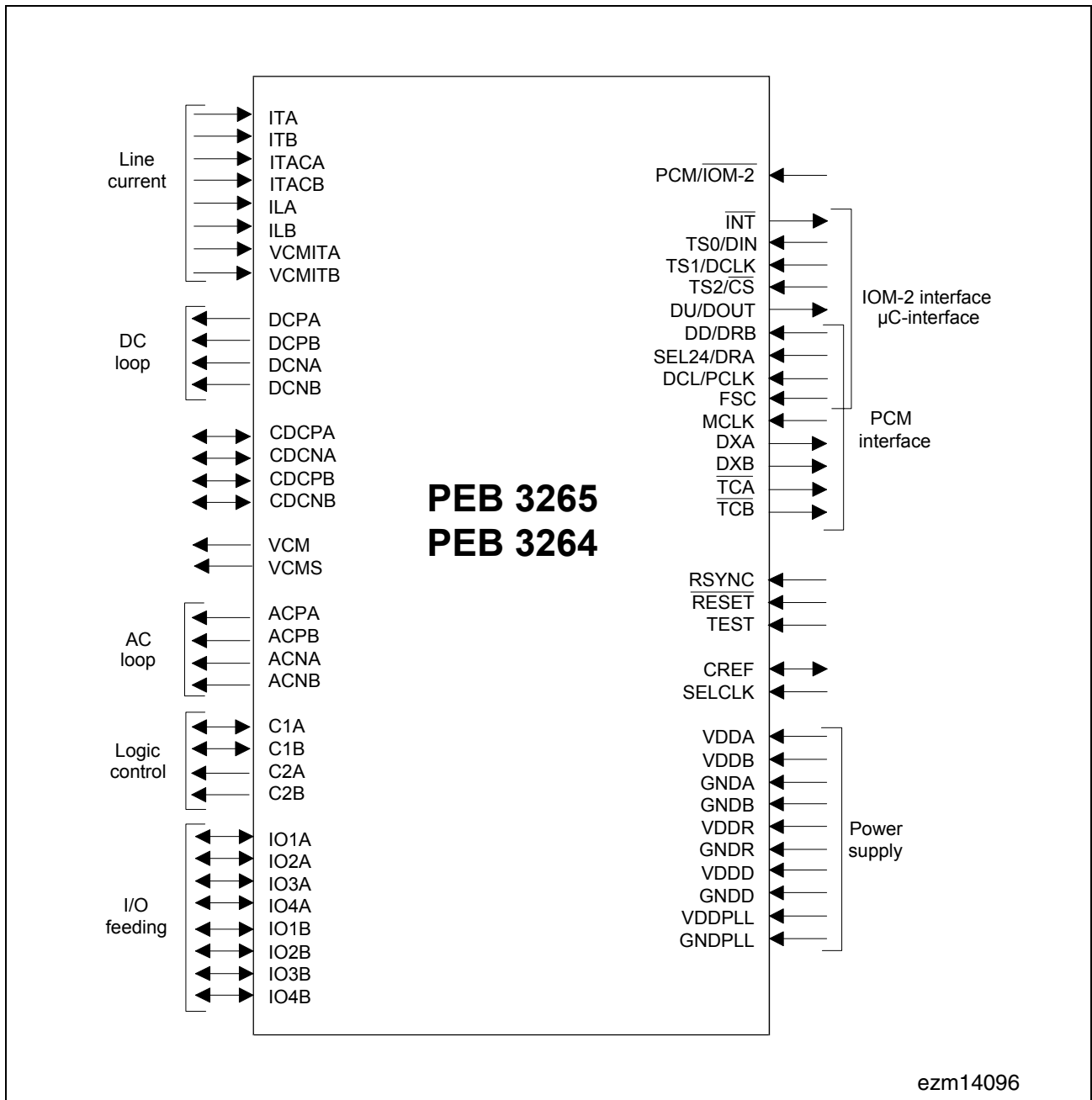


Figure 2 Logic Symbol: SLICOFI-2/-2S