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Preliminary Data Sheet, DS3, July 2003

# DuSLIC

## Dual Channel Subscriber Line Interface Concept

PEB 3264, Version 1.4

PEB 3265, Version 1.5

PEB 4264/-2, Version 1.1/1.2

PEB 4364, Version 1.1/1.2

PEB 4265/-2, Version 1.1/1.2

PEB 4365, Version 1.2

PEB 4266, Version 1.2

Wired Communications

Never stop thinking.

**Edition 2003-07-11**

**Published by Infineon Technologies AG,**
**St.-Martin-Strasse 53,**
**81669 München, Germany**



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**Preliminary Data Sheet**

**Revision History: 2003-07-11** DS3

Previous Version: DS2

| Page | Subjects (major changes since last revision) |
|---|---|
| Title | Product name corrected to *Dual Channel Subscriber Line Interface Concept* |
| all | PEB 3265 version changed from 1.2 to 1.5 |
| all | PEB 4264/-2 and PEB 4265/-2: version 1.2 added |
| all | PEB 4266 version changed from 1.1 to 1.2 |
| all | PEB 3264 version changed from 1.2 to 1.4 |
| all | Bit VRTLIM renamed to VTRLIM |
| all | Bit VRTLIM-M renamed to VTRLIM-M |
| all | New SLICs TSLIC-E and TSLIC-S added |
| all | New SLICOFI-2 (Version 1.5 only) package P-TQFP-64-1 added |
| all | New package P-VQFN-48-4 for SLIC-S/-S2, SLIC-E/-E2 and SLIC-P added |
| all | Former chapter 2 "Pin Descriptions" removed. See updated device data sheets. |
| **Page 18** | **“Overview” on Page 18**: Chapter reworked, tables for codec and SLIC chips added. |
| **Page 23** | **“Features” on Page 23**: ITU-T Recommendation G.712 added |
| **Page 25** | **“Logic Symbols” on Page 25**: Logic symbol for SLIC-E/-E2 Version 1.2 added. |
| **Page 32** | **“Block Diagram SLICOFI-2/-2S” on Page 32**: block diagrams of SLIC devices removed. |
| **Page 33** | **Figure 10 "Signal Paths – DC Feeding" on Page 33**: $C_{ITA}$ ($C_{ITB}$) renamed to $C_{ITACA}$ ($C_{ITACB}$). |
| **Page 38** | **Table 4 "DC Characteristics" on Page 38**: $V_{LIM}$ changed from 50 V to 72 V. |
| **Page 42** | **Figure 19 "Signal Paths – AC Transmission" on Page 42**: $C_{ITA}$ ($C_{ITB}$) renamed to $C_{ITACA}$ ($C_{ITACB}$). |
| **Page 50** | **“Internal Balanced Ringing via SLICs” on Page 50**: $V_{DROP,RT}$ renamed to $V_{DROP,TR}$, $V_{RT,RMS}$ renamed to $V_{TR,RMS}$, $V_{RT0,RMS}$ renamed to $V_{TR0,RMS}$ |
| **Page 61** | **Figure 30 "Bellcore On-Hook Caller ID Physical Layer Transmission" on Page 61**: note added. |
| **Page 61** | **“Caller ID Buffer Handling of SLICOFI-2” on Page 61**: description for listing item (9) changed |
| **Page 64** | **“Non Linear Processor (NLP) in DuSLIC-E/-E2/-P” on Page 64** added. |

| | |
|---|---|
| **Page 66** | **“MIPS Requirements for EDSP Capabilities” on Page 66** updated with NLP examples. |
| **Page 68** | **“Three-party Conferencing in DuSLIC-E/-E2/-P” on Page 68**: sentence about Multi-party Conferencing added |
| **Page 84** | **“Hardware and Power On Reset” on Page 84**: reset routine duration changed to 1.5 ms. |
| **Page 85** | **Figure 36 "DuSLIC Reset Sequence" on Page 85**: textual description changed. |
| **Page 86** | **Table 17**, **“Default DC and AC Values” on Page 86**: $L_X$ and $L_R$ changed. |
| **Page 88** | **“Recommended Procedure for Reading the Interrupt Registers” on Page 88** added. |
| **Page 90** | **“Power Management and Operating Modes” on Page 90**: Power dissipation values and description updated. |
| **Page 94** | **“Integrated Test and Diagnostic Functions (ITDF)” on Page 94**: ITDF is now also available for SLICOFI-2S. |
| **Page 94** | **Figure 3.8.1.2 "DuSLIC Line Testing" on Page 94**: description on line testing capability modified. |
| **Page 97** | **“Using the Level Metering Integrator” on Page 97**: timing for LM-OK bit added. |
| **Page 99** | **Figure 44**, **“Timing LM-OK Bit” on Page 99**: 1 ms delay time for SLICOFI-2 Version 1.5 added. |
| **Page 101** | **Table 20 "KINTDC Setting Table" on Page 101**: description about DuSLICOS settings added below. |
| **Page 113** | **“Capacitance Measurements” on Page 113**: note on offset calibration added at the end of the chapter. |
| **Page 116** | **“Line Capacitance Measurements Ring and Tip to GND” on Page 116**: description of last list item in section "Calculating parameter values" modified, description in table of section "Program Sequence" modified |
| **Page 137** | **Chapter 4.2.3**, **Operation with IOM-2 TE Devices (1.536 MHz)** added. |
| **Page 139** | **“TIP/RING Interface” on Page 139**: content removed - see device data sheets for detailed information. |
| **Page 144** | **“SOP Command” on Page 144**: note on empty register bits added |
| **Page 151** | Register **XCR**: Description for bit ASYNCH-R changed |
| **Page 152** | Register **INTREG1**, bits HOOK and GNDK: description changes |
| **Page 154** | Register **INTREG2**: reset value changed from $20_H$ to $4F_H$, description for bit RSTAT modified |
| **Page 167** | Register **BCR1**, bit SLEEP-EN: note added |
| **Page 170** | Register **BCR2**: description added fot bits UTDX-SRC and PDOT-DIS |
| **Page 177** | Register **BCR5**, bit DTMF-SRC: description added |
| **Page 179** | Register **DSCR**, bit PTG: description added |
| **Page 203** | **“COP Command” on Page 203**: note on empty register bits added |

| | |
|---|---|
| **Page 205** | **Table 35 "CRAM Coefficients" on Page 205**: TTX Slope extended by nibbles 6 and 7 |
| **Page 207** | **“POP Command” on Page 207**: note on the necessity of immediate programming added |
| **Page 207** | **“Sequence for POP Register Programming” on Page 207** added (because added NLP coefficients) |
| **Page 208** | **“POP Register Overview” on Page 208**: NLP coefficients added |
| **Page 213** | **“POP Register Description” on Page 213**: NLP coefficients added |
| **Page 233** | **Table 53 "Range of DeltaPLEC" on Page 233**: "0x80 - no detection" added. |
| **Page 248** | Register **CIS/LEC-MODE**: description added for bit UTDX-SUM and note on bit 3 added. |
| **Page 258** | **“Recommended NLP Coefficients” on Page 258** added |
| **Page 266** | **“SOP Command” on Page 266**: note on empty register bits added |
| **Page 273** | Register XCR: Description for bit ASYNCH-R changed |
| **Page 278** | Register **LMRES1**: bits added. |
| **Page 278** | Register **LMRES2**: bits added. |
| **Page 287** | Register **BCR1**: bits added. |
| **Page 295** | Register **DSCR**, bit PTG: description added |
| **Page 297** | Register **LMCR1**: bits added. |
| **Page 299** | Register **LMCR2**: bits added. |
| **Page 301** | Register **LMCR3**: bits added. |
| **Page 315** | **“COP Command” on Page 315**: note on empty register bits added |
| **Page 318** | **Table 73 "CRAM Coefficients" on Page 318**: TTX slope extended by nibbles 6 and 7 |
| **Page 325** | **“Electrical Characteristics” on Page 325**: SLIC and *SLICOFI-2x* data removed - for detailed information see device data sheets. |
| **Page 326** | **Table 76**, **“AC Transmission” on Page 326**: Symbol $V_{RT}$ renamed to $V_{TR}$ |
| **Page 331** | AC Transmission Characteristics: Values for Distortion and associated figures changed |
| **Page 342** | **“Input/Output Waveform for AC Tests” on Page 342** added. |
| **Page 344** | PCM interface timings **“Single-Clocking Mode” on Page 344** and **“Double-Clocking Mode” on Page 346**:<br>FSC hold time ($t_{FSC\_h}$) renamed to FSC hold time 1 ($t_{FSC\_h1}$),<br>FSC hold time 2 ($t_{FSC\_h2}$) added, formula of max. value for TCA/B delay time off ($t_{dTCoff}$) modified |
| **Page 349** | IOM-2 interface timings **“Single-Clocking Mode” on Page 349** and **“Double-Clocking Mode” on Page 351**:<br>FSC hold time ($t_{FSC\_h}$) renamed to FSC hold time 1 ($t_{FSC\_h1}$),<br>FSC hold time 2 ($t_{FSC\_h2}$) added, parameters and timing of pin DU modified<br>Period PCLK ($t_{PCLK}$) for double clocking: formula for typ. value modified. |

| | |
|---|---|
| **Page 353** | **Figure 90, “Internal (balanced and unbalanced) Ringing with SLIC-P” on Page 353**: pin TS2/CS changed to TS2/$\overline{CS}$, illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added, arrangement of diodes D1 and D2 modified. |
| **Page 355** | **Table 79, “External Components in Application Circuit DuSLIC-E/-E2/-S/-S2/-P” on Page 355**: tolerance of $R_{STAB}$ and $R_{PROT}$ changed to 1%, footnote added. |
| **Page 357** | **Figure 92, “External Unbalanced Ringing with SLIC-E/-E2 or SLIC-S/-S2” on Page 357**: pin TS2/CS changed to TS2/$\overline{CS}$, illustration of connection between pins C3 and IO2A modified,SLIC supply voltages added |
| **Page 359** | **Figure 94, “External Unb. Ringing (Long Loops) with SLIC-E/-E2 or SLIC-S/-S2” on Page 359**: pin TS2/CS changed to TS2/$\overline{CS}$, illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added |
| **Page 363** | **Figure 97, “SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x)” on Page 363**: note on SLIC clockwise pin counting added, security warning for all SLIC packages added |

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# Preface

This Preliminary Data Sheet describes the family of DuSLIC chip sets. Each chip set comprises a dual channel *SLICOFI-2x* codec and two single- or one dual-channel SLICs. For more DuSLIC related documents, please see our webpage at http://www.infineon.com/duslic.

To simplify matters, the following synonyms are used:

*SLICOFI-2x:* Synonym used for all codec versions SLICOFI-2/-2S

SLIC: Synonym used for all SLIC versions SLIC-S/-S2, TSLIC-S, SLIC-E/-E2,

TSLIC-E and SLIC-P.

***Attention: The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4364) and SLIC-E (PEB 4365) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in the specification, also TSLIC-S and TSLIC-E can be deployed.***

### Organization of this Document

- **Chapter 1, Overview**
  A general description of the chip set, the key features, and some typical applications.
- **Chapter 2, Functional Description**
  The main functions of the chip set are presented with functional block diagrams.
- **Chapter 3, Operational Description**
  A brief description of the operating modes, the power management, and the integrated test and diagnostic functions.
- **Chapter 4, Interfaces**
  Connection information including standard IOM-2 and PCM interface timing frames and pins.
- **Chapter 5, SLICOFI-2x Command Structure and Programming**
  A general description of the *SLICOFI-2x* command structure.
- **Chapter 6, Electrical Characteristics**
  Parameters, symbols, and limit values are provided for the chip set.
- **Chapter 7, Application Circuits**
  External components and layout recommendations are identified. Illustrations of balanced ringing, unbalanced ringing, and protection circuits are included.
- **Chapter 8, Package Outlines**
  Illustrations and dimensions of the package outlines.

- **Chapter 9**, **Terminology**
  List of abbreviations and descriptions of symbols.
- **Chapter 10**, **Index**

# 1 Overview

DuSLIC is a family of communications chip sets. Each chip set comprises one dual-channel *SLICOFI-2x* codec and two single-channel SLICs or one dual-channel TSLIC. It is a highly flexible codec/SLIC solution for an analog line circuit and is easily programmable via software. Users can now serve different markets with a single hardware design that meets all standards worldwide.

The key benefits of the DuSLIC family include:

### Integrated DSP Features

- Line echo cancellation (up to 8 ms)
- DTMF
- Caller-ID
- Full V.90 performance

### Integrated Ringing

- Balanced ringing up to 85 Vrms
- Unbalanced ringing up to 50 Vrms
- Full support for external ringing

### Smallest Footprint

- Only 121 mm² per channel
- Minimum external components

### System Features

- Test & diagnostic functions (complete AC & DC)
- Time-slot assignment on two PCM highways

### Proven Technology

- A single hardware design meets/exceeds worldwide requirements.
- 15+ years experience.
- Several million lines deployed worldwide.

The DuSLIC family allows any combination of the codec and SLIC chips shown in Table 1 and Table 2.

**Table 1 Codec Feature Overview**

| Features | SLICOFI-2 | SLICOFI-2S |
|---|---|---|
| Number of Voice Channels | 2 | 2 |
| DTMF Detection | Yes | No |
| Line Echo Cancellation (up to 8 ms) | Yes | No |
| Caller-ID Generation | Yes | No |
| Integrated Test and Diagnostics (Linetesting) | Yes | Yes |
| Modem (V.90) transmission | Yes | Yes |
| Modem tone detection | Yes | No |
| Metering pulses (TTX) | up to 2.5 Vrms | up to 1.2 Vrms |
| PCM/Serial Controller Interface | Yes | Yes |
| IOM2 Interface | Yes | Yes |
| Internal Ring Support | Yes | Yes |
| External Ringing Support | Yes | Yes |
| Supply Voltage | 3.3 V | 3.3 V |

**Table 2 SLIC Feature Overview**

| Features | SLIC-S/ TSLIC-S[1)] | SLIC-S2[2)] | SLIC-E/ TSLIC-E[3)] | SLIC-E2[4)] | SLIC-P |
|---|---|---|---|---|---|
| Maximum DC Feeding | 32 mA | 50 mA | 32 mA | 50 mA | 32 mA |
| Maximum Ringing Voltage (balanced) | 45 Vrms | 45 Vrms | 85 Vrms | 85 Vrms | 85 Vrms |
| Maximum Ringing Voltage (unbalanced) | – | – | – | – | 50 Vrms |
| Longitudinal Balance | 53 dB | 60 dB | 53 dB | 60 dB | 53 dB |
| Supply Voltages (negative/positive) | 2/1 | 2/1 | 2/1 | 2/1 | 3/0 |
| Supply Voltage | 3.3 V... 5 V | 3.3 V... 5 V | 5.0 V | 5.0 V | 3.3 V |
| External Ring Support | Yes | Yes | Yes | Yes | Yes |

**Table 2 SLIC Feature Overview** (cont'd)

| Features | SLIC-S/ TSLIC-S[1)] | SLIC-S2[2)] | SLIC-E/ TSLIC-E[3)] | SLIC-E2[4)] | SLIC-P |
|---|---|---|---|---|---|
| Technology | 90 V | 90 V | 170 V | 170 V | 170 V |
| On-Hook Transmission | Yes | Yes | Yes | Yes | Yes |
| Current Limitation | 105 mA | 105 mA | 105 mA | 105 mA | 60/90 mA |
| Target Application | Low Cost CPE | Linecard (external ringing) | CPE | Linecard | Low Power CPE |

1) Same specifications as SLIC-S, but two voice channels

2) Chip marked as PEB 4264 – packaging unit labeled with PEB 4264-2.

3) Same specifications as SLIC-E, but two voice channels

4) Chip marked as PEB 4265 – packaging unit labeled with PEB 4265-2.

To allow the most cost effective and feature optimized design the following table presents the available SLIC and Codec combinations. The choice of different combinations meets world wide design requirements.

**Table 3 DuSLIC Chip Sets Presented in this Data Sheet**

| Chip Set | DuSLIC-S/ -S2 | DuSLIC-SE/-SE2 | DuSLIC-ES/-ES2 | DuSLIC-E/ -E2 | DuSLIC-P |
|---|---|---|---|---|---|
| Marketing Name | SLICOFI-2S/ SLIC-S/-S2 (TSLIC-S)[1)] | SLICOFI-2S/ SLIC-E/-E2 (TSLIC-E)[2)] | SLICOFI-2/ SLIC-S/-S2 (TSLIC-S)[1)] | SLICOFI-2/ SLIC-E/-E2 (TSLIC-E)[2)] | SLICOFI-2/ SLIC-P |
| Product ID | PEB 3264/ PEB 4264/-2 (PEB 4364) | PEB 3264/ PEB 4265/-2 (PEB 4365) | PEB 3265/ PEB 4264/-2 (PEB 4364) | PEB 3265/ PEB 4265/-2 (PEB 4365) | PEB 3265/ PEB 4266 |

1) Single channel SLIC-S or dual channel TSLIC-S package

2) Single channel SLIC-E or dual channel TSLIC-E package

- The DuSLIC chip sets presented in this Data Sheet are differentiated in terms of the DSP features and ringing voltage :
  - DuSLIC-S (Standard)
  - DuSLIC-SE (Standard Codec, Enhanced SLIC)
  - DuSLIC-ES (Enhanced Codec, Standard SLIC)
  - DuSLIC-E (Enhanced)
  - DuSLIC-P (Power Management).

- For both the DuSLIC-S and DuSLIC-E there are also long-haul versions, offering increased longitudinal balance (60 dB) :
  – DuSLIC-E2 (using SLIC-E2)
  – DuSLIC-S2 (using SLIC-S2)

### Usage of Codecs and SLICs

The DuSLIC-S and DuSLIC-S2 chip sets use the SLICOFI-2S (PEB 3264) codec offering full basic POTS functionality, including programmable AC and DC characteristics, integrated ringing and Integrated Test & Diagnostic Functions (ITDF) etc.

The DuSLIC-E, DuSLIC-E2, and DuSLIC-P chip sets use the same SLICOFI-2 (PEB 3265) codec with full EDSP (Enhanced Digital Signal Processor) features such as DTMF detection, Caller ID generation, Universal Tone Detection (UTD) and Line Echo Cancellation (LEC).

These codecs (SLICOFI-2 and SLICOFI-2S) are manufactured using an advanced 0.35 µm 3.3 V CMOS process.

The main criteria for choosing the appropriate SLIC device, are the ringing voltage and longitudinal balance.

- SLIC-S and SLIC-S2 offer balanced ringing (up to 45 Vrms)
- SLIC-E and SLIC-E2 offer balanced ringing (up to 85 Vrms)
- SLIC-P offers both balanced (85Vrms) and unbalanced ringing (50 Vrms)
  *Note: the above ring voltages are achievable with 20 Vdc offset. Smaller dc offset will increase the maximum achievable ring voltage*

The SLIC-S2 and SLIC-E2 are optimized for longhaul applications, and offer a minimum of 60 dB longitudinal balance.
All Infineon SLICs are manufactured in our well-proven 90 V and 170 V Smart Power Technology (SPT) processes.

### Dual-channel SLICs : TSLIC-S & TSLIC-E

The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4264) and SLIC-E (PEB 4265) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in this and other DuSLIC documentation, also TSLIC-S and TSLIC-E can be deployed.

### DuSLIC Architecture

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC functions and low-voltage SLIC functions.

The low-voltage functions are handled in the *SLICOFI-2x* device. The partitioning of the functions is shown in **Figure 1**.

For further information see **Chapter 2.1**.

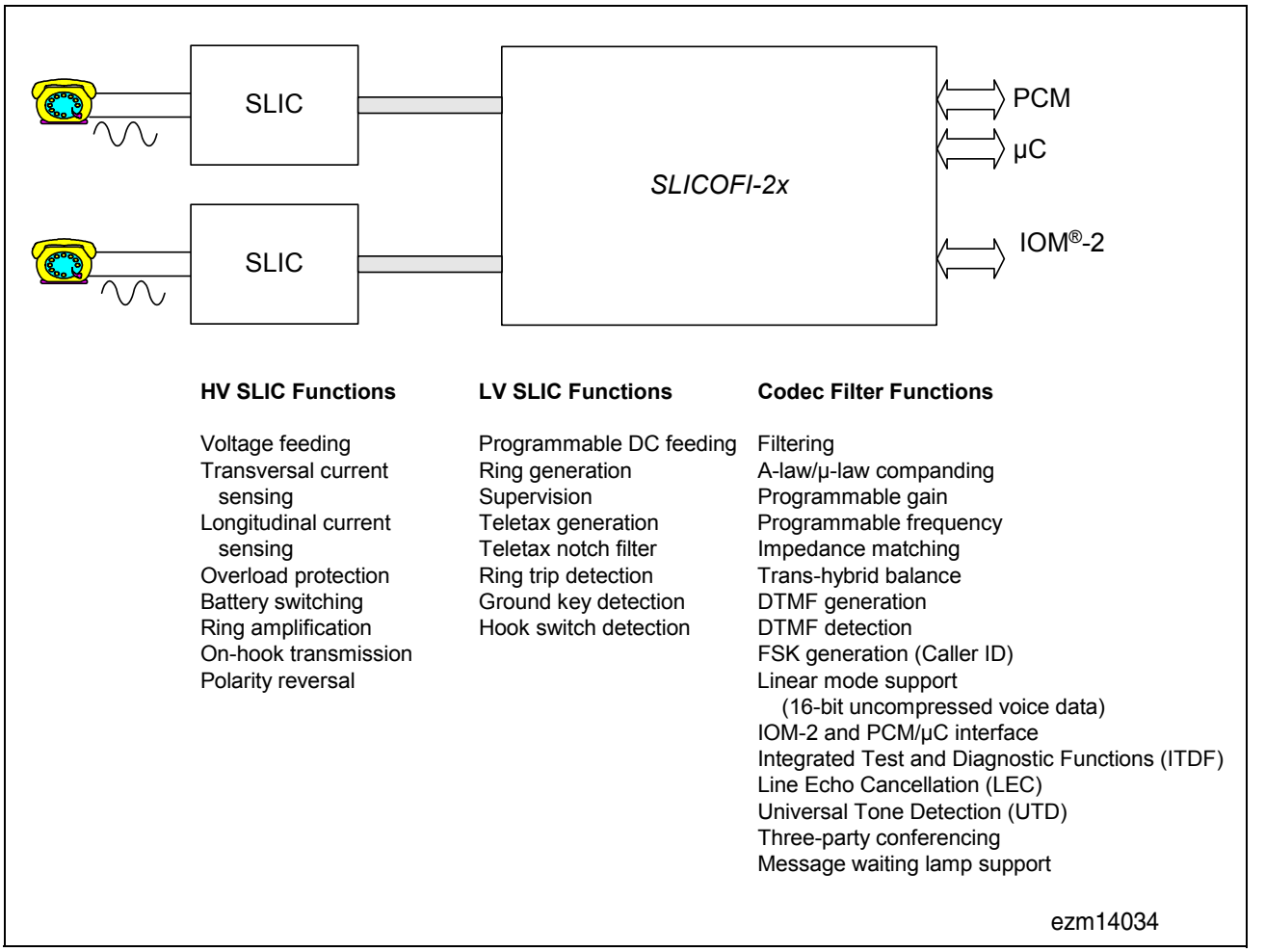


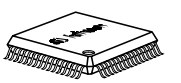

**Figure 1 DuSLIC Chip Set**

**Dual Channel Subscriber Line Interface Concept DuSLIC**

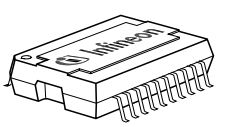
**PEB 3264**
**PEB 3265**
**PEB 4264/-2**
**PEB 4364**
**PEB 4265/-2**
**PEB 4365**
**PEB 4266**

## 1.1 Features

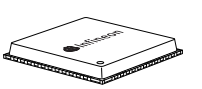
- Fully programmable dual-channel codec
- Programmable AC and DC characteristics
- Integrated Test and Diagnostic Functions (ITDF)
- Programmable integrated ringing : Balanced (85 Vrms) and/or Unbalanced (50 Vrms)
- Programmable Teletax (TTX) generation
- Programmable battery feeding with capability for driving longer loops
- Ground start/loop start signaling supported
- Polarity reversal (hard or soft)
- On-hook transmission
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID generator (FSK or DTMF)
- Universal Tone Detection (UTD) - fax/modem detection
- Integrated Line Echo Cancellation (LEC) up to 8 ms
- Optimized filter structure for modem transmission
- Three-party conferencing (in PCM/µC mode)
- Message waiting lamp support (PBX)
- Power optimized architecture
- Power management capability (integrated battery switches)



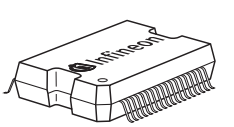
P-MQFP-64-1,-2 P-TQFP-64-1



P-DSO-20-5



P-VQFN-48-4



P-DSO-36-15

| Type | Package |
|---|---|
| PEB 3264 | P-MQFP-64-1 or P-TQFP-64-1 |
| PEB 3265 | P-MQFP-64-1 or P-TQFP-64-1 |
| PEB 4264/-2 | P-DSO-20-5 or P-VQFN-48-4 |
| PEB 4364 | P-DSO-36-15 |
| PEB 4265/-2 | P-DSO-20-5 or P-VQFN-48-4 |
| PEB 4365 | P-DSO-36-15 |
| PEB 4266 | P-DSO-20-5 or P-VQFN-48-4 |

- 8 kHz and 16 kHz PCM Transmission
- IOM-2 or PCM/µC Interface selectable
- G.711 A-law / µ-law companding
- Specifications: ITU-T G.712, Q.552, LSSGR, TR57

## 1.2 Typical Applications

DuSLIC offers an optimized solution for various applications. The following main applications can be highlighted:

- Access Networks
  - Central Office (CO)
  - Next-Generation Digital Subscriber Line Access Module (NG-DSLAM)
  - Digital Loop Carrier (DLC)
  - Wireless Local Loop (WLL)
  - Fiber in the Loop (FITL)
  - Digital Added Main Line (DAML) / PCM-x
  - Multi-dwelling / Multi-tennant units (MDU / MTU)
- Customer Premises Equipment
  - Private Branch Exchange (PBX)
  - Integrated Access Device (IAD)
  - Voice over Packet (VoDSL, VoIP, VoATM, etc.)
  - ISDN Intelligent Network Termination (iNT)
  - ISDN Terminal Adapter (TA)
  - Cable Modem
  - xDSL NT
  - Router

## 1.3 Logic Symbols

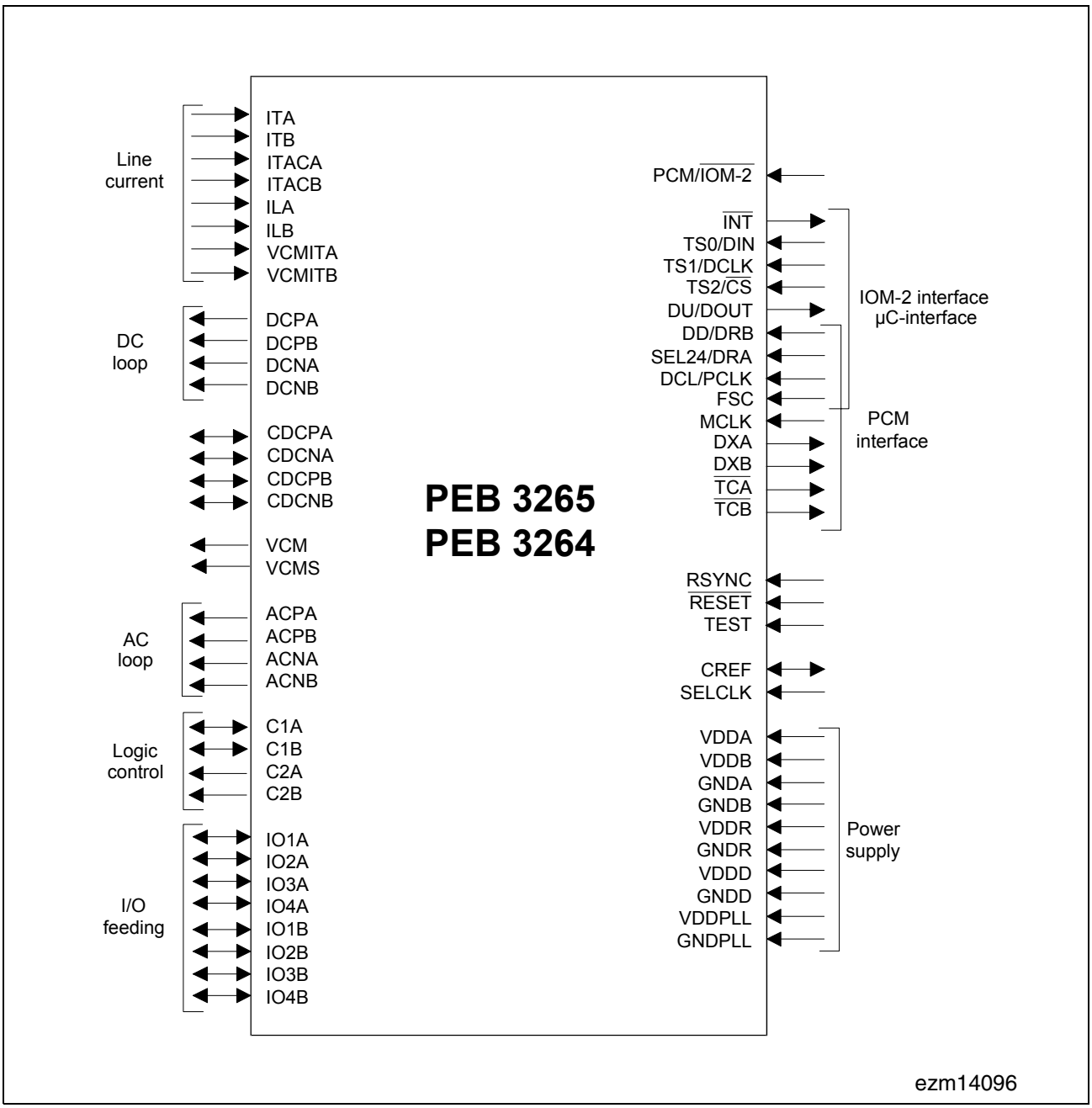



**Figure 2 Logic Symbol: SLICOFI-2/-2S**