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ICs for Communications

Multichannel Network Interface Controller for HDLC
MUNICH32

PEB 20320 Version 3.4

User's Manual 01.2000

DS3

PEB 20320 **Revision History:**		**Current Version: 01.2000**
Previous Version:		User's Manual 1998-06-01 DS2 (V3.4)
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
		Package P-TQFP-176-1 removed from User's Manual.

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide:
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Edition 01.2000

**Published by Infineon Technologies AG,
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Preface

The Multichannel Network Interface Controller for HDLC (MUNICH32) is a Multichannel Protocol Controller for a wide area of telecommunication and data communication applications.

Organization of this Document

This User's Manual is divided into 9 chapters. It is organized as follows:

- Chapter 1, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- Chapter 2, Functional Description
  This chapter provides a detailed description of the interfaces and the protocol modes.
- Chapter 3, Operational Description
  Provides a description of MUNICH32 reset procedure and initialization.
- Chapter 4, Detailed Register Description
  Gives a detailed description of the shared memory organization.
- Chapter 5, Application Notes
- Chapter 6, Application Hints
- Chapter 7, Electrical Characteristics
  Gives a detailed description of all electrical DC and AC characteristics and provides timing diagrams and values for all interfaces.
- Chapter 8, Package Outlines
- Chapter 9, Appendix
  This chapter provides source code examples.

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1 Introduction

The Multichannel Network Interface Controller for HDLC (MUNICH32) is a Multichannel Protocol Controller, which handles up to 32 data channels of a full duplex PCM highway. It performs layer 2 HDLC formatting/deformatting or V.110 and X.30 protocols up to a network data rate of 38.4 Kbit/s as well as transparent transmission for the DMI mode 0, 1 and 2. The processed data is passed on to an external memory shared with one or more host processors.

MUNICH32 is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT as well as with HDLC, SDLC, LAPB DMI protocols. It provides any rate adaption for time slot transmission data rate from 64 Kbit/s down to 8 Kbit/s and the concatenation of any time slots to data channels, supporting the ISDN H0, H11, H12 superchannels.

Due to these functions the MUNICH32 can be used in a wide area of telecommunication and data communication applications, e.g. in central office switches, for the connection of a digital PABX to a host computer, as a central D-channel controller to 32 ISDN basic access D-channels or as a multiplexer for terminals and other peripherals. Up to 4 MUNICH32s can be connected to one PCM highway, so a D-channel controller with 128 channels can be achieved.

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1.1 Features

P-MQFP-160-1

- Serial Interface
  - Up to 32 independent communication channels.
  - Serial multiplexed (full duplex) input/output for 2048-, 4096-, 1544- or 1536-Kbit/s PCM highways.
- Dynamic Programmable Channel Allocation
  - Compatible with T1/DS1 24-channel and CEPT 32-channel PCM byte format.
  - Concatenation of any, not necessarily consecutive, time slots to superchannels independently for receive and transmit direction.
  - Support of H0, H11, H12 ISDN-channels.
  - Subchanneling on each time slot possible.
- Bit Processor Functions (adjustable for each channel)
  - HDLC Protocol
    - Automatic flag detection and transmission
    - Shared opening and closing flag
    - Detection of interframe-time-fill change, generation of interframe-time-fill ‘1’s or flags
    - Zero bit insertion
    - Flag stuffing and flag adjustment for rate adaption
    - CRC generation and checking (16 or 32 bits)
    - Transparent CRC option per channel and/or per message
    - Error detection (abort, long frame, CRC error, 2 categories of short frames, non-octet frame content)
    - Special short frame mode to allow reception of ‘frames’ with a least on byte length
    - ABORT/IDLE generation

Type	Package
PEB 20320	P-MQFP-160-1

  - V.110/X.30 Protocol
    - Automatic synchronization in receive direction, automatic generation of the synchronization pattern in transmit direction
    - E / S / X bits freely programmable in transmit direction, van be changed during transmission; changes monitored and reported in receive direction
    - Generation/detection of loss of synchronism
    - Bit framing with network data rates from 600 bit/s up to 38.4 Kbit/s
  - Transparent Mode A
    - Slot synchronous transparent transmission/reception without frame structure
    - Bit-overwrite with fill/mask bits
    - Flag generation, flag stuffing, flag extraction, flag generation in the abort case with programmable flag
  - Transparent Mode B
    - Transparent transmission/reception in frames delimited by 00_H flags
    - Shared opening and closing flag
    - Flag stuffing, flag detection, flag generation in the abort case
    - Error detection (non octet frame content, short frame, long frame)
  - Transparent Mode R
    - Transparent transmission/reception with GSM 08.60 frame structure
    - Automatic 0000_H flag generation/detection
    - Support of 40, $39^1/_2$, $40^1/_2$ octet frames
    - Error detection (non octet frame content, short frame, long frame)
  - Protocol Independent
    - Channel inversion (data, flags, IDLE code)
    - Format conventions as in CCITT Q.921 § 2.8
    - Data over- and underflow detected
- Processor Interface
  - ON-CHIP 64-channel DMA controller with buffer chaining capability.
  - Compatible with Motorola 68020 processor family and Intel 32-bit processor (80386).
  - 32 bit data bus and 32 bit address bus (4 Gbyte RAM addressable, Motorola and Intel non-parity) or 28 bit address bus (256 Mbyte RAM addressable, Intel parity)
  - Intel parity mode with data byte parity (4 parity bits)
    - Parity check for read accesses
    - Parity generation for write accesses
  - Interrupt-circular buffer with variable size
  - Maskable interrupts for each channel
  - µP interface buffer of depth 16 long words for adaptive bus occupation

- General
  - Connection of up to four MUNICH32 supporting a 128-channel basic access D-channel controller.
  - ON-CHIP receive and transmit data buffer; the buffer size is 256 bytes each.
  - HDLC protocol or transparent mode, support of ECMA 102, CCITT I4.63 RA2, V.110, X.30, DMI mode 0, 1, 2 (bit rate adaption), GSM 08.60 TRAU frames.
  - LOOP mode, complete loop as well as single channel loop
  - JTAG boundary scan test
  - Advanced low-power CMOS technology
  - TTL-compatible inputs/outputs
  - 160 pin P-MQFP package

1.2 Pin Configuration

(top view)

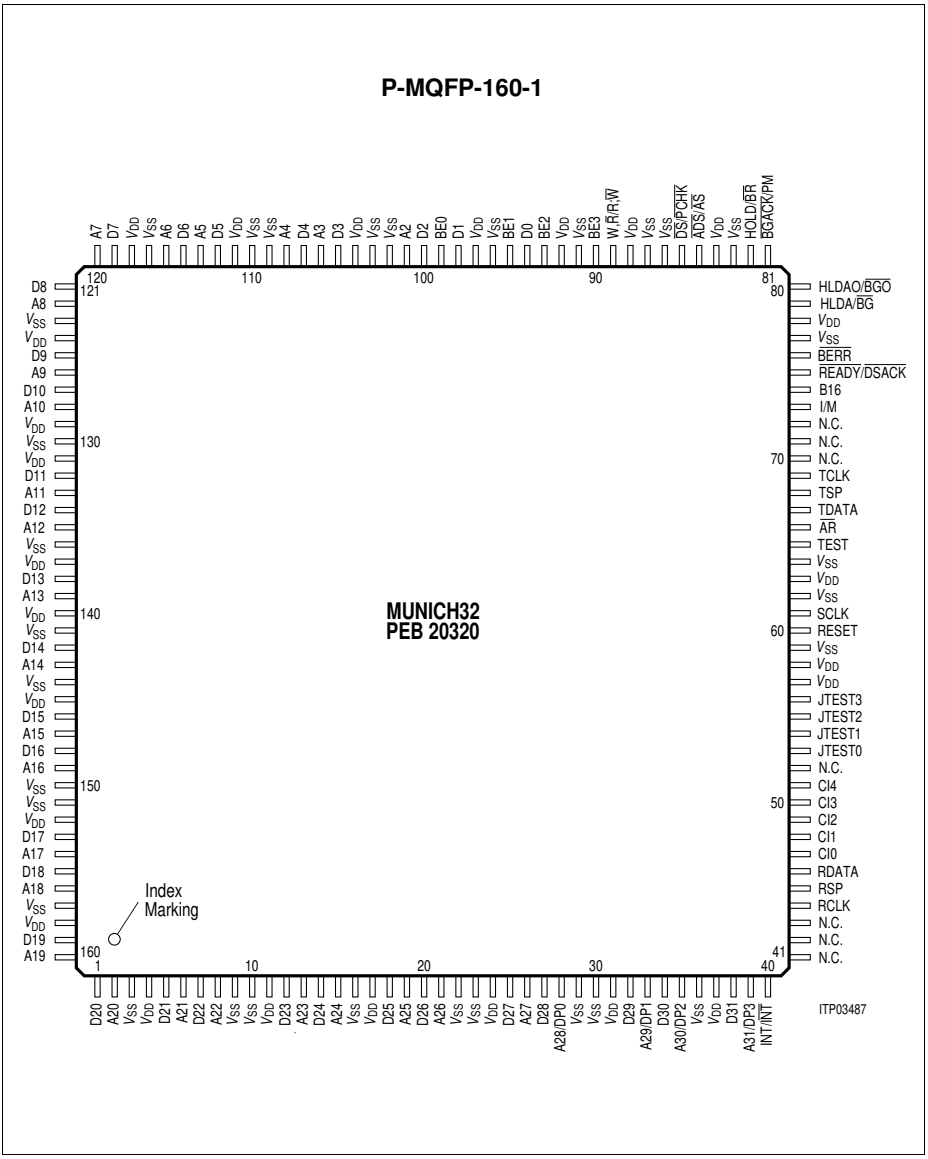

Figure 1

1.3 Pin Definitions and Functions

Pin Definitions and Functions

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
83, 87, 88, 92, 97, 103, 104, 110, 111, 117, 123, 130, 136, 141, 144, 150, 151, 157, 3, 9, 10, 16, 22, 23, 29, 30, 36, 59, 62, 64, 77	V_{SS}	I	**Ground** (0 V) All pins must have the same level.
73	I/M	I	**Intel Bus Mode or Motorola Bus Mode** By connecting this pin to either V_{SS} or V_{DD} the bus interface can be adapted to either Intel or Motorola environment. The data is interpreted either in Intel or Motorola manner; i.e. little or big endian convention. I/M = low: Intel bus mode I/M = high: Motorola bus mode
39	A31 DP3	O I/O	**Address Bit 31** (Intel non-parity/Motorola) tristate when unused. **Data Parity 3** (Intel parity mode), bidirectional tristate line containing/ expecting parity bit of D(31:24).
35	A30 DP2	O I/O	**Address Bit 30** (Intel non-parity/Motorola) tristate when unused. **Data Parity 2** (Intel parity mode), bidirectional tristate line containing/ expecting parity bit of D(23:16).

Note: Input pins that are unused in a specific configuration must be strapped to V_{SS}. I/O or output pins that are unused in a specific configuration must be left open!

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
33	A29	O	**Address Bit 29** (Intel non-parity/Motorola) tristate when unused.
	DP1	I/O	**Data Parity 1** (Intel parity mode), bidirectional tristate line containing/ expecting parity bit of D(15:8)
28	A28	O	**Address Bit 28** (Intel non-parity/Motorola) tristate when unused
	DP0	I/O	**Data Parity 0** (Intel parity mode), bidirectional tristate line containing/ expecting parity bit of D(7:0)
26, 21, 19, 15, 13, 8, 6, 2, 160, 156, 154, 149, 147, 143, 139, 135, 133, 128, 126, 122, 120, 116, 114, 109, 107, 102	A(27:2)	O	**Address Bus** tristate when unused.
91, 94, 96, 100	BE(3:0)	O	**Byte Enable** (Intel bus mode) The MUNICH32 provides word and long word transfer. The byte enables determine the address offset to the address A31 … A2, the actual word has been stored to. **Address Offset Size** (Motorola mode) Indicates the number of bytes remaining to be transferred for this access. These signals define the active sections of the data bus. In both cases these signals are tristate when unused. See **Chapter 2.2** for details.

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
38, 34, 32, 27, 25, 20, 18, 14, 12, 7, 5, 1, 159, 153, 148, 146, 142, 138, 134, 132, 127, 125, 121, 119, 115, 113, 108, 106, 101, 99, 95	D(31:0)	I/O	**Data Bus** The data bus lines are bidirectional tristate lines which interface with the system's data bus.
86	$\overline{DS}$	O	**Data Strobe** (Motorola mode) This signal indicates that valid data is to be placed on the data bus (read cycle) or has been placed on the data bus by the MUNICH32 (write cycle).
	$\overline{PCHK}$	O	**Parity Check** (Intel parity mode) This signal indicates, whether the parity bits of a read cycle are valid ($\overline{PCHK}$ high) or invalid ($\overline{PCHK}$ low). See **Chapter 2.2.1** for details.
84, 93, 89, 98, 105, 112, 118, 124, 129, 131, 137, 140, 145, 152, 158, 4, 11, 17, 24, 31, 37, 57, 58, 63, 78	V_{DD}	I	**Supply voltage** 5 V ± 5% All pins must have the same level.
85	$\overline{ADS}$	O	**Address Status** (Intel bus mode) This signal indicates that a valid bus cycle definition and address are being driven at the pins.
	$\overline{AS}$	O	**Address Strobe** (Motorola bus mode) A valid address is transmitted on the address bus at the falling edge of $\overline{AS}$. In both cases this signal is active low and tristate when unused.

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
90	W/$\overline{R}$	O	**Write**/**Read** (Intel bus mode) This signal distinguishes write from read operations.
	R/$\overline{W}$	O	**Read**/**Write** (Motorola bus mode) This signal distinguishes between read and write operations. In both cases this signal is tristate when unused.
75	$\overline{READY}$	I	**Ready** (Intel bus mode) This signal indicates that the current bus cycle is complete. When $\overline{READY}$ is asserted during a read cycle the MUNICH32 latches the input data and terminates the cycle. When $\overline{READY}$ is asserted during a write cycle the MUNICH32 terminates the cycle.
	$\overline{DSACK}$	I	**Data Transfer Acknowledge** (Motorola bus mode) This active low input indicates that a data transfer may be performed. During a read cycle data becomes valid at the falling edge of $\overline{DSACK}$. The data is latched internally and the bus cycle is terminated. During a write cycle the falling edge of $\overline{DSACK}$ marks the latching of data and the bus cycle is terminated.

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
76	$\overline{\text{BERR}}$	I	**Bus Error** (Intel and Motorola bus mode) This active low signal informs the MUNICH32 that a bus cycle error has occurred. The MUNICH32 terminates the bus cycle. In case of an erroneous read cycle in the control and configuration section an 'Action Request Fail' interrupt is generated and the action is suspended. In case of an erroneous read cycle in the transmit data section the corresponding frame is aborted and a FO interrupt is generated. In all other cases of read or write cycles terminated with an error condition no further actions are performed by the MUNICH32. Please see **Chapter 2.2**, 'Microprocessor Interface', first paragraph and **Figure 18**. As bus cycles are executed without time limit this signal prevents a hang-up situation of the MUNICH32.
74	B16	I	**Word Operation** Setting this bit to V_{DD} causes the MUNICH32 to perform 32-bit long word accesses to the shared memory, setting it to V_{SS} causes the MUNICH32 to perform 16-bit word accesses on the data lines D(15:0) only. In 16-bit word access mode the data lines D(31:16) should be left open. This bit is **not** dynamic and should be set to V_{DD} in Intel parity mode.

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
82	HOLD	O	**Bus Hold Request** (Intel bus mode) This signal is driven high when the MUNICH32 requests the control of the bus.
	$\overline{BR}$	I/O	**Bus Request** (Motorola bus mode) This signal is driven low when the MUNICH32 requests the control of the bus and is interpreted when another MUNICH32 wants to be the bus master.
79	HLDA	I	**Bus Hold Acknowledge** (Intel bus mode) This active high signal indicates that the processor has released the control of the bus. The MUNICH32 starts the bus cycles.
	$\overline{BG}$	I	**Bus Grant** (Motorola bus mode) This active low signal indicates that the MUNICH32 may assume the bus mastership.
81	$\overline{BGACK}$	I/O	**Bus Grant Acknowledge** (Motorola bus mode) This signal is driven low by the device, when it has become the bus master. It also informs the MUNICH32 whether another device is bus master.
	PM	I	**Parity Mode** (Intel bus mode) This signal has to be strapped to V_{DD} before reset to enable the Intel parity mode or to V_{SS} before reset to enable the Intel non-parity mode. It has to be left strapped during reset and operation.

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
80	HLDAO	O	**Bus Hold Acknowledge Passing ON** (Intel bus mode) If another MUNICH32 has initiated a HOLD REQUEST the HOLD ACKNOWLEDGE is passed on via HLDAO. The MUNICH32 does not give another HOLD REQUEST before the HOLD ACKNOWLEDGE has been deactivated in order to prevent blocking in the case of continuous request by one MUNICH32.
	$\overline{\text{BGO}}$	O	**Bus Grant Acknowledge** (Motorola bus mode) If the MUNICH32 has not requested the bus mastership it passes on the BUS GRANT. The MUNICH32 does not give another BUS REQUEST before the BUS REQUEST and the BUS GRANT ACKNOWLEDGE have been deactivated in order to prevent blocking in the case of continuous request by one MUNICH32.
66	$\overline{\text{AR}}$	I	**Action Request** $\overline{\text{AR}}$ must be pulsed low to cause an action of the MUNICH32. The $\overline{\text{AR}}$ is activated for updating the mode and channel configurations, setting a test loop, or initializing the interrupt queue. The min. time between Reset and first $\overline{\text{AR}}$ is 500 µs.

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
40	INT/$\overline{\text{INT}}$	O	**Interrupt Request** An interrupt is given when a transmission/ reception error is detected, frames are received or transmitted, or a host initiated action is performed. The interrupt pulse signal interacts with a write cycle to the shared memory. The data written into the interrupt queue contains the interrupt specification. The interrupt is active high for Intel bus mode and active low for Motorola bus mode.
44	RCLK	I	**Receive Clock** This clock provides the data clock for RDA T1/DS1 24-channel 1.544 MHz 24-channel 1.536 MHz CEPT 32-channel 2.048 MHz 32-channel 4.096 MHz
45	RSP	I	**Receive Synchronization Pulse** This signal provides the reference for the receive PCM frame synchronization. It marks the first bit in the PCM frame.
46	RDATA	I	**Receive Data** Serial data is received at this PCM input port. The MUNICH32 supports the T1/ DS1 24-channel PCM format, the CEPT 32-channel PCM format as well as a 32-channel PCM format with 4.096-Mbit/s bit rate.
61	SCLK	I	**System Clock** PCM highway system clock highway frequency 32-channel 16.384 MHz 2.048 or 4.096 MHz 24-channel 12.288 MHz 1.536 MHz 24-channel 12.352 MHz 1.544 MHz

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
51 … 47	CI(4:0)	I	**Chip Identification** Up to four MUNICH32 can be connected to the PCM highway. These inputs define the start address of the control section pointer in the shared memory. CI4 is the polarity of A31 … A22 CI3 is the polarity of A21 … A16 CI2 is the polarity of A15 … A4 CI1 is the polarity of A3 CI0 is the polarity of A2 A1, A0 are always '00'
56 … 53	JTEST (3:0)	I/O	**Test Pins** The MUNICH32 supports the JTAG boundary scan test and the JTAG test standards.
65	TEST	I	**Test** If this bit is set to V_{DD} MUNICH32 works in a test mode. For the functional working mode this bit must be set to V_{SS}.
67	TDATA	O	**Transmit Data** Serial data is sent by this PCM output port is push-pull for active bits in the PCM frame and tristate for inactive bits.
68	TSP	I	**Transmit Synchronization Pulse** This signal provides the reference for the transmit frame synchronization. It marks the last bit in the PCM frame.
69	TCLK	I	**Transmit Clock** This clock provides the data clock for TDATA T1/DS1 24-channel 1.544 MHz 24-channel 1.536 MHz CEPT 32-channel 2.048 MHz 32-channel 4.096 MHz

Pin Definitions and Functions (cont'd)

Pin No. P-MQFP-160-1	Symbol	Input (I) Output (O)	Function
60	RESET	I	**Reset**
41, 42, 43, 52, 70, 71, 72	N.C.	-	**No Connect** These pins are reserved and should not be connected

1.4 Logic Symbol

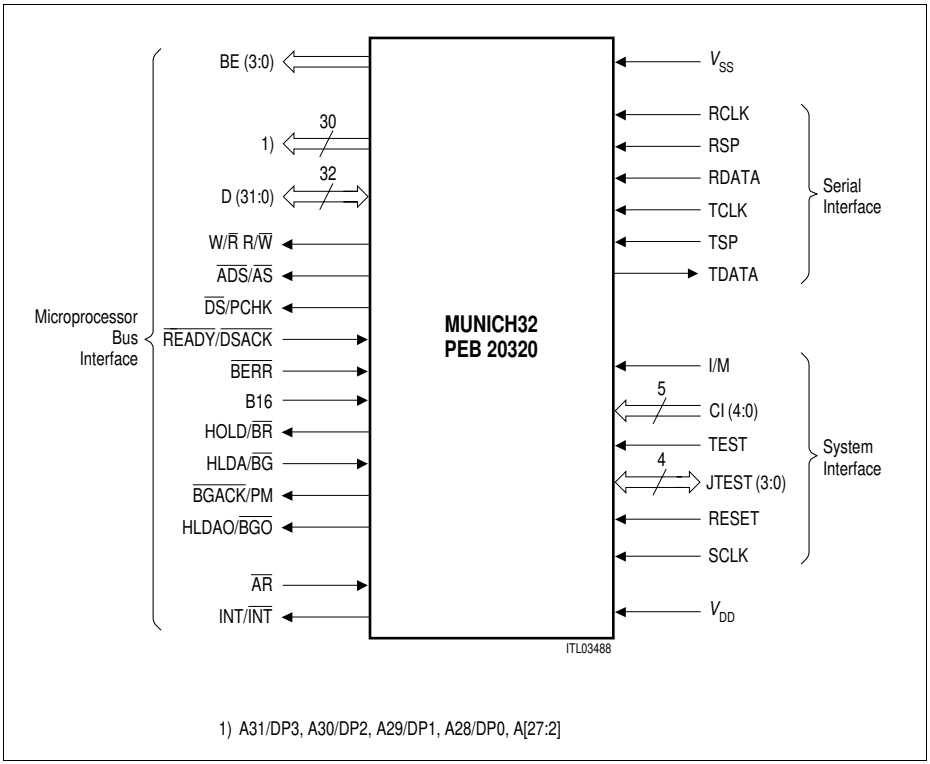

Figure 2
MUNICH32 Logic Symbol

1.5 Functional Block Diagram

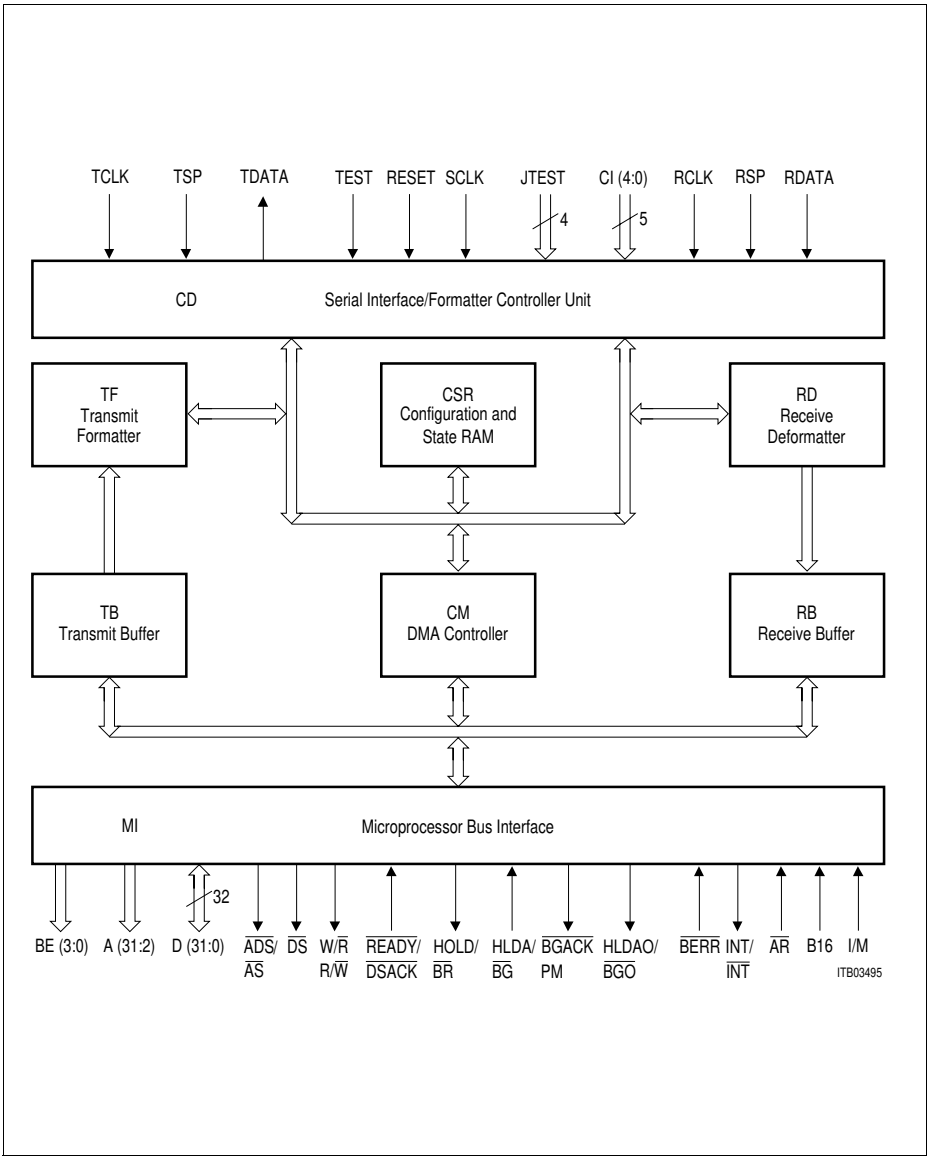

Figure 3
Block Diagram of MUNICH32

The internal functions of MUNICH32 are partitioned into 8 major blocks.

1. Serial Interface, Formatter Control Unit CD
   – Parallel-Serial conversion, PCM timing, switching of the test loops, controlling of the multiplex procedure.
2. Transmit Formatter TF
   – HDLC frame, bit stuffing, flag generation, flag stuffing and adjustment, CRC generation, transparent mode transmission and V.110, X.30 80 bit framing.
3. Transmit Buffer TB
   – Buffer size of 64 long words allocated to the channels, i.e. eight PCM frames can be stored before transmission, individual channel capacity programmable.
4. Receive Deformatter RD
   – HDLC frame, zero-bit deletion, flag detection, CRC checking, transparent mode reception and V.110, X.30 80 bit framing.
5. Receive Buffer RB
   – Buffer size of 64 long words allocated to the channels, i.e. eight PCM frames can be stored, individual long words are freely accessible by each channel.
6. Configuration and State RAM CSR
   – Since the Transmit Formatter, Receive Deformatter are used in a multiplex manner, the state and configuration information of each channel has to be stored.
7. DMA Controller CM
   – Interrupt processing, memory address calculation, chaining list handling, chip configuration.
8. µP interface MI
   – Motorola/Intel microprocessor interface.

1.6 System Integration

The MUNICH32 is designed to handle up to 32 data channels of a PCM highway. It transfers the data between the PCM highway and a memory shared with a host processor via a 32-bit µP interface. At the same time it performs protocol formatting and deformatting as well as rate adaption for each channel independently. The host sets the operating mode, bit rate adaption method and time slot allocation of each channel by writing the information into the shared memory.

Using subchanneling each time slot can be shared between up to four MUNICH32s; so that in one single time slot four different D-channels can be handled by four MUNICH32s.

Figure 4, Figure 5 and **Figure 6** give a general overview of system integration of the MUNICH32.

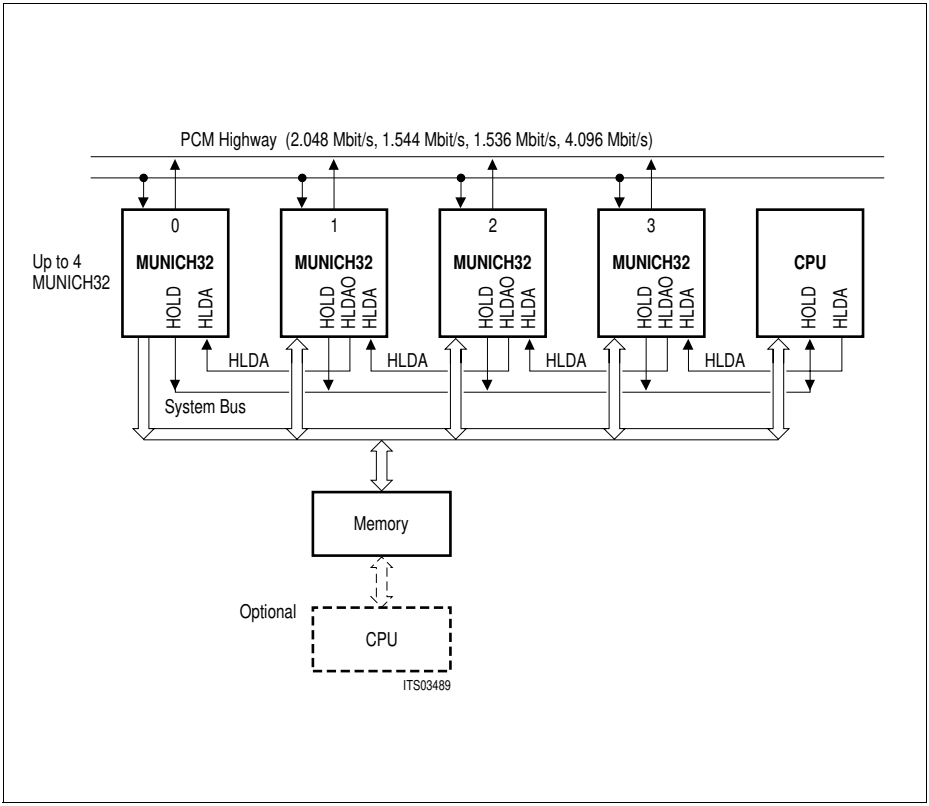

Figure 4
General System Integration (Intel Bus Mode)