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Data Sheet, DS2, Feb. 2001

MUNICH32X

Multichannel Network Interface Controller for HDLC

PEB 20321 Version 2.2
PEF 20321 Version 2.2

Datacom

Infineon technologies

Never stop thinking.

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Page	Subjects (major changes since last revision)
	Package P-TQFP-176-1 removed from User's Manual.
47, 43	Added description of bit shift to chapter **Serial PCM Core**.
204	Programming examples for IOM-2 single rate clock added.
225	Renamed register bit MODE2.TSF to MODE2.TSR.
257	Changed locations of bits IMRX and IMTX in register SSCIM.
263	Register description IOMSTAT reworked.
348	Added timings for LBI Master Demultiplexed Mode
351	Added timing 19, 19A and 24B to**Table 50**. Changed timing 23, 25, 27, 28, 31, 24, 35A, 36A and 36C with respect to previous version of the data sheet.
344ff	Clarified timings for usage of $\overline{\text{LRDY}}$
	plus some minor reworks.

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Preface

This document provide complete reference information about the Multichannel Network Interface Controller for HDLC PEB 20321 (MUNICH32X).

Organization of this Document

This Data Sheet is divided into 16 chapters. It is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications. Furthermore it lists pin locations with associated signals, categorizes signals according to function and describes signals.

- **Chapter 2, Serial PCM Core**
  This chapter provides a functional description of the serial interface.

- **Chapter 3, Basic Functional Principles**
  Provides a description of key concepts including DMA, descriptior operation, buffer management and device configuration.

- **Chapter 4, Detailed Protocol Description**
  Explains supported protocols and available protocol features.

- **Chapter 5, Microprocessor Bus Interface**
  The PCI bus interface and the generic bus interface is covered in this chapter.

- **Chapter 6, Local Bus Interface (LBI)**
  This chapter provides a description of the local bus interface and its DMA modes.

- **Chapter 7, Synchronous Serial Control (SSC) Interface**
  Provides a detailed description of the SSC interface.

- **Chapter 8, IOM®-2 Interface**
  The functions and features of the IOM-2 interface is covered here.

- **Chapter 9, General Purpose Port**
  Gives a description of the general purpose port.

- **Chapter 10, Reset and Initialization**
  This chapter provides information about reset and initialization sequence.

- **Chapter 11, Slave Register Descriptions**
  Provides an overview of the device's registers and a detailed description of each

register.

- **Chapter 12, Host Memory Organization**
  This chapter contains information about the external data structures.

- **Chapter 13, Boundary Scan Unit**

- **Chapter 14, Electrical Characteristics**
  Gives a detailed description of all electrical DC and AC characteristics and provides timing diagrams and values for all interfaces.

- **Chapter 15, MUNICH32X Bus Utilization**
  Contains information about bus utilization on the PCI bus for different parameters.

- **Chapter 16, Package Outline**

Your Comments

We welcome your comments on this document. We are continuously trying improving our documentation. Please send your remarks and suggestions by e-mail to sc.docu_comments@infineon.com

Please provide in the subject of your e-mail:
device name (MUNICH32X), device number (PEB 20321 or PEF 20321), device version (Version 2.2), and in the body of your e-mail:
document type (Data Sheet), issue date (2001-02-14) and document revision number (DS2).

Table of Contents **Page**

List of Figures **Page**

List of Tables

1 Overview

The MUNICH32X is an enhanced version of the Multichannel Network Interface Controller for HDLC, MUNICH32 (PEB 20320, refer to the User's Manual 01.2000).

Key enhancements include:

- a 33 MHz/32-bit PCI bus Master/Slave interface with integrated DMA controllers for higher performance, lower development effort and risk,
- symmetrical Rx and Tx buffer descriptor formats for faster switching,
- an improved Tx idle channel polling process for significantly reduced bus occupancy,
- an integrated Local Bus Interface (LBI) for connection to other peripherals that do not have a PCI bus interface with DMA capability,
- an SSC interface and
- an IOM®-2 interface.

The MUNICH32X provides capability for up to 32 full-duplex serial PCM channels. It performs layer 2 HDLC formatting/deformatting or V.110 or X.30 protocols up to a network data rate of 38.4 Kbit/s (V.110) or 64 Kbit/s (HDLC), as well as transparent transmission for the DMI mode 0, 1, and 2. Processed data are passed on to an external memory shared with one or more host processors.

The MUNICH32X is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT, as well as with HDLC, SDLC, LAPB and DMI protocols. It provides any rate adaption for time slot transmission data rate from 64 Kbit/s down to 8 Kbit/s and the concatenation of any time slots to data channels, supporting the ISDN H0, H11, H12 superchannels.

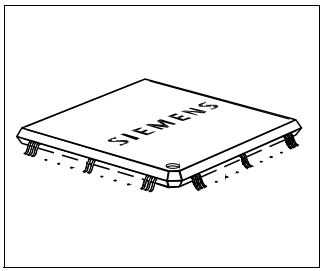
The MUNICH32X may be used in a wide range of telecommunication and networking applications, e.g.

- in switches to provide the connection to a PBX, to a host computer, or as a central D-channel controller for 32 D-channels,
- for connection of up to 4 MUNICH32Xs to one PCM highway to achieve a D-channel controller with 128 channels,
- in routers and bridges for LAN-WAN internetworking via channelized T1/E1 or multiple S/T interfaces,
- for wide area trunk cards in routers and switches (Frame Relay, ISDN PRI, Internet Protocols, etc.), and
- for centralized D- or B-channel packet processing in routers, switches (Frame Relay, Q.931 Signaling, X.25, etc.)

Note: In the course of the Data Sheet, the expression 'DWORD' always refers to 32-bit words in correspondence to the PCI specification.

Version 2.2

1.1 Features



32-channel HDLC controller with PCI interface:

- **Serial PCM core**
  - Up to 32 independent full-duplex channels
  - Serial PCM traffic at 2.048, 4.096, 1.544, 1.536, 3.088, 6.176 or 8.192-Mbit/s
- **Dynamic Programmable Channel Allocation**
  - Compatible with T1/DS1 24-channel and CEPT 32-channel PCM byte format
  - Concatenation of any, not necessarily consecutive, time slots to superchannels
  - independently for receive and transmit direction
  - Support of H0, H11, H12 ISDN-channels
  - Subchanneling on each time slot possible
- **Bit Processor Functions** (adjustable for each channel)
  - HDLC Protocol
    - Automatic flag detection
    - Shared opening and closing flag
    - Detection of interframe-time-fill change, generation of interframe-time-fill ‘1’s or flags
    - Zero bit insertion
    - Flag stuffing and flag adjustment for rate adaption
    - CRC generation and checking (16 or 32 bits)
    - Transparent CRC option per channel and/or per message
    - Error detection (abort, long frame, CRC error, 2 categories of short frames, non-octet frame content)
    - ABORT/IDLE flag generation
  - V.110/X.30 Protocol

Type	Package
PEB 20321	P-MQFP-160-1
PEF 20321	P-MQFP-160-1

  - Automatic synchronization in receive direction, automatic generation of the synchronization pattern in transmit direction
  - E/S/X bits freely programmable in transmit direction, may be changed during transmission; changes monitored and reported in receive direction
  - Generation/detection of loss of synchronism
  - Bit framing with network data rates from 600 bit/s up to 38.4 Kbit/s
- Transparent Mode A
  - Slot synchronous transparent transmission/reception without frame structure
  - Flag generation, flag stuffing, flag extraction, flag generation in the abort case with programmable flag
  - Synchronized data transfer for fractional T1/PRI channels
- Transparent Mode B
  - Transparent transmission/reception in frames delimited by 00_H flags
  - Shared opening and closing flag
  - Flag stuffing, flag detection, flag generation in the abort case
  - Error detection (non octet frame content, short frame, long frame)
- Transparent Mode R
  - Transparent transmission/reception with GSM 08.60 frame structure
  - Automatic 0000_H flag generation/detection
  - Support of 40, $39^1/_2$, $40^1/_2$ octet frames
  - Error detection (non octet frame contents, short frame, long frame)
- Protocol Independent
  - Channel inversion (data, flags, IDLE code)
  - Format conventions as in CCITT Q.921 § 2.8
  - Data over- and underflow detected

- **Microprocessor Interface**
  - 32-bit PCI bus interface option, 33 MHz
  - 32-bit De-multiplexed bus interface option, 33 MHz
  - 68 channel DMA controller (64 for 32 serial channels, 4 for 2 LBI channels) with buffer chaining capability
  - Master 4-DWORD burst read and write capability
  - Slave single-DWORD read and write capability
  - Interrupt-circular buffers with variable sizes
  - Maskable interrupts for each channel
- **IOM®-2 Interface with on-chip C/I and monitor handlers**
- **Synchronous Serial Control (SSC) Interface**
- **8-/16-bit Local Bus Interface (LBI)**

- **General**
  - Connection of up to four MUNICH32X supporting a 128-channel basic access D-channel controller
  - On-chip Rx and Tx data buffers 256 bytes each
  - HDLC protocol or transparent mode, support of ECMA 102, CCITT I4.63 RA2, V.110, X.30, DMI mode 0, 1, 2 (bit rate adaption), GSM 08.60 TRAU frames
  - Loopback mode, complete loop as well as single channel loop
  - JTAG boundary scan test
  - 0.5 µm low-power CMOS technology
  - 3.3 V and 5 V voltage supply
  - TTL-compatible inputs/outputs
  - 160-pin P-MQFP package

1.2 New or Changed from MUNICH32, PEB 20320

- Symmetrical Rx and Tx Buffer Descriptor formats for faster switching
- Improved Tx idle channel polling process, which significantly reduces bus occupancy of idle Tx channels
- Additional PCM modes supported: 3.088 Mbit/s, 6.176 Mbit/s, 8.192 Mbit/s
- 32-bit PCI bus Master/Slave interface (33 MHz) with integrated DMA controllers for higher performance, and lower development effort and risk
- Enhanced Interrupt Structure providing:
  separate serial PCM Rx and Tx Interrupt Queues in host memory,
  separate DMA related LBI Rx and Tx Interrupt Queues in host memory,
  dedicated LBI pass-through, SSC, General Purpose bus and IOM®-2 Peripheral Interrupt Queue in host memory
- Slave read capability of serial PCM core, LBI, SSC and IOM®-2 read/write registers
- Time Slot Shift capability
- Bit Shift Capability
  programmable from -4 clock edges to +3 clock edges relative to synchronization pulse,
  programmable to sample Tx data at either clock falling or rising edge,
  programmable to sample Rx data at either clock falling or rising edge,
- Software initiated Action Request via a bit field in the Command register
- Tx End-of-Packet transmitted-on-wire interrupt capability per channel
- Tx packet size increased to 16 Kbytes
- Rx packet size 8 kbyte limit interrupt disable
- Rx Enable bit field of the MODE1 register
- Rx Interrupt Disable bit field of the MODE1 register
- Tx data tristate control line ($\overline{\text{TXDEN}}$)
- Synchronized data transfer in TMA mode for complete transparency when using fractional T1/PRI channels
- Integrated Local Bus Interface (LBI), which allows connection to peripherals that do not provide a PCI bus interface
- IOM®-2 interface with single and double data rate clock
- Collision control on S/T interface by QUAT-S (PEB 2084) via data ready control line (DRDY)
- Synchronous Serial Control (SSC) interface
- 16-bit General Purpose Bus (8 bits are shared with LBI, the other eight bits are shared with SSC; the respective bits can not be used when LBI and/or SSC are enabled)
- Internal Descriptor and Table Dump capability for software development purposes
- Little/Big Endian data formats selectable via a bit field in Configuration register

1.3 Pin Configuration

(top view)

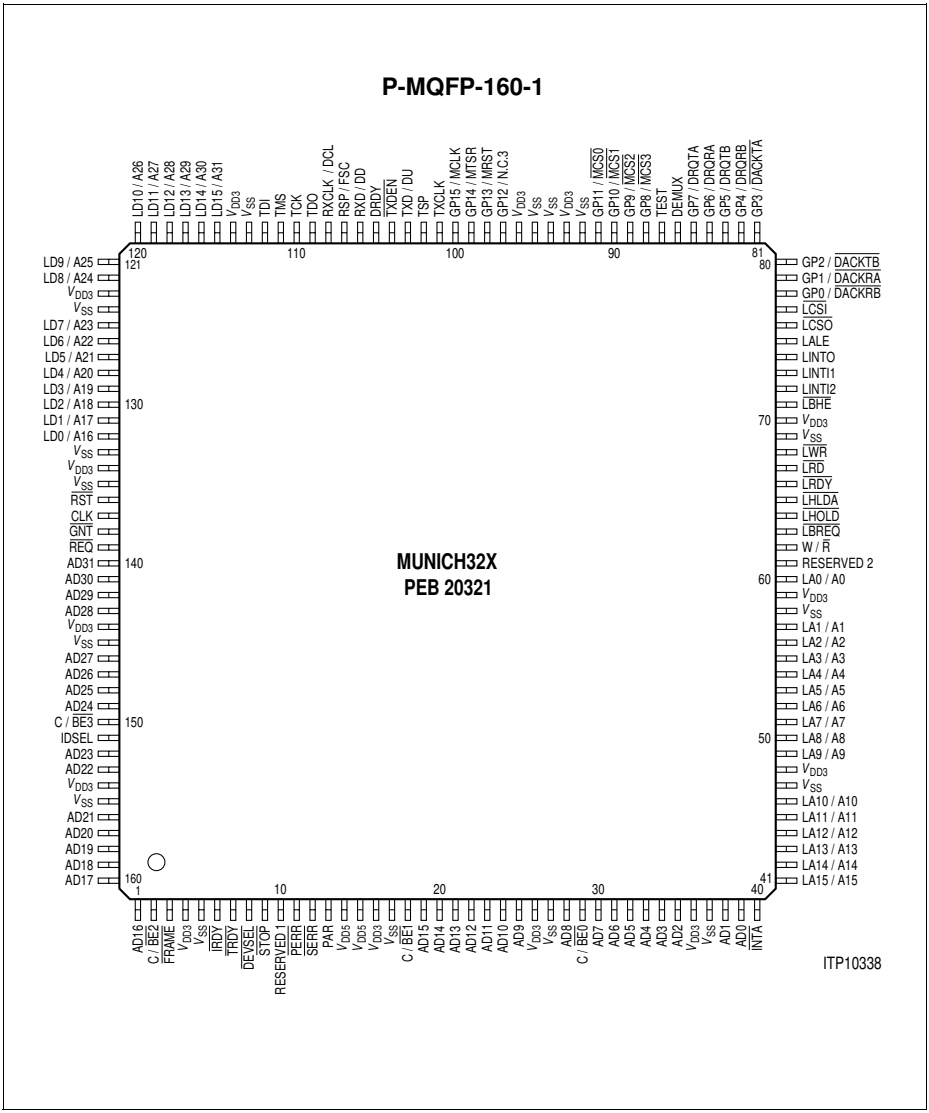


Figure 1 Pin Configuration

Signal Type Definition:

The following signal type definitions are mainly taken from the PCI Specification Revision 2.1:

in	*Input* is a standard input-only signal.
out	*Totem Pole Output* is a standard active driver.
t/s, I/O	*Tri-State* or *I/O* is a bi-directional, tri-state input/output pin.
s/t/s	*Sustained Tri-State* is an active low tri-state signal owned and driven by one and only one agent at a time. (For further information refer to the PCI Specification Revision 2.1)
o/d	*Open Drain* allows multiple devices to share as a wire-OR. A pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.

1.3.1 PCI Bus Interface Pins

Table 1 PCI Bus Interface Pins

Pin No.	Symbol	I/O	Function
140, 141, 142, 143, 146, 147, 148, 149, 152, 153, 156, 157, 158, 159, 160, 1, 19, 20, 21, 22, 23, 24, 25, 28, 30, 31, 32, 33, 34, 35, 38, 39	AD(31:0)	t/s	**Address/Data Bus** A bus transaction consists of an address phase followed by one or more data phases. When MUNICH32X is Master, AD(31:0) are outputs in the address phase of a transaction. During the data phases, AD(31:0) remain outputs for write transactions, and become inputs for read transactions. When MUNICH32X is Slave, AD(31:0) are inputs in the address phase of a transaction. During the data phases, AD(31:0) remain inputs for write transactions, and become outputs for read transactions. AD(31:0) are updated and sampled on the rising edge of CLK.
150, 2, 18, 29	C/$\overline{\text{BE}}$(3:0)	t/s	**Command/Byte Enable** During the address phase of a transaction, C/$\overline{\text{BE}}$(3:0) define the bus command. During the data phase, C/$\overline{\text{BE}}$(3:0) are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/$\overline{\text{BE0}}$ applies to byte 0 (lsb) and C/$\overline{\text{BE3}}$ applies to byte 3 (msb). When MUNICH32X is Master, C/$\overline{\text{BE}}$(3:0) are outputs. When MUNICH32X is Slave, C/$\overline{\text{BE}}$(3:0) are inputs. C/$\overline{\text{BE}}$(3:0) are updated and sampled on the rising edge of CLK.