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DSCC4

DMA Supported Serial Communication Controller with 4 Channels

PEB 20534 Version 2.1
PEF 20534 Version 2.1

Datacom

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429-438	427-435	corrected timing values #81-#86, #132, #149

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Preface

The *DMA Supported Serial Communication Controller with 4 Channels* (DSCC4) is a Multi Protocol Controller for a wide range of data communication and telecommunication applications. This document provides complete reference information on hardware and software related issues as well as on general operation.

Organization of this Document

This Data Sheet is divided into 15 chapters. It is organized as follows:

- Chapter 1, Overview
  Gives a general description of the product, lists the key features, and presents some typical applications.

- Chapter 2, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- Chapters 3,4,5,6,7 Functional Description
  These chapters provide detailed descriptions of all DSCC4 internal function blocks.

- Chapter 8, Detailed Protocol Descriptions
  Gives a detailed description of all protocols supported by the serial communication controllers SCCs.

- Chapter 9, Reset and Initialization Procedure
  Gives examples for DSCC4 initialization procedure and operation.

- Chapter 10, Detailed Register Description
  Gives a detailed description of all DSCC4 on chip registers.

- Chapter 11, Host Memory Organization
  Provides an overview of all DSCC4 data structures located in the shared memory

- Chapter 12, JTAG Boundary Scan
  Gives a detailed description of the boundary scan unit.

- Chapter 13, Electrical Characteristics
  Gives a detailed description of all electrical DC and AC characteristics and provides timing diagrams and values for all interfaces.

- Chapter 14, Package Outline

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1 Overview

The DSCC4 is a DMA Supported Serial Communication Controller with four independent serial channels[1]. The serial channels are derived from updated protocol logic of the ESCC device family providing a large set of protocol support and variety in serial interface configuration. This allows easy integration to different environments and applications.

A 33-MHz/32-bit PCI bus Master/Slave interface with integrated high performance DMA controllers provides data transfer from or to host memory with low bus utilization and easy software handshaking.

An additional de-multiplexed bus interface mode is provided for integration in non-PCI bus environments with little glue-logic depending on the bus type.

The DMA Controller operates on linked lists which are optimized for data communication applications. Different control mechanisms allow easy software development well adapted to the needs of special applications.

Large onchip FIFOs in combination with enhanced threshold control mechanisms allow decoupling of traffic requirements on host bus and serial interfaces with little exception probabilities such as data underuns or overflows.
In a PCI bus application an integrated Local Bus Interface (LBI) provides bridging functionality to non PCI peripherals such as framers or line interface units (LIUs).

A Synchronous Serial Control (SSC) interface as well as a General Purpose Port (GPP) allows covering application specific requirements without additional controllers.

Each of the four Serial Communication Controllers (SCC) contains an independent Baud Rate Generator, DPLL, programmable protocol processing (HDLC, BISYNC, ASYNC and PPP). Data rates of up to 2 Mbit/s (DPLL assisted modes, ASYNC, BISYNC), 10 Mbit/s (HDLC, PPP) and 52 Mbit/s (H-52 version) are supported. The channels can also handle a large set of layer-2 protocol functions reducing bus and host CPU load. Four channel specific timers are provided to support protocol functions.

The DSCC4 devices can be used in LAN-WAN inter-networking applications such as Routers, Switches and Trunk cards and support the common V.35, ISDN BRI (S/T) or Asynchronous Dial-up interfaces. Its new features provide powerful hardware and software interfaces to develop high performance systems.

[1] The serial channels are also called ’ports’ or ’cores’ depending on the context.

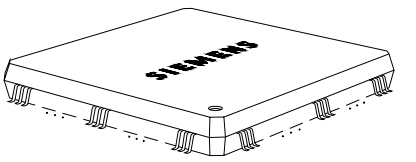
DMA Supported Serial Communication Controller with 4 Channels
DSCC4

PEB 20534
PEF 20534

Version 2.1

CMOS

1.1 Features



P-FQFP-208-7

Serial Communication Controllers (SCCs)

- Four independent channels
- Full duplex data rates on each channel of up to 10 Mbit/s sync - 2 Mbit/s with DPLL, 2 Mbit/s async
- Full duplex data rate of up to 52 Mbit/s on any two channels in high speed mode (HDLC: Address Mode 0 and extended transparent protocol mode); up to 45 Mbit/s on any two channels in high speed mode (HDLC: PPP modes). The aggregate bandwith for all channels is limited to 108 Mbit/s per direction.
- 17 DWORDs deep receive FIFO per SCC (+ 128 DWORDs central receive FIFO).
- 8 DWORDs deep transmit FIFO per SCC (+ 128 DWORDs central transmit FIFO).

Serial Interface

- On-chip clock generation or external clock sources
- On-chip DPLLs for clock recovery
- Baud rate generator
- Clock gating signals
- Clock gapping capability
- Programmable time-slot capability for connection to TDM interfaces (e.g. T1, E1)
- NRZ, NRZI, FM and Manchester data encoding
- Optional data flow control using modem control lines ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, CD)
- Support of bus configuration by collision detection and resolution

Type	Package
PEB 20534 H-10	P-FQFP-208-7
PEF 20534 H-10	P-FQFP-208-7
PEB 20534 H-52	P-FQFP-208-7

- HDLC/SDLC Protocol Modes
  - Automatic flag detection and transmission
  - Shared opening and closing flag
  - Generation of interframe-time fill ’1’s or flags
  - Detection of receive line status
  - Zero bit insertion and deletion
  - CRC generation and checking (CRC-CCITT or CRC-32)
  - Transparent CRC option per channel and/or per frame
  - Programmable Preamble (8 bit) with selectable repetition rate
  - Error detection (abort, long frame, CRC error, short frames)
- Bit Synchronous PPP Mode
  - Bit oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Zero bit insertion/deletion
  - 15 consecutive ’1’ bits abort sequence
- Octet Synchronous PPP Mode
  - Octet oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Programmable character map of 32 hard-wired characters (00_H-$1F_H$)
  - Four programmable characters for additional mapping
  - Insertion/deletion of control-escape character ($7D_H$) for mapped characters
- Asynchronous PPP Mode
  - Character oriented transmission of HDLC frame (flag, data, CRC, flag)
  - Start/stop bit framing of single character
  - Programmable character map of 32 hard-wired characters (00_H-$1F_H$)
  - Four programmable characters for additional mapping
  - Insertion/deletion of control-escape character ($7D_H$) for mapped characters
- Asynchronous (ASYNC) Protocol Mode
  - Selectable character length (5 to 8 bits)
  - Even, odd, forced or no parity generation/checking
  - 1 or 2 stop bits
  - Break detection/generation
  - In-band flow control by XON/XOFF
  - Immediate character insertion
  - Termination character detection for end of block identification
  - Time out detection
  - Error detection (parity error, framing error)
- BISYNC Protocol Mode
  - Programmable 6/8 bit SYN pattern (MONOSYNC)
  - Programmable 12/16 bit SYN pattern (BISYNC)
  - Selectable character length (5 to 8 bits)
  - Even, odd, forced or no parity generation/checking
  - Generation of interframe-time fill ’1’s or SYN characters
  - CRC generation (CRC-16 or CRC-CCITT)
  - Transparent CRC option per channel and/or per frame

  - Programmable Preamble (8 bit) with selectable repetition rate
  - Termination character detection for end of block identification
  - Error detection (parity error, framing error)
- Extended Transparent Mode
  - Fully bit transparent (no framing, no bit manipulation)
  - Octet-aligned transmission and reception
- Protocol and Mode Independent
  - Data bit inversion
  - Data overflow and underrun detection
  - Timer

Protocol Support

- Address Recognition Modes
  - No address recognition (Address Mode 0)
  - 8-bit (high byte) address recognition (Address Mode 1)
  - 8-bit (low byte) or 16-bit (high and low byte) address recognition (Non Auto Mode)
- HDLC Auto Mode
  - 8-bit or 16-bit address generation/recognition
  - Support of LAPB/LAPD
  - Automatic handling of S- and I-frames
  - Automatic processing of control byte(s)
  - Modulo-8 or modulo-128 operation
  - Programmable time-out and retry conditions
  - SDLC Normal Response Mode (NRM) operation for slave

Microprocessor Interface

- 33 MHz/32-bit PCI bus interface option.
- 33 MHz/32-bit De-multiplexed bus interface option.
- 8-channel DMA controller with buffer chaining capability.
  - Master 15-word burst read and write capability (PCI Mode).
  - Master 4-word burst read and write capability (DEMUX Mode).
  - Slave single-word read and write capability.
- Circular interrupt queues with variable size.
- Maskable interrupts for each channel

Other Interfaces

- 8-/16-bit optional Local Bus Interface (LBI) for driving non-PCI peripherals in a PCI environment.
- Synchronous Serial Control interface (SSC) for controlling peripherals.
- 16-bit General Purpose Port (GPP).

General

- On chip Rx and Tx data buffer; the buffer size is 128 32-bit words each.
- Programmable buffer size in transmit direction per channel; buffer allocation in receive direction on request.
- Programmable watermark for receive channels to control transfer of receive data to host memory.
- Two programmable watermarks for each transmit channel. One controlling data loading from host memory and one controlling transfer of transmit data to the corresponding Serial Communication Controller (SCC).
- Internal test loop capability.
- JTAG boundary scan test according to IEEE 1149.1
- Advanced low-power CMOS technology
- TTL-compatible inputs/outputs
  – 3.3 V & 5 V power supply
  – 3.3 V interfaces (TTL levels; 5 V tolerant in 5 V environment)
- P-FQFP-208-7 package
- The 10 MHz version only is available in extended temperature range -40 .. +85 °C (PEF 20534 H-10)

1.2 Differences between the DSCC4 and the ESCC Family

This chapter is useful for all being familiar with the Infineon Technologies' ESCC family.

1.2.1 Enhancements to the ESCC Serial Core

The DSCC4 SCC cores contain the core logic of the ESCC2 V3.2A as the heart of the device. Some enhancements are incorporated in the SCCs. These are:

- Asynchronous PPP protocol support as in Internet RFC-1662
- Octet and Bit Synchronous PPP protocol support as in Internet RFC-1662
- 16-Kbyte packet length byte counter
- Enhanced address filtering (16-bit maskable)
- Enhanced time slot assigner
- Support of high data rates (45 Mbit/s for DS3 or 52 Mbit/s for OC1). Protocol support limited to HDLC Sub-modes without address recognition.

1.2.2 Simplifications to the ESCC Serial Core

The following features of the ESCC core have been removed:

- SDLC Loop mode
- Extended transparent mode 0
  (this mode provided octet buffered data reception without usage of FIFOs; the DSCC4 supports octet buffered reception via appropriate threshold configurations for the SCC receive FIFOs)

1.3 Logic Symbol

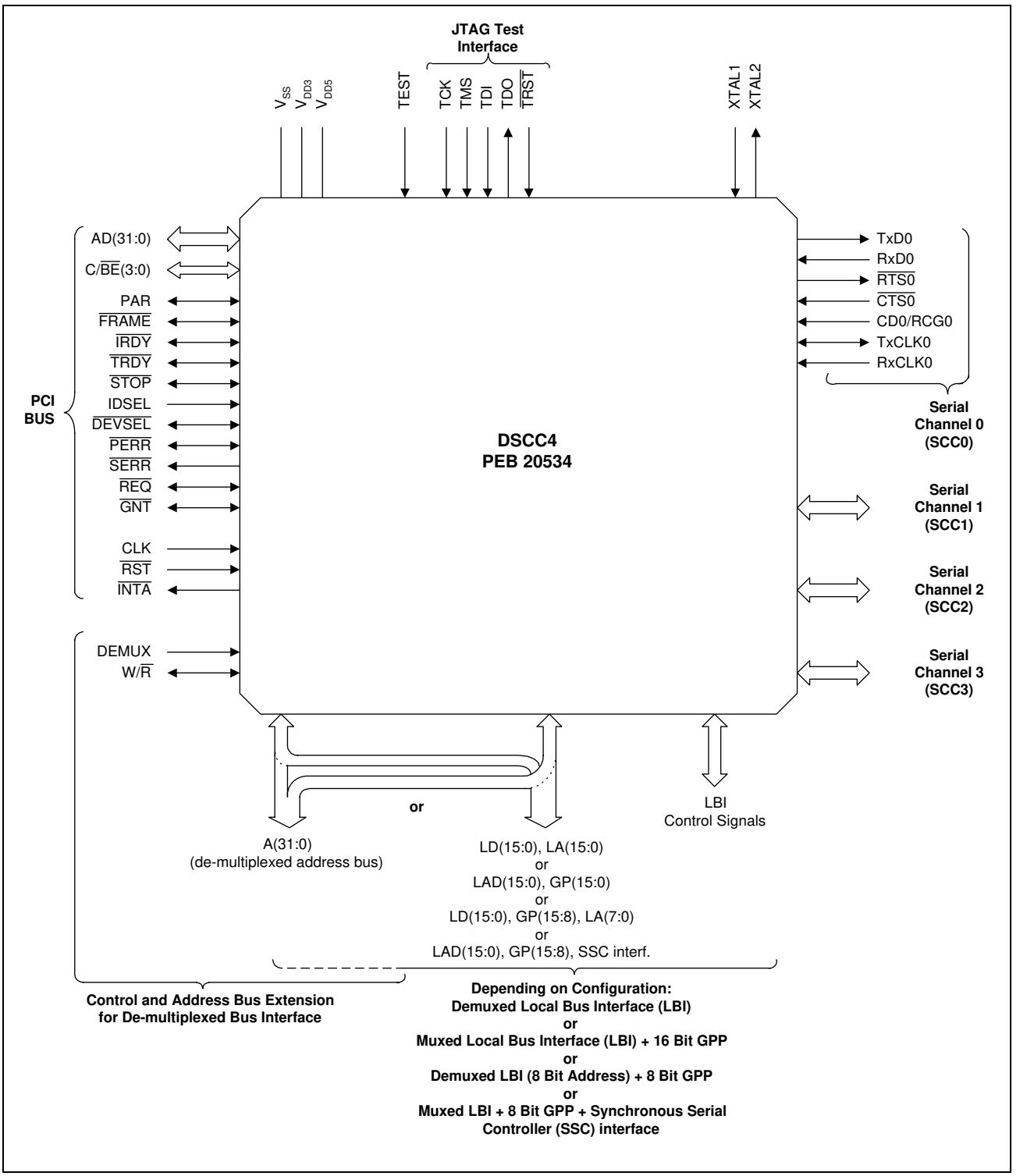


Figure 1 Logic Symbol

1.4 Typical Applications

The DSCC4 is designed to handle up to 4 serial data ports in various configurations, depending on the application. It transfers the data between the serial ports and a shared memory via its 32 bit/33 MHz PCI Bus Interface which can optionally be configured as a generic 32 bit de-multiplexed bus interface in the case that no PCI bus is applicable.

Figure 2 provides a general overview upon system integration of the DSCC4 in a PCI bus environment:

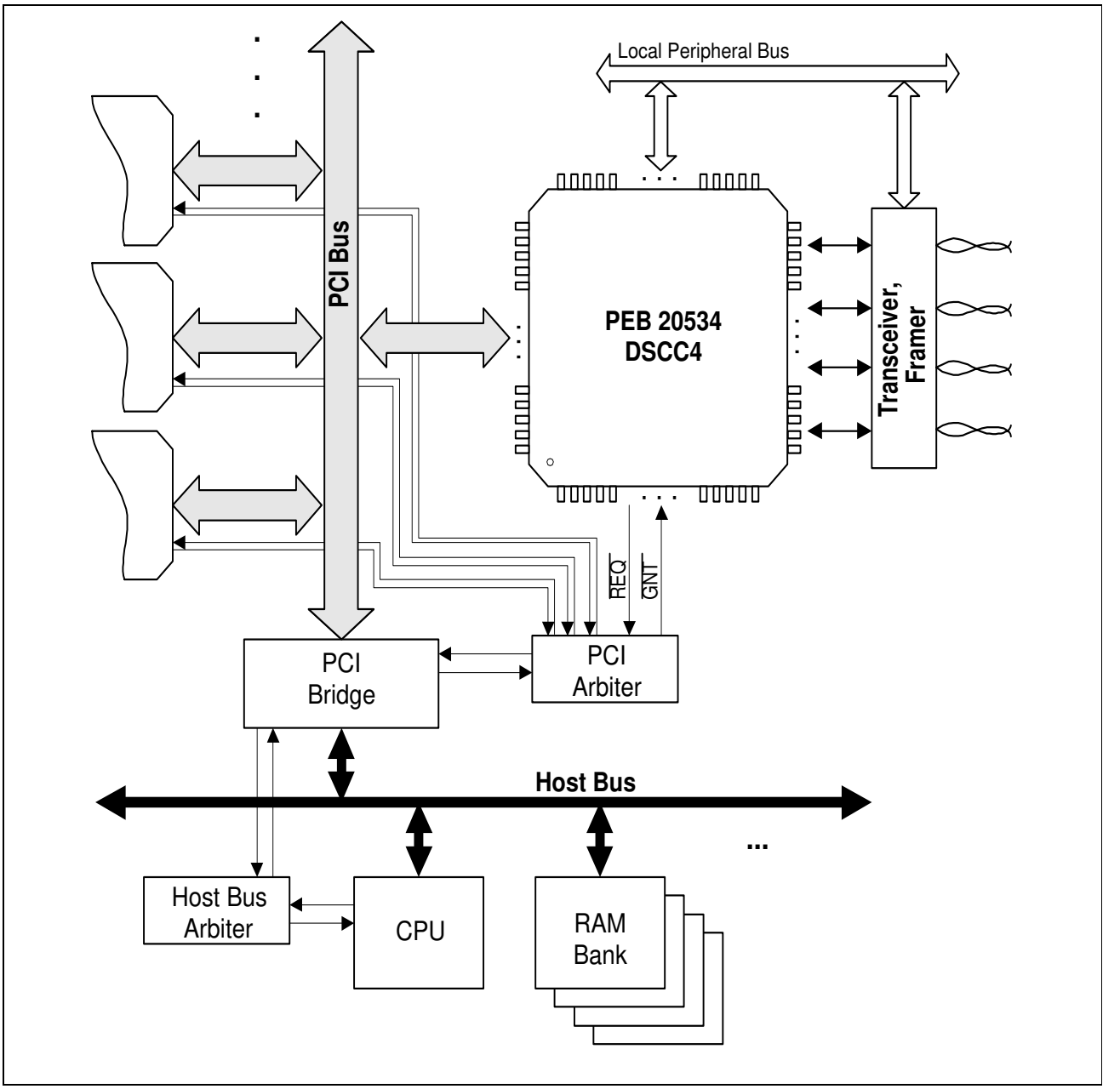


Figure 2 General System Integration (PCI Bus Interface)

Connection of DSCC4 to PCI Bus according to PCI Specification Rev. 2.1 is free of any glue-logic.

Figure 3 provides an overview upon system integration in a non PCI bus environment by the example of a Motorola 68360 CPU bus:

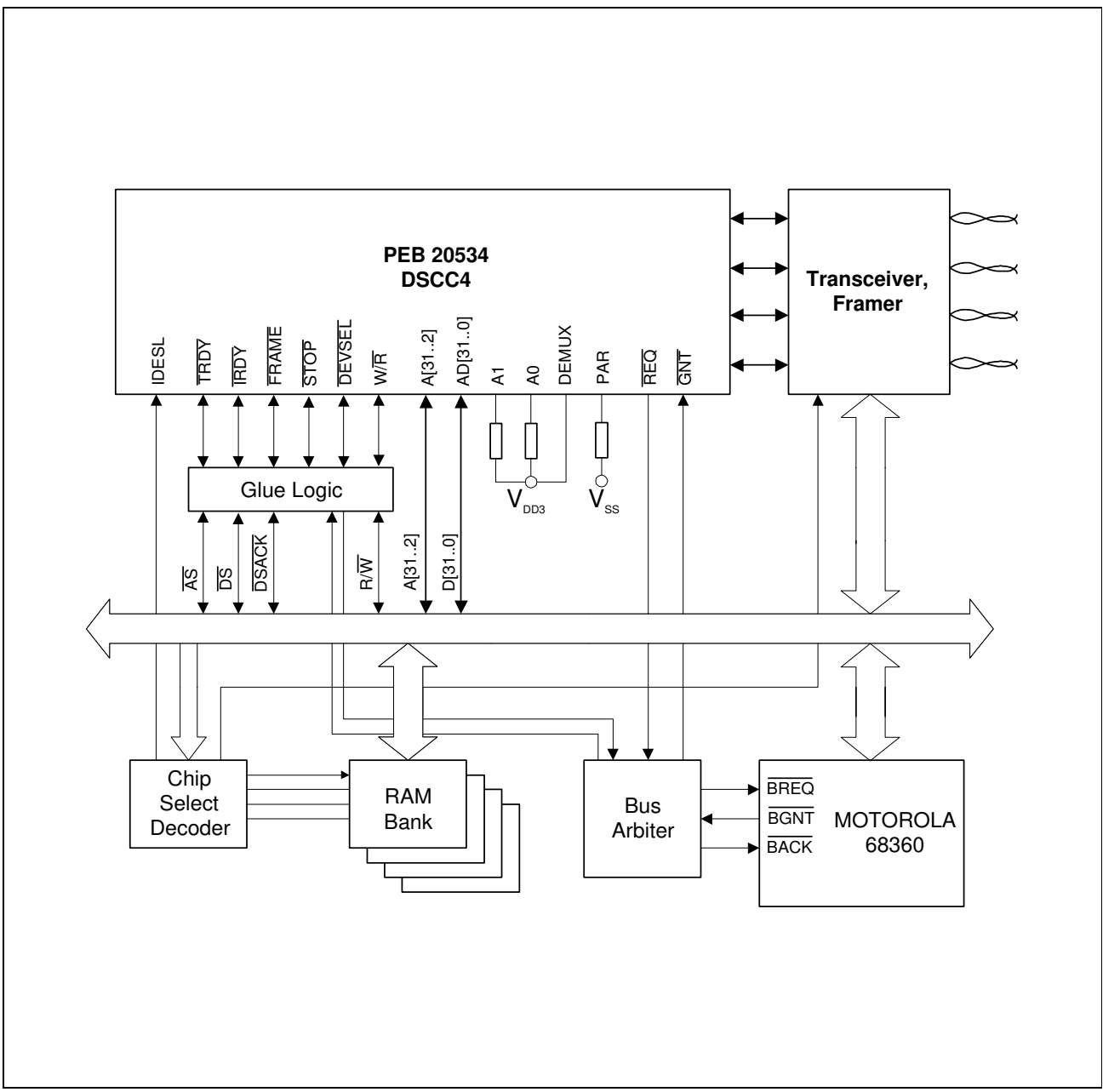


Figure 3 General System Integration (De-multiplexed Interface)

The glue-logic depends on the host bus which the DSCC4 should be connected to. The example in **Figure 3** shows the glue-logic for connection to an Motorola 68360 like de-multiplexed 32 bit bus.