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SIEMENS

ICs for Communications

ISDN D-Channel Exchange Controller (IDEC®)
PEB 2075

User´s Manual 05.92

PEB 2075 Revision History: 05.92	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **“Processing Guidelines”** and **“Quality Assurance”** for ICs, see our **“Product Overview”**.

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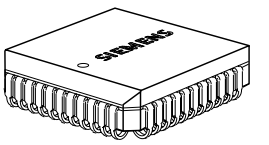
SIEMENS

ISDN D-Channel Exchange Controller (IDEC®) PEB 2075

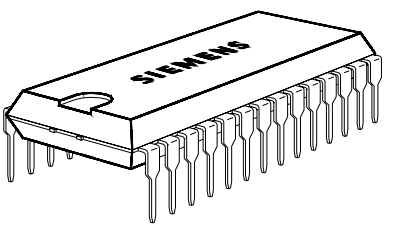
CMOS IC

1 Features

- Four independent HDLC channels
- 64-byte FIFO storage per channel and direction
- Handling of basic HDLC functions
  flag detection/generation
  zero deletion/insertion
  CRC checking/generation
  check for abort
- Address recognition
- C/I channel handler
- Single connection and quad connection modes
- IOM® interface or PCM interface
- Programmable time slots and channel data rates (up to 4 Mbit/s)
- Different methods of contention resolution
- Standard µP- interface, multiplexed or non-multiplexed address and data buses
- Vectored interrupt
- Advanced CMOS technology
- Power consumption less than 50 mW during operation.



P-LCC-44



P-DIP-28

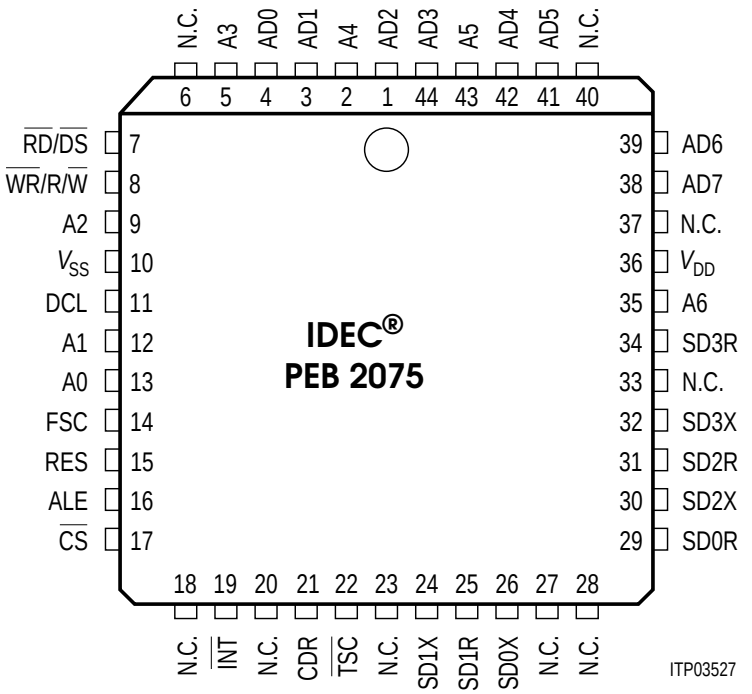
Type	Version	Ordering Code	Package
PEB 2075-N	V.1.3	Q67100-H6189	P-LCC-44 (SMD)
PEB 2075-P	V.1.3	Q67100-H6188	P-DIP-28

The ISDN Digital Exchange Controller PEB 2075 (IDEC) is a serial HDLC data communication circuit with four independent channels. Its telecommunication specific features make it especially suited for use in variable data rate PCM systems. In addition, the device contains sophisticated switching functions and it implements automatic contention resolution between packet data from different sources.

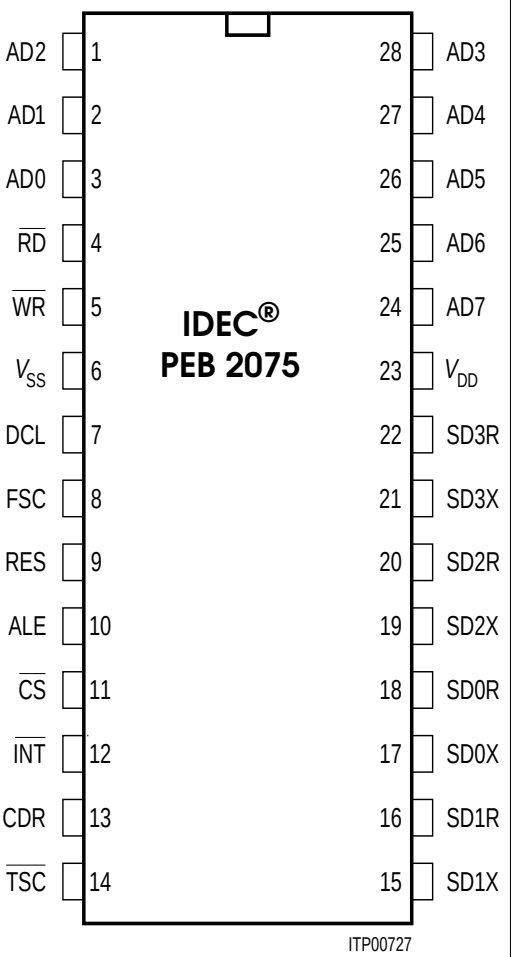
Its applications include: communication multiplexers, peripheral ISDN line cards, packet handlers and X.25 packet switching devices. The IDEC is a fundamental building block for networks with either centralized, de-centralized or mixed signaling/packet data handling architectures.

1.1 Pin Configuration

(top view)



P-LCC-44



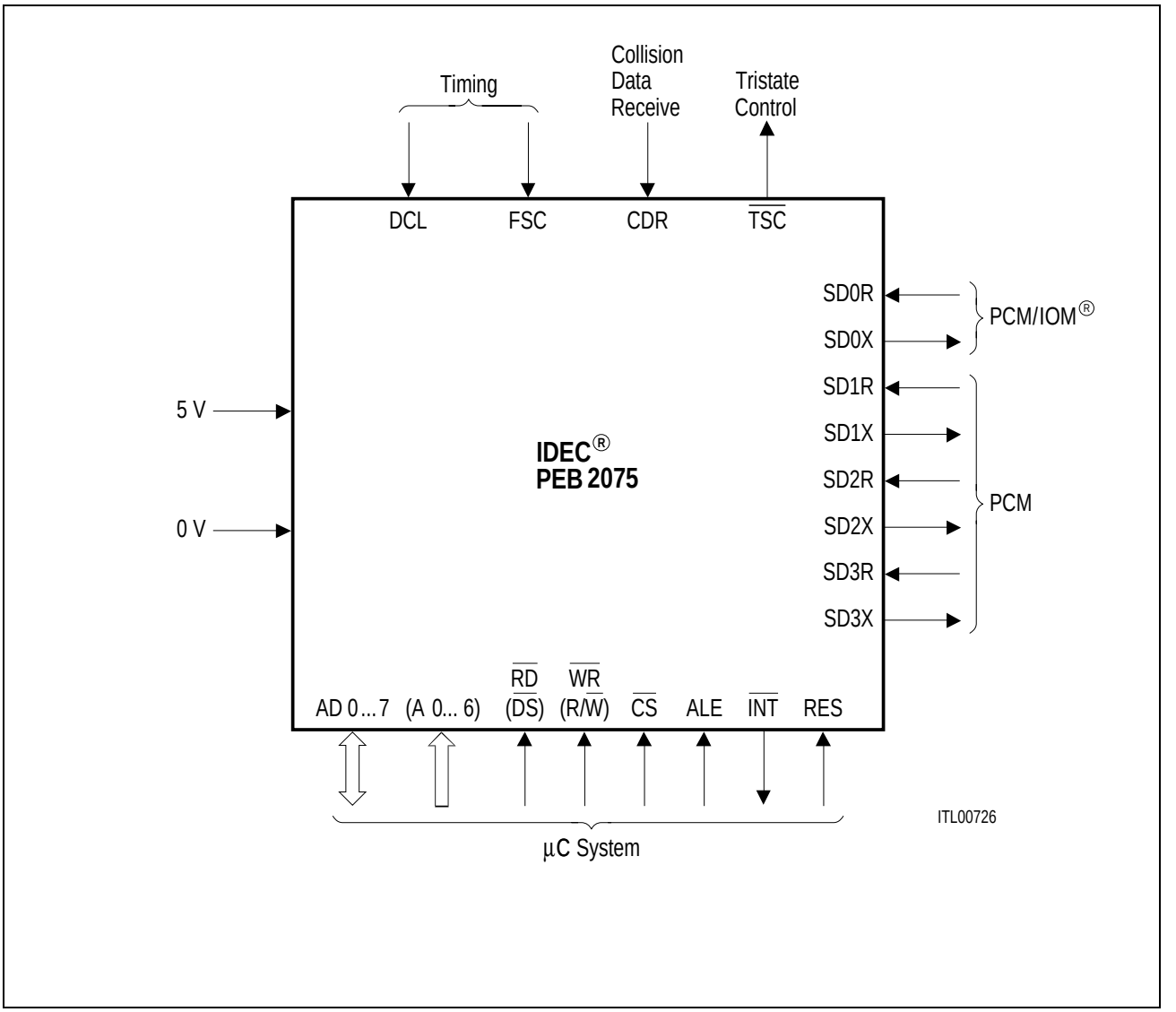
P-DIP-28

1.2 Pin Definitions and Functions

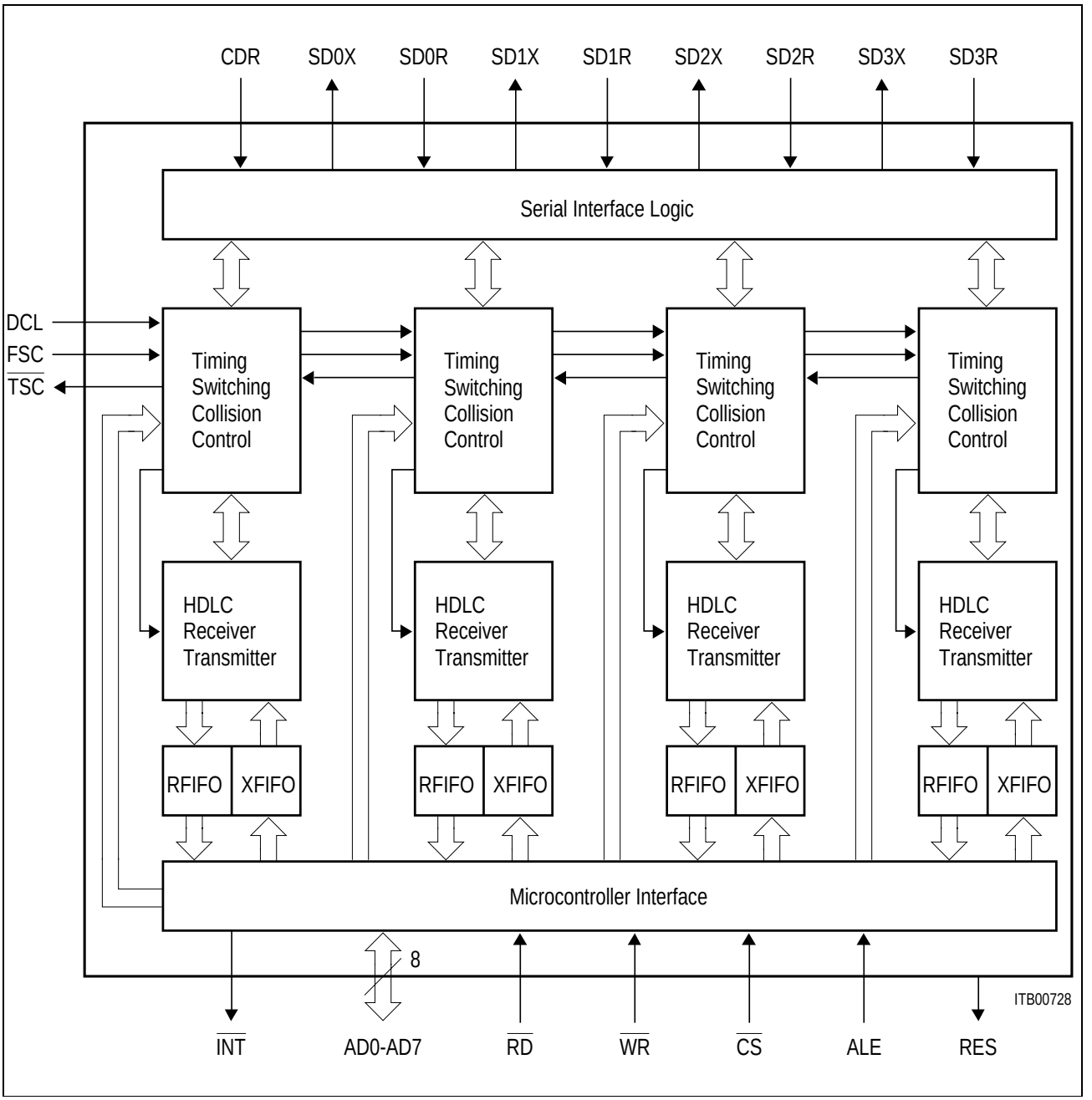
Pin No. P-LCC-44	Pin No. P-DIP-28	Symbol	Input (I) Output (O) Open Drain (OD)	Function
4 3 1 44 42 41 39 38	3 2 1 28 27 26 25 24	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I / O	**Address Data Bus.** If the multiplexed address/data µP interface bus mode is selected these lines transfer data and commands between the µP and the IDEC. If a demultiplexed mode is used, these lines interface with the system data bus.
13 12 9 5 2 43 35	- - - - - - -	A0 A1 A2 A3 A4 A5 A6	I	**Address Bus.** These inputs interface to the system´s address bus to select an internal register for a read or write access. Only provided in the P-LCC package and only active if a demultiplexed µP interface is selected.
17	11	$\overline{CS}$	I	**Chip Select.** A low on this line selects the IDEC for a read/write operation.
8 8	5 -	$\overline{WR}$ R/$\overline{W}$	I I	**Write.** This signal indicates a write operation, active low (Siemens/Intel bus mode). **Read/Write.** At "high", identifies a valid µP access as a read operation. At "low", identifies a µP access as a write operation (Motorola bus mode). Only provided in the P-LCC package.
7 7	4 -	$\overline{RD}$ $\overline{DS}$	I I	**Read.** This signal indicates a read operation, active low (Siemens/Intel bus mode). **Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode). Only provided in the P-LCC package.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC-44	Pin No. P-DIP-28	Symbol	Input (I) Output (O) Open Drain (OD)	Function
16	10	ALE	I	**Address Latch Enable.** In the Siemens/ Intel type multiplexed µP interface mode a "high" on this line indicates an address of an internal register on the external address/data bus. In the Siemens/Intel type demultiplexed µP interface mode this line should be connected to V_{SS}, in the demultiplexed Motorola type µP interface mode it should be connected to V_{DD}.
19	12	$\overline{INT}$	OD	**Interrupt Request.** This signal is activated when the IDEC requests an interrupt.
15	9	RES	I	**Reset.** A "high" on this interrupt brings the IDEC into the reset state.
29 25 31 34	18 16 20 22	SD0R SD1R SD2R SD3R	I	Serial data receive.
26 24 30 32	17 15 19 21	SD0X SD1X SD2X SD3X	O	Serial data transmit. Serial data transmit. Serial data transmit. Serial data transmit. Serial data transmit. Collision output. Serial data transmit. -
11	7	DCL	I	**Data Clock;** supplies a clock signal either equal to or twice the data rate.
14	8	FSC	I	Frame synchronization or data strobe signal.
22	14	$\overline{TSC}$	O	**Time-Slot Control.** Supplies a control signal for an external driver.
21	13	CDR	I	Collision data receive.
10	6	V_{SS}	I	Ground.
36	23	V_{DD}	I	Positive power supply.



Logic Symbol



Block Diagram

1.3 System Integration

Communication Multiplexers

The four independent serial HDLC communication channels implemented in the IDEC make the circuit suitable for use in communication multiplexers.

The collision detection/resolution capability of the circuit allows statistical multiplexing of packets in one or several physical data communication channels, for example in DMI (mode 3) applications.

Centralized Signaling / Data Packet Handlers

The IDEC can be used in central packet handlers of ISDN networks to process signaling or packet data of four ISDN subscribers. In this application, it may be used with or without the Extended PCM Interface Controller (EPIC®) PEB 2055.

The IDEC can be connected to the IOM interface of the EPIC, which is itself connected to the PCM system highway. The EPIC implements concentration and time slot assignment functions. As an alternative, the IDEC may be directly connected to PCM highways (**figure 1**).

The size (from 1 to 8 bits) and the position of the time slot associated with each HDLC controller is software programmable. In addition to the receive and transmit data highways, the IDEC accepts a third input connection for collision detection purposes. The mode of collision detection is programmable. A "collision highway" (or time slot) can be used for remote collision control, as a "clear to send" lead, or for local contention resolution among several IDECs.

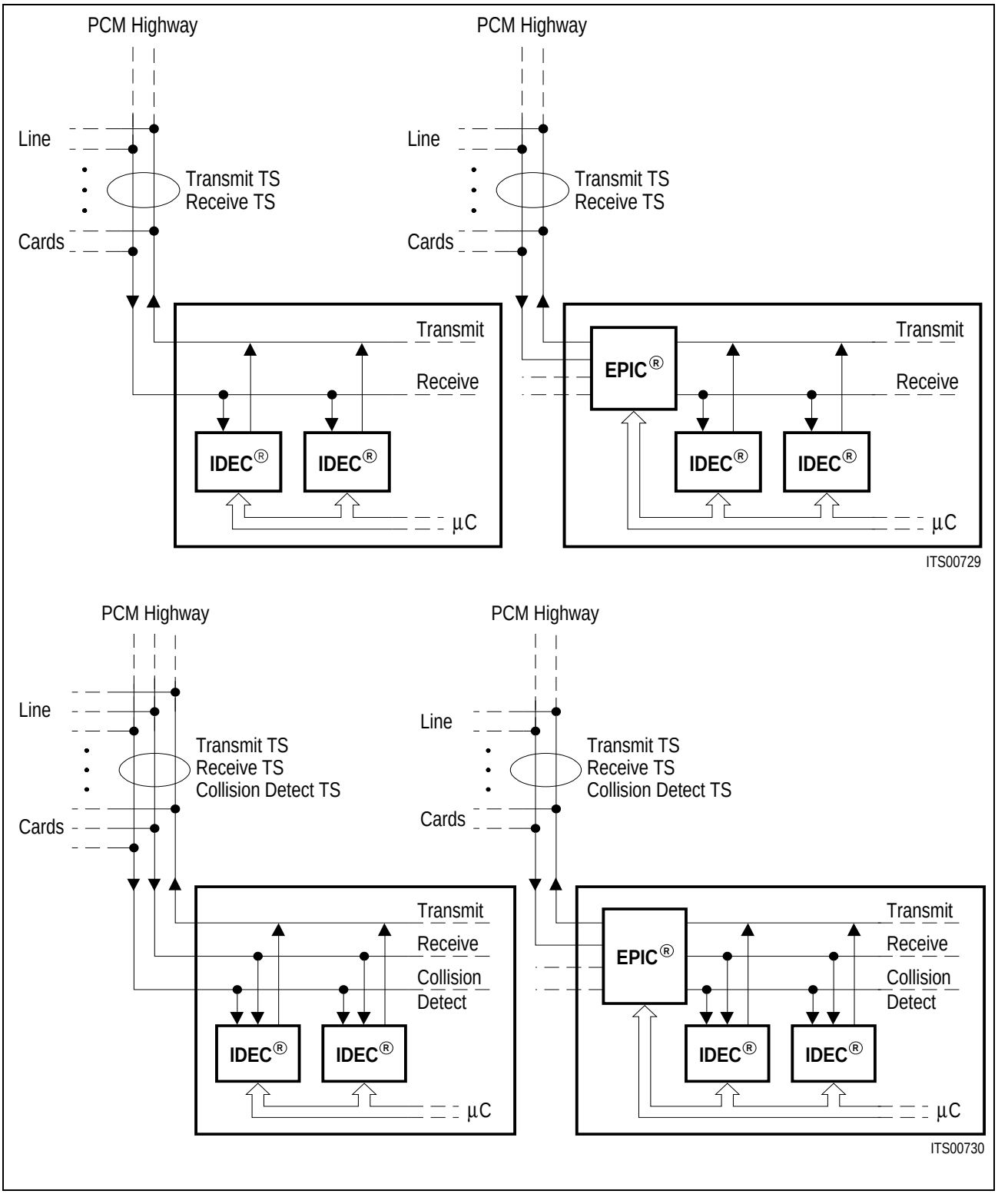


Figure 1
Use of IDEC® in Central Signaling / Data Packet Handlers

Line Cards in De-Centralized or Mixed Signaling / Data Packet Handling Architectures

The IDEC can be used on peripheral line cards to process D-channel packets for ISDN subscribers. The PCM Controller PEB 2055 has the layer-1 controlling capacity and a B-channel switching capacity for a total of 32 subscribers. The B and D channels and the control information for eight subscribers are carried by one IOM interface. Thus a line card dimensioned for 32-ISDN subscribers may employ up to eight IDECs, two for each IOM connection (**figure 2**). A High Level Serial Communication Controller (HSCX) SAB 82525 with two HDLC channels, or another IDEC may be used to transmit and receive signaling via the system highway in a common channel. Again, such a common channel may be shared among several line cards, due to the statistical multiplexing capability of these controllers.

In completely de-centralized D-channel processing architectures, the processing capacity of a line card is usually dimensioned so as to avoid blocking situations even under maximum conceivable D-channel traffic conditions. It may sometimes be more advantageous to perform p-packet handling in a centralized manner while keeping s-packet handling on the line cards. A statistical increase in p-packet traffic has then no effect on the line card, and can be easily dealt with by one of the modular architectures for a central packet handler shown in the previous section. A more effective sharing of the total p-packet handling capacity is the result, especially in a situation where p-packet traffic patterns vary widely from one subscriber group to another.

The use of an IDEC in the mixed D-channel processing architecture is illustrated in **figure 3**.

The additional "transparent data" connections supported by the IDEC enable a merging of p and s packets into one D channel. Possible collision situations are dealt with by the IDEC which uses either the additional collision detect line (**figure 3**) or a time slot on the system highway (**figure 3**) from the line card to the central packet handler.

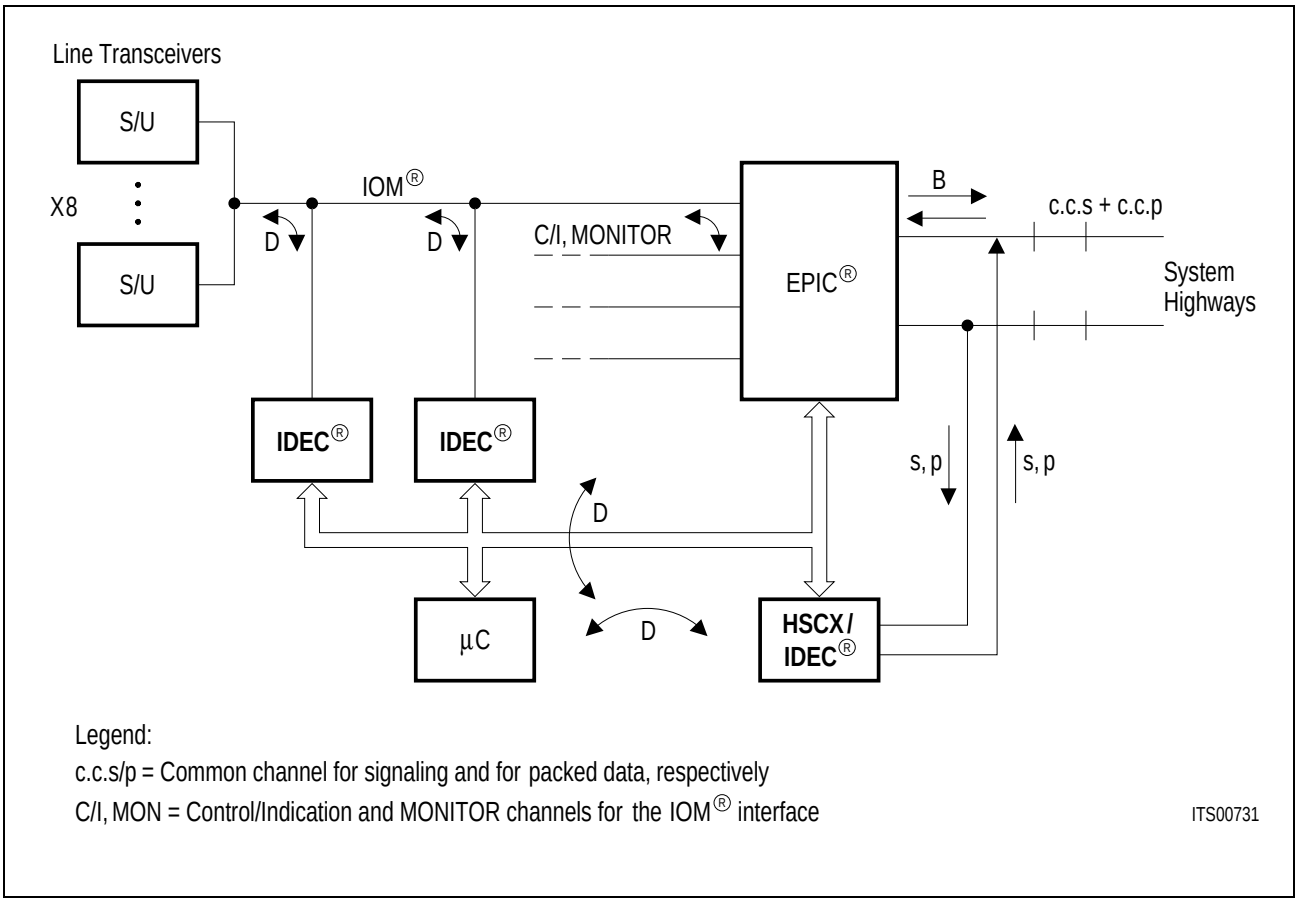


Figure 2
Line Card in a De-Centralized D-Channel Handling Architecture

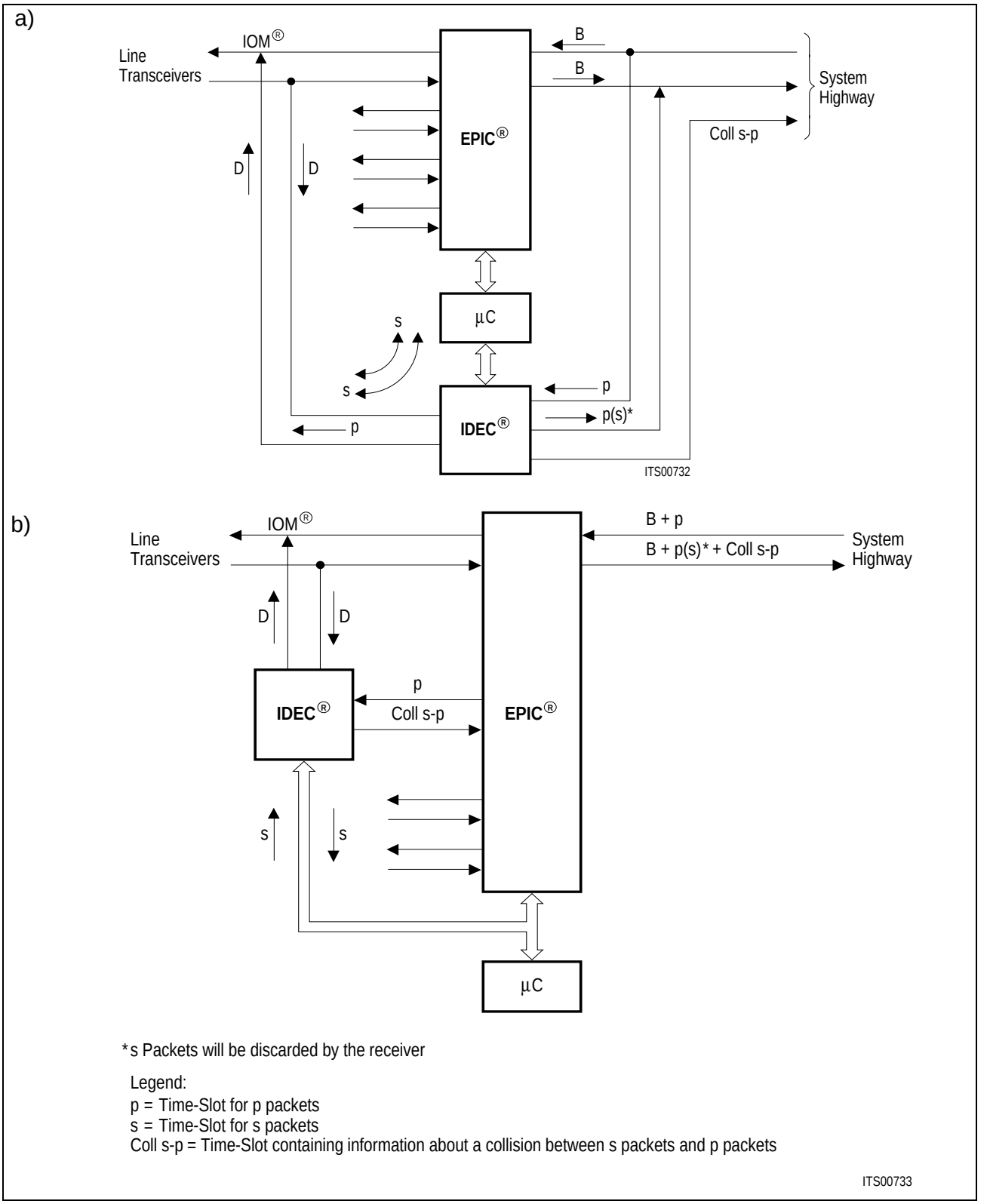


Figure 3
IDEC® on a Line Card in a Mixed D-Channel Processing Architecture

2 Functional Description

2.1 General Functions and Device Architecture

The IDEC is an HDLC controller which handles four HDLC communication channels, each channel fully independent and programmable by its own register set. The circuit performs the following functions:

- Extraction (reception) and insertion (transmission) of the HDLC data packets in a time division multiplex bit stream.
- Implementation of the basic HDLC functions of the layer-2 protocol, including address recognition.
- Interfacing of the data packets to the microprocessor bus. For the temporary storage of data packets internal FIFOs are used.
- Switching of data between serial interfaces.
- Implementation of different types of collision resolution.
- Test functions.

2.2 Operating Modes

Each HDLC controller of the IDEC is assigned to one time channel determined either by time slot assignment or by an external strobe signal.

Two basic configurations are distinguished (**figure 4**):

- In the quad connection configuration the four HDLC controllers (A - D) are connected to individual time multiplexed communication lines;
- In the single connection configuration the four HDLC channels are all connected to one time multiplexed communication line.

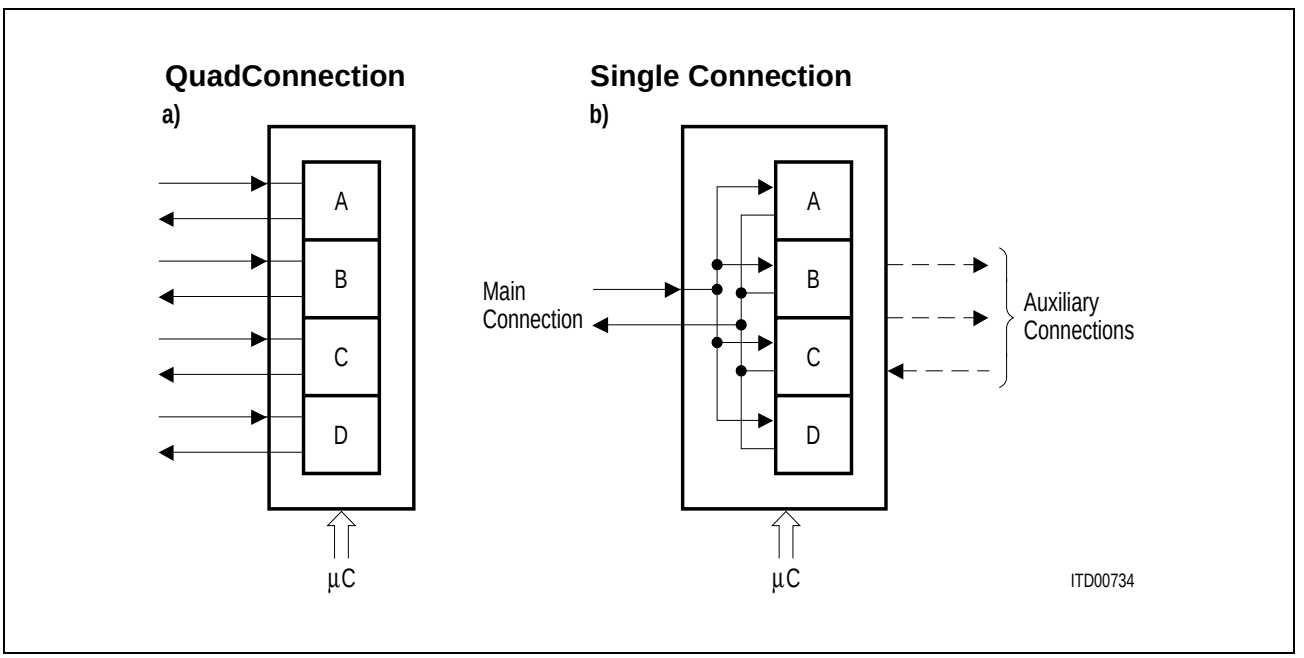


Figure 4

In the quad connection configuration two modes are distinguished as follows:

- Each connection is a time slotted highway, the lengths and positions of the time slots are programmable (quad connection time slot mode);
- Each connection is a communication line, the time channels are marked by an external strobe signal (quad connection common control mode).

Two modes are distinguished in turn for the single connection configuration as follows:

- The connection is a standard IOM interface with predefined channel positions (single connection IOM mode);
- The connection is a time slotted highway (single connection time slot mode).

For simplicity, a time slotted highway will usually be referred to as a "PCM highway", or PCM for short.

Table 1
Four Basic Operation Modes of the IDEC

MDS1	MDS0	Mode Description
0	0	Single connection time slot mode
0	1	Quad connection common control mode
1	0	Single connection IOM mode
1	1	Quad connection time slot mode

To program the single connection IOM mode (CCR:MDS1, MDS0 = 10)
with the slave mode (MODE3-0:CMS1, CMS0 = 01) or
with the multi master mode (MODE3-0:CMS1, CMS0 = 10) or
with the uncond. trans. mode (MODE3-0:CMS1, CMS0 = 00)

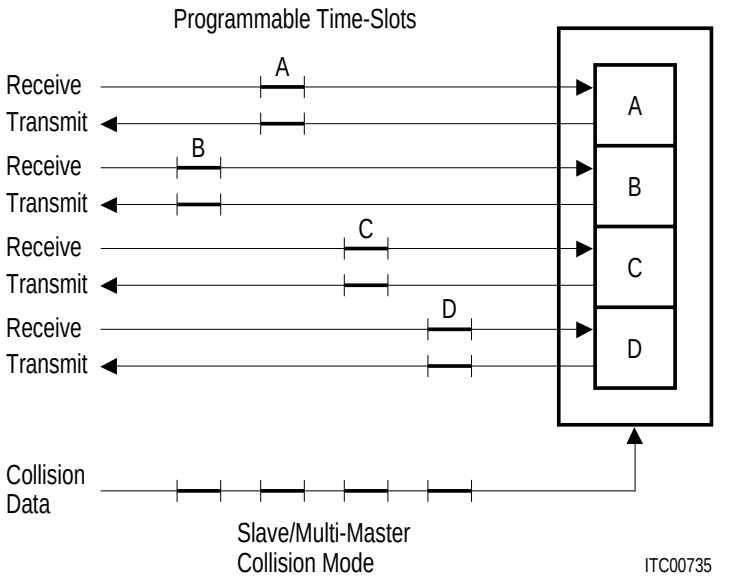
this additional programming has to be made:

MODE0:CCS1, CCS0 = 00 bin
MODE1:CCS1, CCS0 = 00 bin
MODE2:CCS1, CCS0 = 00 bin
MODE3:CCS1, CCS0 = 00 bin

TSR0 = 0C hex
TSR1 = 1C hex
TSR2 = 2C hex
TSR3 = 3C hex

The four modes of operation are illustrated in **figure 5**. Via channel-by-channel programming, one of a number of collision detection modes may be selected in each of the basic modes of operation. For future reference, they are also depicted in **figure 5**.

a) Quad Connection TS Mode



b) Quad Connection Common Control Mode

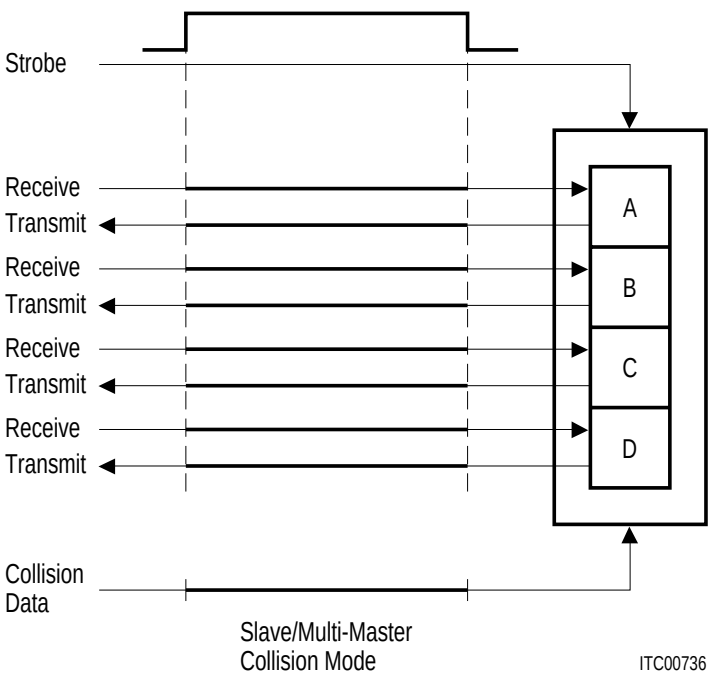
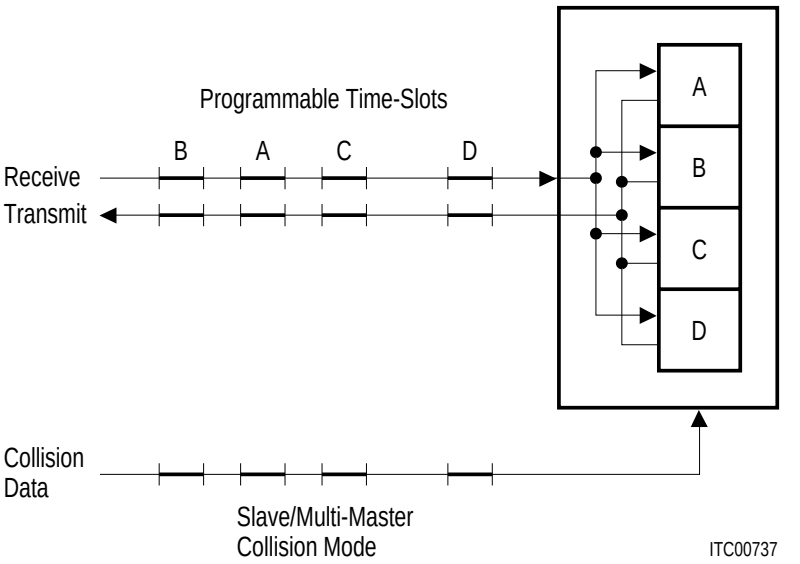


Figure 5a, 5b
Operating Modes of the IDEC

c) Single Connection TS Mode



d) Single Connection IOM® Mode

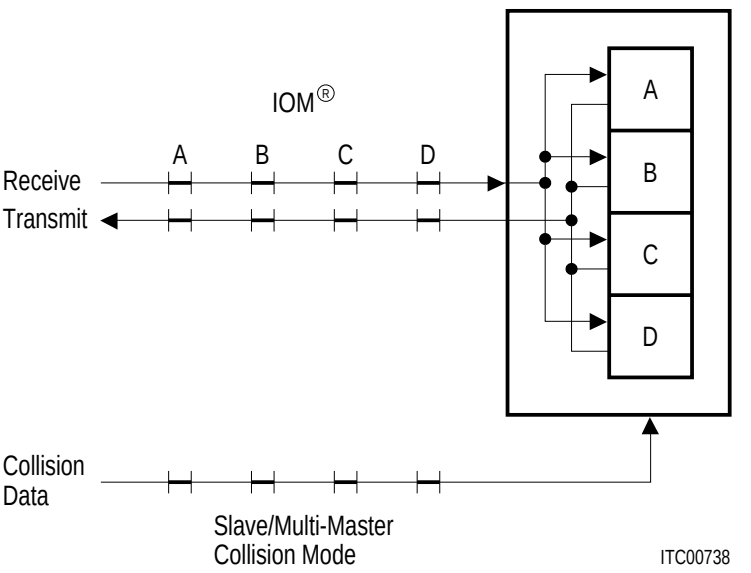


Figure 5c, 5c
Operating Modes of the IDEC

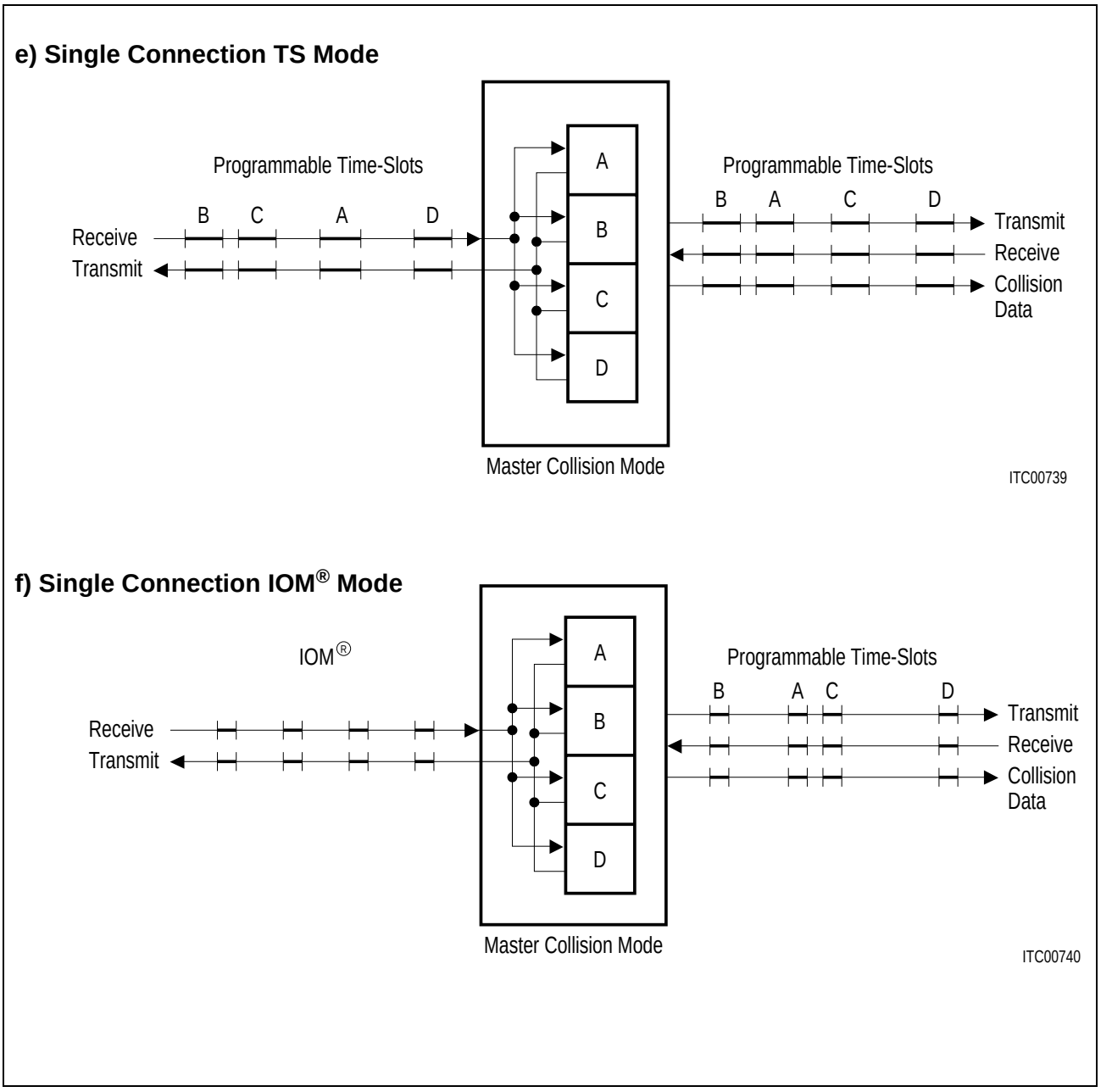


Figure 5e, 5f
Operating Modes of the IDEC

2.3 Interfaces

Microcontroller Interface

The IDEC is programmable over an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (19) lines and is directly compatible with processors of the multiplexed and demultiplexed address/ data bus types (Siemens/Intel or Motorola processor families). The microprocessor interface signals are summarized in **table 2**.

Table 2
Microcontroller Interface Signals of the IDEC

Symbol	Input (I) Output (O) Open Drain (OD)	Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Address Data Bus.** If the multiplexed address/data µP interface bus mode is selected these lines transfer data and commands between the µP and the IDEC. If a demultiplexed mode is used, these lines interface with the system data bus.
A0 ... A6	I	**Address Bus.** These inputs interface to the system´s address bus to select an internal register for a read or write access. Only provided in the P-LCC package and only active if a demultiplexed µP interface is selected.
$\overline{CS}$	I	**Chip Select.** A low on this line selects the IDEC for a read/write operation.
$\overline{WR}$ R/$\overline{W}$	I	**Write.** This signal indicates a write operation, active low (Siemens/Intel bus mode). **Read/Write.** At "high", identifies a valid µP access as a read operation. At "low", identifies a µP access as a write operation (Motorola bus mode). Only provided in the P-LCC package.
$\overline{RD}$ $\overline{DS}$	I	**Read.** This signal indicates a read operation, active low (Siemens/Intel bus mode). **Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode). Only provided in the P-LCC package.

Table 2 (cont'd)

Microcontroller Interface Signals of the IDEC

Symbol	Input (I) Output (O) Open Drain (OD)	Function
ALE	I	**Address Latch Enable**. In the Siemens/Intel type multiplexed µP interface mode a "high" on this line indicates an address of an internal register on the external address/data bus. In the Siemens/Intel type demultiplexed µP interface mode this line should be connected to V_{SS}. In the demultiplexed Motorola type µP interface mode it should be connected to V_{DD}.
$\overline{INT}$	OD	**Interrupt Request**. The signal is activated when the IDEC requests an interrupt.
RES	I	**Reset**. A "high" on this input brings the IDEC into the reset state.

In addition to 8-bit processors, the IDEC supports a direct connection to 16-bit processors. Thus, through an internal address transformation, it is possible to access all IDEC registers using either even microprocessor addresses only or odd microprocessor addresses only.

Serial Interfaces

Depending on the selected mode, the IDEC supports four physically separate, full duplex serial interfaces, or one full duplex serial interface.

In addition to the data input and data output lines, the serial interface requires a common data clock (input DCL) and a frame synchronization signal (input FSC). Input data is latched on the falling edge of DCL and output data is clocked off on the rising edge of DCL. The IDEC may be programmed so that the data clock rate is either equal to the data rate, or twice the data rate.

2.4 Individual Functions

2.4.1 Channel Access

The four HDLC controllers of the IDEC are connected to the serial interfaces as shown in **table 3**. The table indicates the selection of the data channel, the selectable time slot widths, the output driver type, and the function of the active-low Tri-State Control ($\overline{TSC}$) output in each of the operating modes.

The data output is set in a high impedance state outside the time channel where data is transmitted.

OD = Open-drain driver,
PP = Push-pull driver.
The output driver type refers to the SD0X (or SD0X, SD1 X, SD2X and SD3X) outputs.
$\overline{TSC}$ is a push-pull signal.

Quad Connection Time-Slot Mode

Channel selection is performed via the Time-Slot Select Registers (TSR). For each HDLC channel, the 8- bit TSR register gives the position of a time slot with a two-bit resolution. The length of the time slot, either 1, 2, 7 or 8 bits, can be selected using the MODE register (CCS1, 0). These parameters are common to the receive and the transmit channel.

In the case where the number of bits in a PCM frame is 256 or 512, the frame synchronization signal FSC need not be provided at every PCM frame beginning, since bit counters are automatically reset at frame end. When the PCM frame length is not equal to either 256 or 512 bits, the frame synchronization signal has to be provided at the beginning of every PCM frame.

Table 3
HDLC Controller Channel Selection and Characteristics

Mode		Channel Input				Channel Output				Description
MDS1	MDS0	A	B	C	D	A	B	C	D	
0	0	SD0R	SD0R	SD0R	SD0R	SD0X	SD0X	SD0X	SD0X	Single connection TS mode
0	1	SD0R	SD1R	SD2R	SD3R	SD0X	SD1X	SD2X	SD3X	Quad connection common control mode
1	0	SD0R	SD0R	SD0R	SD0R	SD0X	SD0X	SD0X	SD0X	Single connection IOM mode
1	1	SD0R	SD1R	SD2R	SD3R	SD0X	SD1X	SD2X	SD3X	Quad connection TS mode

Mode		Channel Characteristics		Tri-State Control ($\overline{TSC}$) Signal	Output Driver
MDS1	MDS0	Channel Select	Channel Width	Defined by	
0	0	TSR A-D registers	1, 2, 7, 8	TSR A-D	PP or OD
0	1	FSC strobe	Arbitrary	FSC inverted	PP or OD
1	0	Fixed two-bit TS´s	2	Fixed two-bit TS´s A-D	OD
1	1	TSR A-D registers	1, 2, 7, 8	TSR B	PP or OD

OD = Open-drain driver,
PP = Push-pull driver.
The output driver type refers to the SD0X (or SD0X, SD1X, SD2X and SD3X) outputs.
$\overline{TSC}$ is a push-pull signal.

The tristate control output line $\overline{TSC}$ marks the time slot when data is transmitted/received by the HDLC controller B.

The position of a time slot with respect to FSC, as a function of the TSR register contents, is shown in **figure 6**.

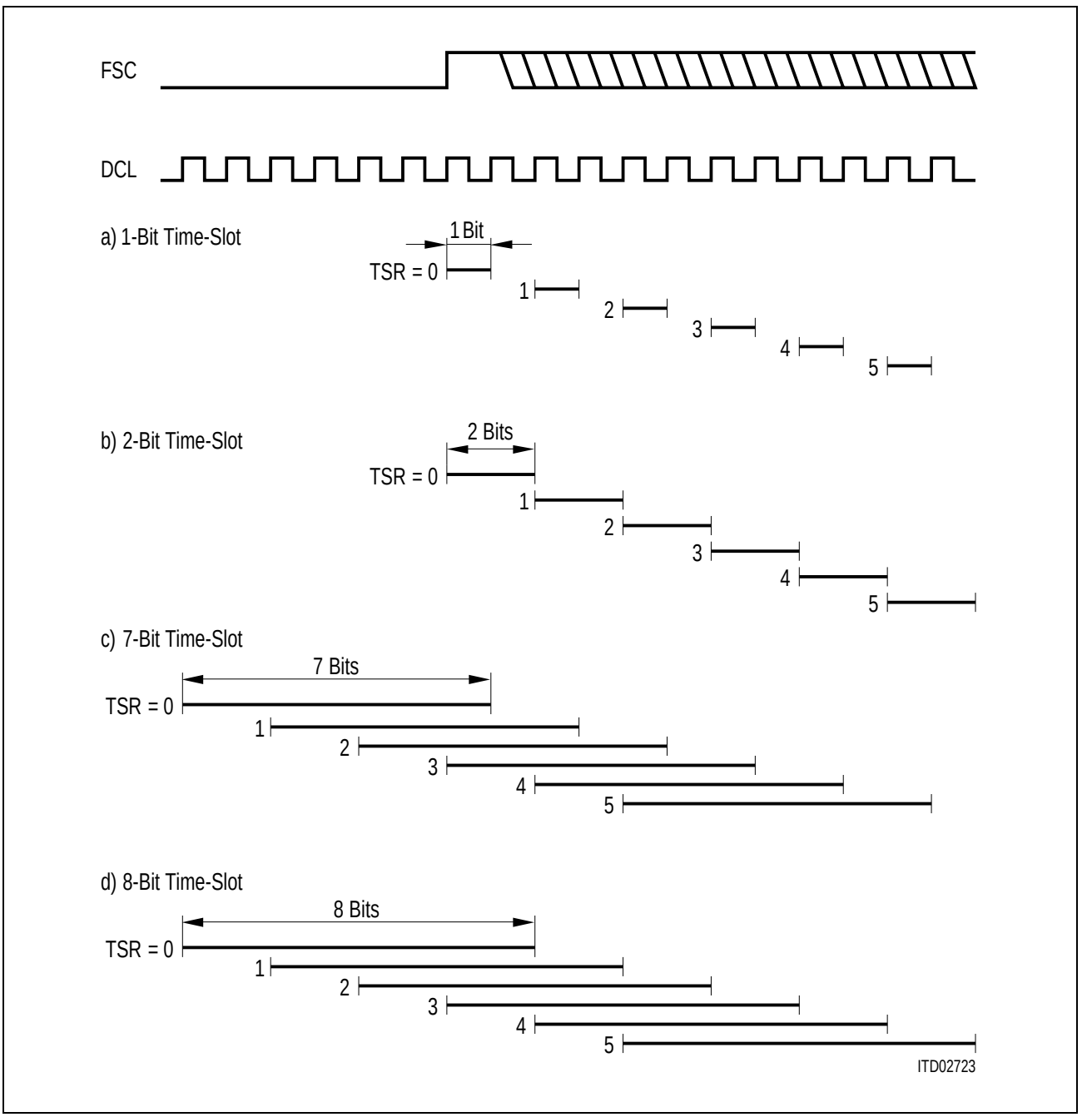


Figure 6
Position of Time Slot for Different Channel Widths as a Function of TSR Register Contents

Quad Connection Common Control Mode

Channel selection is performed by an active high strobe signal provided through the FSC input. The strobe signal is common to all four HDLC channels.

The $\overline{\text{TSC}}$ output is active when the FSC strobe is active.

Single ConnectionTS Mode

The time slots selected by the TSR registers all pertain to the same PCM highway. The programming of a channel otherwise proceeds exactly as explained above.

The tristate control output line $\overline{\text{TSC}}$ marks the time slots when data is transmitted/received by any of the four controllers.

Single Connection IOM - Mode

The IOM is an interface where a frame is composed of n IOM channels (n Š 1; n = 8 in **figure 7**). Each IOM channel has a unique structure. It consists of: two eight-bit bytes, corresponding to the ISDN B channels, a MONITOR byte, and a control byte of which the first two bits are allocated to the ISDN D channel.

In the single connection IOM mode the serial interface has an IOM frame structure and the four HDLC channels are assigned to the D bits of four consecutive IOM channels. The choice whether the four HDLC controllers are assigned to IOM channels 0 - 3 or 4 - 7 is governed by the microcontroller bit VIS (Common Configuration Register). See **figure 7**.