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SIEMENS

ICs for Communications

ISDN SubscribernAccess Controller
ISAC®.-S

PEB 2085

PEB 2086

User's Manual 10.94

PEB 2085/PEB 2086 **Revision History: 10.94**	
Previous Releases: **11.88; 3.89; 12.89; 02.95**	
Page	Subjects (changes since last revision)
	The present documentation is an editorial update of the Technical Manual 12.89

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **“Processing Guidelines”** and **“Quality Assurance”** for ICs, see our **“Product Overview”**.

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Introduction

The PEB 2085/2086 ISAC®-S implements the four-wire S/T interface used to link voice/data terminals to an ISDN.

The PEB 2085 combines the functions of the S-Bus Interface Circuit (SBC: PEB 2080) and the ISDN Communications Controller (ICC: PEB 2070) on one chip.

The component switches B and D channels between the S/T and the ISDN Oriented Modular (IOM®) interfaces, the latter being a standard backplane interface for the ISDN basic access.

The device provides all electrical and logical functions of the S/T interface, such as: activation/ deactivation, mode dependent timing recovery and D channel access and priority control.

The HDLC packets of the ISDN D channel are handled by the ISAC-S which interfaces them to the associated microcontroller. In one of its operating modes the device offers high level support of layer-2 functions of the LAPD protocol.

The ISAC-S is a CMOS device, available in a P-DIP-40 (PEB 2085 only), P-LCC-44 and P-MQFP-64 (PEB 2086 only) package. It operates from a single + 5 V supply and features a power-down state with very low power consumption.

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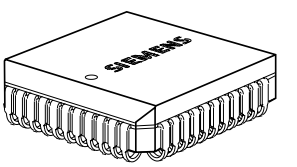
ISDN Subscriber Access Controller ISAC®-S

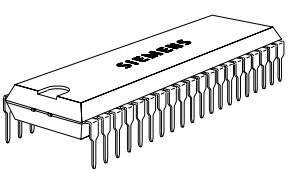
PEB 2085
CMOS IC

1 Features

1.1 Features of PEB 2085



P-LCC-44-1



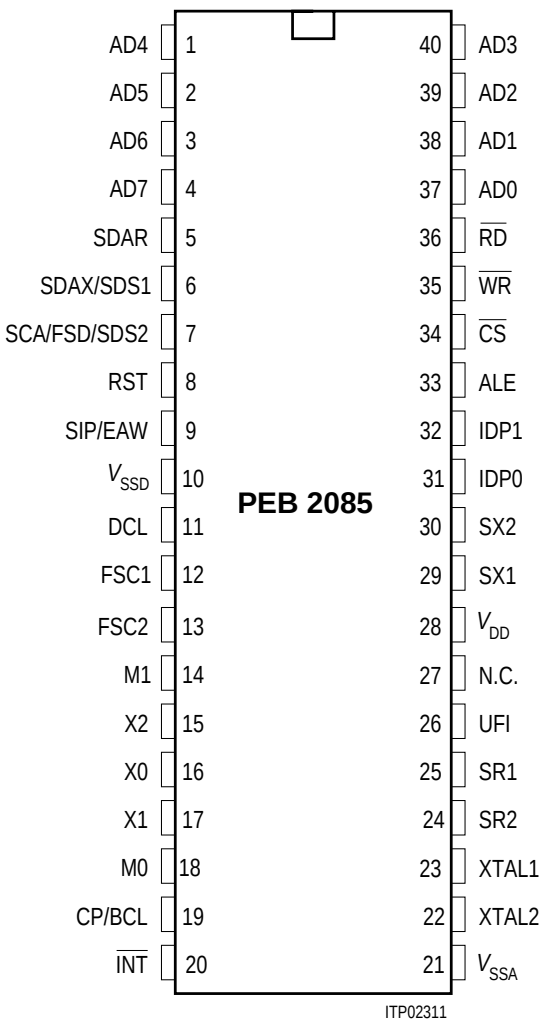
P-DIP-40-2

- Full duplex 2B + D S/T interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T interface and IOM
- Receive timing recovery according to selected operating mode
- D-channel access control
- Activation and deactivation procedures, with automatic wake-up from power-down state
- Access to S and Q bits of S/T interface
- Adaptively switched receive thresholds
- Frame alignment with absorption of phase wander in NT2 network side applications
- Support of LAPD protocol
- FIFO buffer (2×64 bytes) for efficient transfer of D-channel packets
- 8-bit microprocessor interface, multiplexed or non-multiplexed
- Serial interfaces: IOM-1, SLD, SSI
  IOM-2
- Implementation of IOM-1/IOM-2 MONITOR and C/I channel protocol to control peripheral devices
- µP access to B-channels and intercommunication channels
- B-channel switching
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption: standby 8 mW
  active 80 mW

Type	Ordering Code	Package
PEB 2085N	Q67100-H6218	P-LCC-44-1 (SMD)
PEB 2085P	Q67100-H6219	P-DIP-40-2

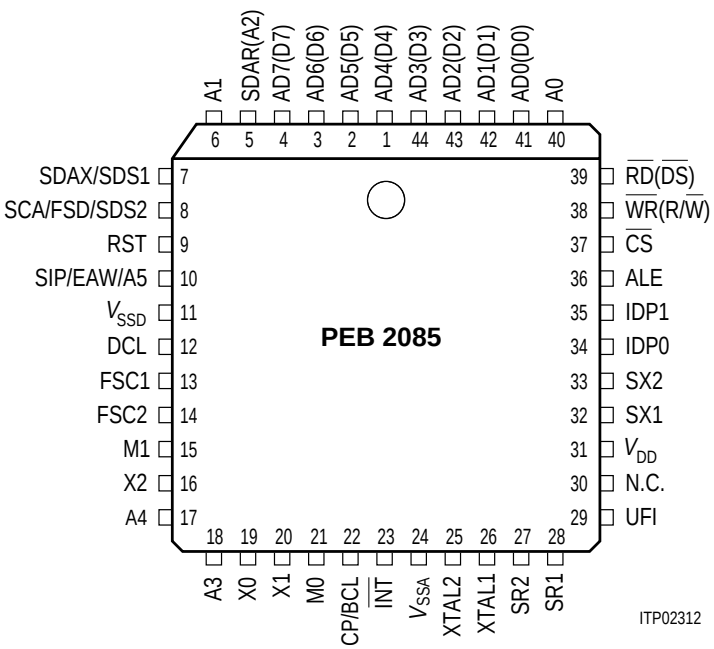
Pin Configurations
(top view)

P-DIP-40



ITP02311

P-LCC-44



ITP02312

1.1.1 Pin Definitions and Functions of PEB 2085

Pin No. P-DIP-40	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
37 38 39 40 1 2 3 4	41 42 43 44 1 2 3 4	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** Address/data bus transfers addresses from the µP system to the ISAC-S and data between the µP system and the ISAC-S. **Non-Multiplexed Bus Mode:** Data bus. Transfers data between the µP system and the ISAC-S.
34	37	$\overline{CS}$	I	**Chip Select:** A "Low" on this line selects the ISAC-S for a read/write operation.
	38	R/$\overline{W}$	I	**Read/Write:** When "High" identifies a valid µP access as a read operation. When "Low", identifies a valid µP access as a write operation (Motorola bus mode).
35	38	$\overline{WR}$	I	**Write:** This signal indicates a write operation (Intel bus mode).
	39	$\overline{DS}$	I	**Data Strobe:** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
36	39	$\overline{RD}$	I	**Read:** This signal indicates a read operation (Intel bus mode).
20	23	$\overline{INT}$	OD	**Interrupt Request:** The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
33	36	ALE	I	**Address Latch Enable:** A high on this line indicates an address on the external address bus (multiplexed bus type only). ALE also selects the microprocessor interface type (multiplexed or non-multiplexed) P-LCC only.

Pin Definitions and Functions of PEB 2085 (cont'd)

Pin No. P-DIP-40	Pin No. P-LCC-44	Symbol	Input (I) Output (O)	Function
7	8	SCA	O	**Serial Clock Port A,** IOM-1 timing mode 0. A 128-kHz data clock signal for serial port A (SSI).
7	8	FSD	O	**Frame Sync Delayed,** IOM-1 timing mode 1. An 8-kHz synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round-trip delay for B1 and B2 channels is guaranteed.
7	8	SDS2	O	**Serial Data Strobe 2,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on the IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on its function only after a write access to SPCR is made.
8	9	RST	I/O	**Reset:** A "High" on this input forces the ISAC-S into reset state. The minimum pulse length is four DCL clock periods or four ms. If the terminal specific functions are enabled, the ISAC-S may also supply a reset signal.
12	13	FSC1	I/O	**Frame Sync 1:** LT-S/NT/LT-T: input synchronization signal, IOM-1 and IOM-2 mode TE: a programmable strobe output, selecting either B1 or B2 channel on the SSI interface, IOM-1 mode TE: frame sync output, "High" during channel 0 on the IOM-2 interface, IOM-2 mode.
13	14	FSC2	I/O	**Frame Sync 2:** LT-S/LT-T/NT: input synchronization signal IOM®-1 and IOM®-2 mode TE: programmable strobe output, selecting either B1 or B2 channel on the SSI interface. TE: Pull-up connection for IDP1, IOM-2 mode.
11	12	DCL	I/O	**Data Clock:** Clock of frequency equal to twice the data rate on the IOM interface LT-S/LT-T: clock input 512-kHz IOM-1 mode 4096-kHz IOM-2 mode TE: clock output 512-kHz IOM-1 mode 1536-kHz IOM-2 mode NT: clock input 512-kHz

Pin Definitions and Functions of PEB 2085 (cont'd)

Pin No. P-DIP-40	Pin No. P-LCC-44	Symbol	Input (I) Output (O)	Function
–	40	A0	I	**Address Bit 0** (Non-multiplexed bus type).
–	6	A1	I	**Address Bit 1** (Non-multiplexed bus type).
–	5	A2	I	**Address Bit 2** (Non-multiplexed bus type).
5	5	SDAR	I	**Serial Data Port A Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
–	18	A3	I	**Address Bit 3** (Non-multiplexed bus type).
–	17	A4	I	**Address Bit 4** (Non-multiplexed bus type).
–	10	A5	I	**Address Bit 5** (Non-multiplexed bus type)
9	10	SIP	I/O	**SLD Interface Port,** IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels.
9	10	EAW	I	**External Awake** (termina specific function). If a falling edge on this input is detected, the ISAC-S generates an interrupt and, if enabled, a reset pulse.
6	7	SDAX	O	**Serial Data Port A Transmit,** IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels.
6	7	SDS1	O	**Serial Data Strobe 1,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on its function only after a write access to SPCR is made.
14	15	M1	I	Setting of operating mode (**see chapter 2.2**).
18	21	M0	I	
15	16	X2	I/O	Mode specific function pins (**see chapter 2.2**).
17	20	X1	I/O	
16	19	X0	I	
19	22	CP	I/O	**Clock Pulses**/Special purpose pin, IOM-1 mode and IOM-2 (except TE) mode
19	22	BCL	O	**Bit Clock:** Clock of frequency 768 kHz, IOM-2 mode in TE.

Pin Definitions and Functions of PEB 2085 (cont'd)

Pin No. P-DIP-40	Pin No. P-LCC-44	Symbol	Input (I) Output (O)	Function
10	11	V_{SSD}	–	Digital ground
21	24	V_{SSA}	–	Analog ground
28	31	V_{DD}	–	Power supply (5 V ± 5%)
23 22	26 25	XTAL1 XTAL2	I O	Connection for crystal or external clock input Connection for external crystal. Left unconnected if external clock is used.
24 25	27 28	SR2 SR1	I O	**S Bus Receiver Input** **S Bus Receiver Output** (2.5 V reference)
26	29	UFI	O	Connection for external pre-filter for S Bus receiver, if used.
29 30	32 33	SX1 SX2	O O	**S Bus Transmitter Output** (positive) **S Bus Transmitter Output** (negative)
31 32	34 35	IDP0(DD) IDP1(DU)	I/O I/O	**IOM Data Port 0 (DD)** **IOM Data Port 1 (DU)** IOM-1: IDP1: Open-drain with internal pull-up resistor IDP0: Push-pull IOM-2: Open drain without internal pull-up resistor or push-pull (ADF2:ODS)

1.1.2 Logic Symbol of PEB 2085

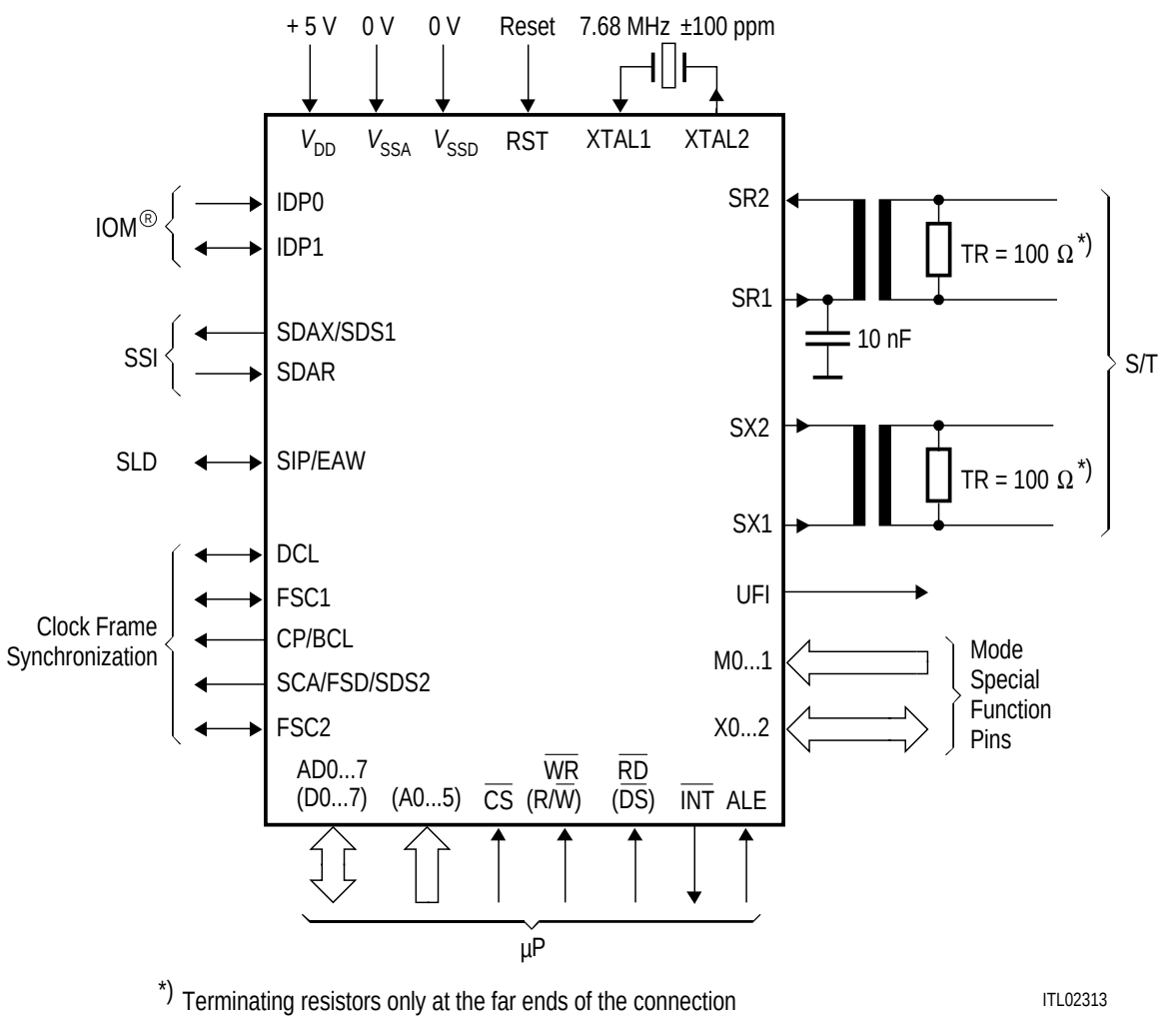


Figure 1
Logic Symbol of the ISAC®-S

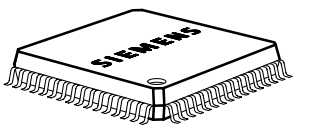
ISDN Subscriber Access Controller ISAC®-S

PEB 2086
CMOS IC

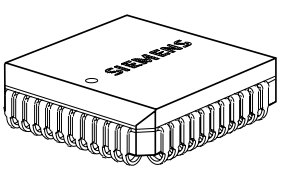
1.2 Features of PEB 2086

Enhanced version of the PEB 2085 with following new features:

- Symmetrical S/T-interface receiver
- B-channel mapping on SSI-interface
- Demultiplexed microprocessor interface in IOM®-1 mode
- Multiframe synchronization



P-MQFP-64-11



P-LCC-44-1

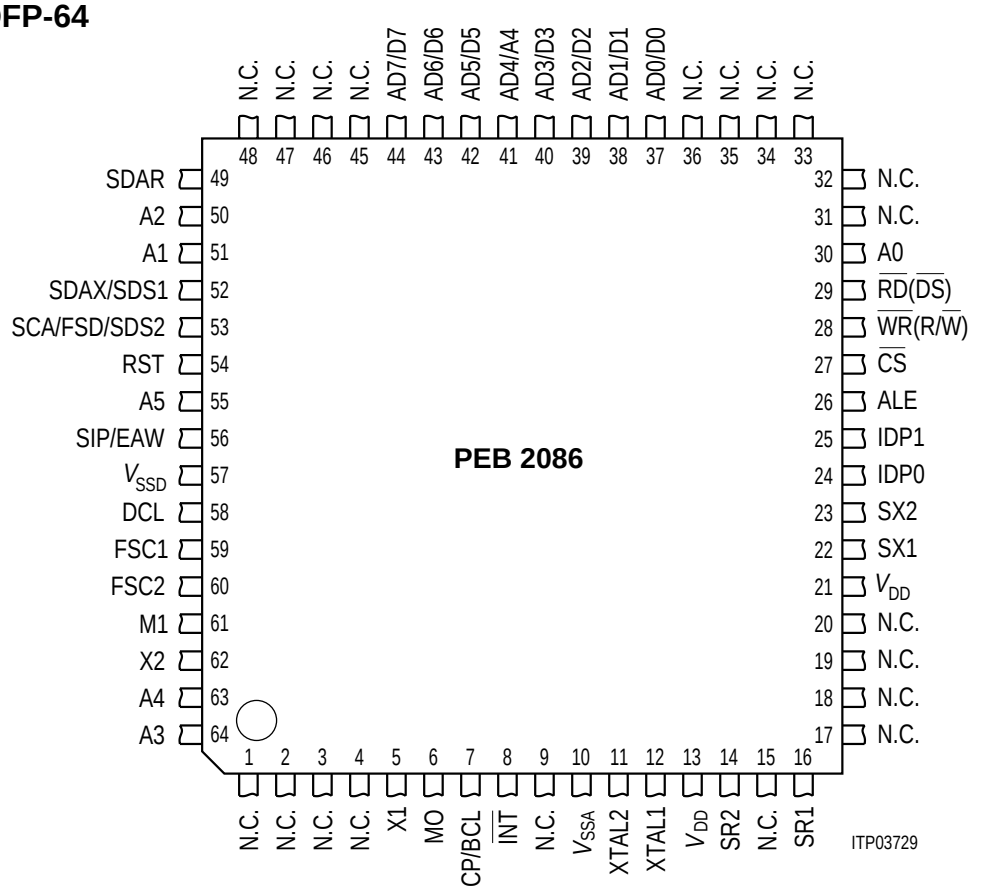
Type	Ordering Code	Package
PEB 2086H	Q67100-H6307	P-MQFP-64-1 (SMD)
PEB 2086N	Q67100-H6356	P-LCC-44-1 (SMD)

The PEB 2086 is an enhanced version of the PEB 2085. The PEB 2086 includes a symmetrical S/T-interface receiver and may use the M-bit of the S/T-interface frame for synchronization purposes.

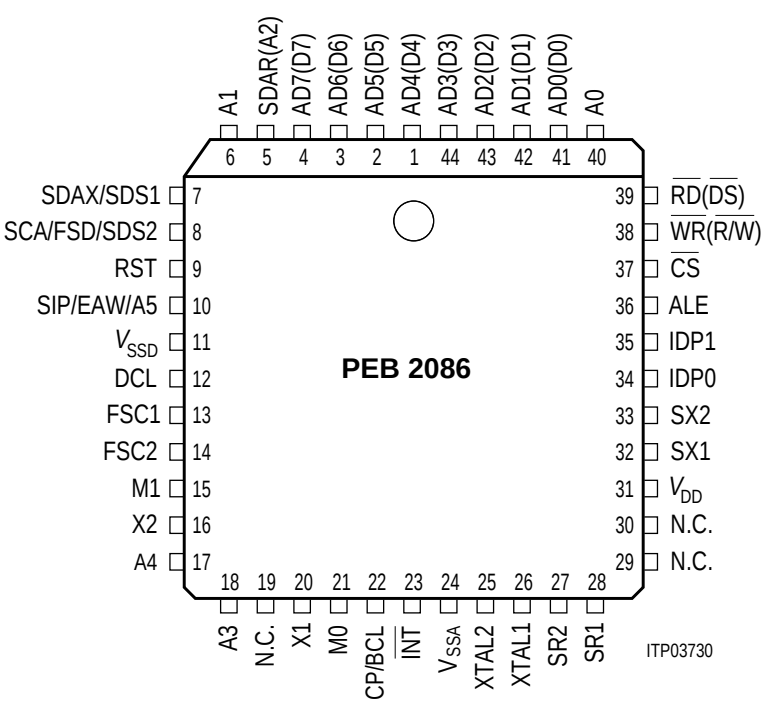
The PEB 2086 is software compatible to the PEB 2085.

Pin Configuration
(top view)

P-MQFP-64



P-LCC-44



1.2.1 Pin Definitions and Functions of PEB 2086

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
37 38 39 40 41 42 43 44	41 42 43 44 1 2 3 4	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** Address/data bus transfers addresses from the µP system to the ISAC-S and data between the µP system and the ISAC-S. **Non-Multiplexed Bus Mode**: Data bus. Transfers data between the µP system and the ISAC-S.
27	37	$\overline{CS}$	I	**Chip Select**: A “Low“ on this line selects the ISAC-S for a read/write operation.
28	38	R/$\overline{W}$	I	**Read/Write**: When “High“ identifies a valid µP access as a read operation. When “Low“, identifies a valid µP access as a write operation (Motorola bus mode).
28	38	$\overline{WR}$	I	**Write**: This signal indicates a write operation (Intel bus mode).
29	39	$\overline{DS}$	I	**Data Strobe**: The rising edge marks the end of a valid read or write operation (Motorola bus mode).
29	39	$\overline{RD}$	I	**Read**: This signal indicates a read operation (Intel bus mode).
8	23	INT	OD	**Interrupt Request**: The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
26	36	ALE	I	**Address Latch Enable**: A high on this line indicates an address on the external address bus (multiplexed bus type only). ALE also selects the microprocessor interface type (multiplexed or non-multiplexed).

Pin Definitions and Functions of PEB 2086 (cont'd)

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
53	8	SCA	O	**Serial Clock Port A**, IOM-1 timing mode 0. A 128-kHz data clock signal for serial port A (SSI).
53	8	FSD	O	**Frame Sync Delayed**, IOM-1 timing mode 1. An 8-kHz synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round-trip delay for B1- and B2-channels is guaranteed.
53	8	SDS2	O	**Serial Data Strobe 2**, IOM-2 mode. A programmable strobe signal, selecting either one or two B- or IC-channels on the IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on its function only after a write access to SPCR is made.
54	9	RST	I/O	**Reset**: A "High" on this input forces the ISAC-S into reset state. The minimum pulse length is four DCL-clock periods or four ms. If the terminal specific functions are enabled, the ISAC-S may also supply a reset signal.
59	13	FSC1	I/O	**Frame Sync 1**: LT-S/NT/LT-T: input synchronization signal, IOM-1 and IOM-2 mode. TE: a programmable strobe output, selecting either B1- or B2-channel on the SSI-interface, IOM-1 mode. TE: frame sync output, "High" during channel 0 on the IOM-2 interface, IOM-2 mode.
60	14	FSC2	I/O	**Frame Sync 2**: LT-S/LT-T/NT: input synchronization signal, IOM-1 and IOM-2 mode. TE: programmable strobe output, selecting either B1- or B2-channel on the SSI-interface, IOM-1 mode. TE: Pull-up connection for IDP1, IOM-2 mode.

Pin Definitions and Functions of PEB 2086 (cont'd)

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
58	12	DCL	I/O	**Data Clock**: Clock of frequency equal to twice the data rate on the IOM-interface LT-S/LT-T: clock input 512-kHz IOM-1 mode 4096-kHz IOM-2 mode TE: clock output 512-kHz IOM-1 mode 1536-kHz IOM-2 mode NT: clock input 512-kHz
30	40	A0	I	**Address Bit 0** (Non-multiplexed bus type).
51	6	A1	I	**Address Bit 1** (Non-multiplexed bus type).
50	5	A2	I	**Address Bit 2** (Non-multiplexed bus type).
49	5	SDAR	I	**Serial Data Port A Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
64	18	A3	I	**Address Bit 3** (Non-multiplexed bus type).
63	17	A4	I	**Address Bit 4** (Non-multiplexed bus type).
55	10	A5	I	**Address Bit 5** (Non-multiplexed bus type).
56	10	SIP	I/O	**SLD Interface Port**, IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels.
56	10	EAW	I	**External Awake** (terminal specific function). If a falling edge on this input is detected, the ISAC-S generates an interrupt and, if enabled, a reset pulse.
52	7	SDAX	O	**Serial Data Port A Transmit**, IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels.
52	7	SDS1	O	**Serial Data Strobe 1**, IOM-2 mode. A programmable strobe signal, selecting either one or two B- or IC-channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on its function only after a write access to SPCR is made.
61 6	15 21	M1 M0	I I	Setting of operating mode.

Pin Definitions and Functions of PEB 2086 (cont'd)

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
62 5	16 20	X2 X1	I/O I/O	Mode specific function pins.
7 7	22 22	CP BCL	I/O O	**Clock Pulses**/Special purpose pin, IOM-1 mode and IOM-2 (except TE) mode. **Bit Clock**: Clock of frequency 768 kHz, IOM-2 mode in TE.
57	11	V_{SSD}	–	Digital ground
10	24	V_{SSA}	–	Analog ground
13, 21	31	V_{DD}	–	Power supply (5 V ± 5 %)
12 11	26 25	XTAL1 XTAL2	I O	Connection for crystal or external clock input. Connection for external crystal. Left unconnected if external clock is used.
14 16	27 28	SR2 SR1	I I	**S-Bus Receiver Input** **S-Bus Receiver Input**
22 23	32 33	SX1 SX2	O O	**S-Bus Transmitter Output** (positive) **S-Bus Transmitter Output** (negative)
24 25	34 35	IDP0(DD) IDP1(DU)	I/O I/O	**IOM-Data Port 0 (DD)** **IOM-Data Port 1 (DU)** IOM-1: IDP1: Open-drain with internal pull-up resistor IDP0: Push-pull IOM-2: Open drain without internal pull-up resistor or push-pull (ADF2:ODS)

1.2.2 Logic Symbol of PEB 2086

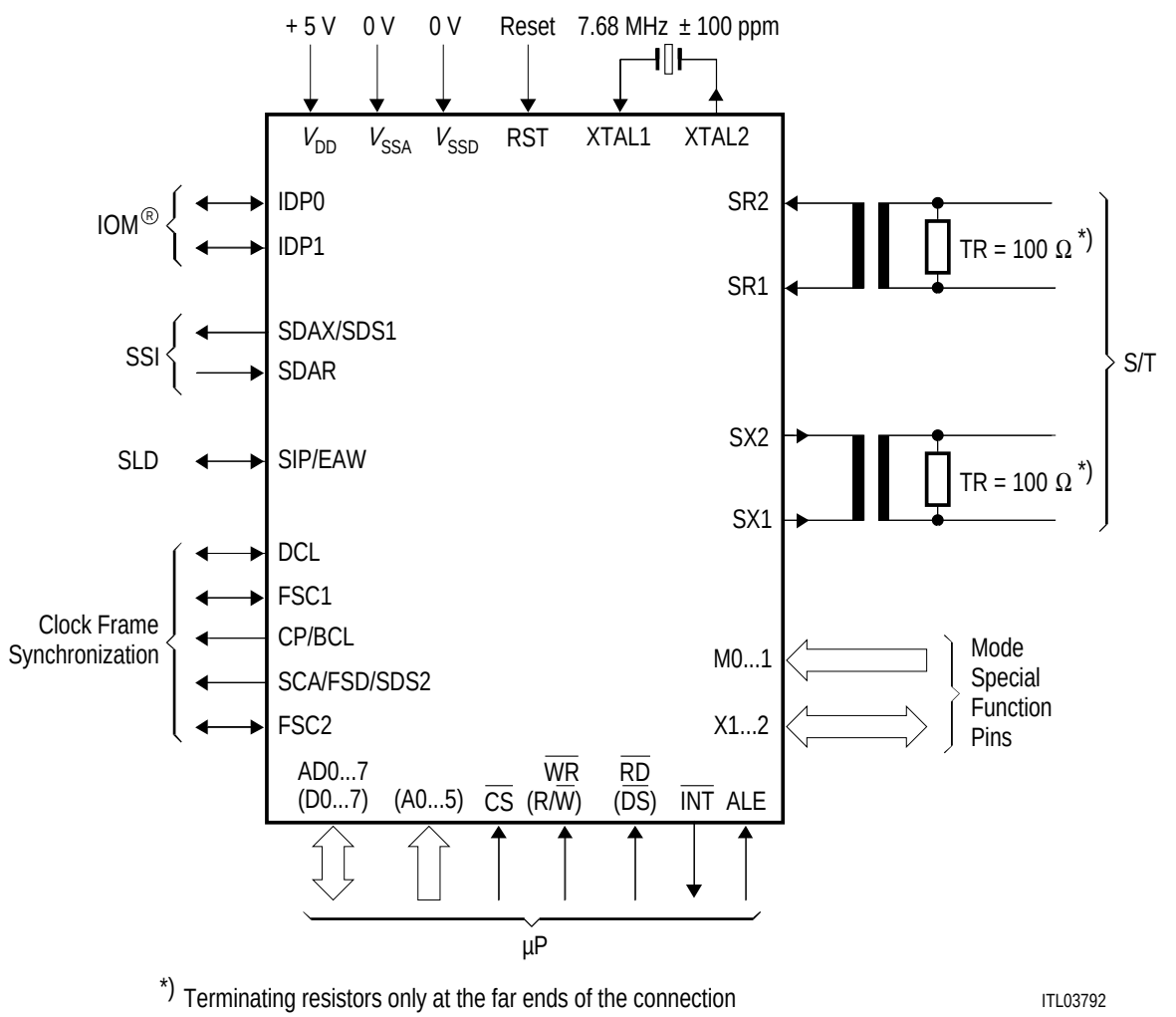


Figure 2
Logic Symbol of the ISAC®-S

1.3 Functional Block Diagram

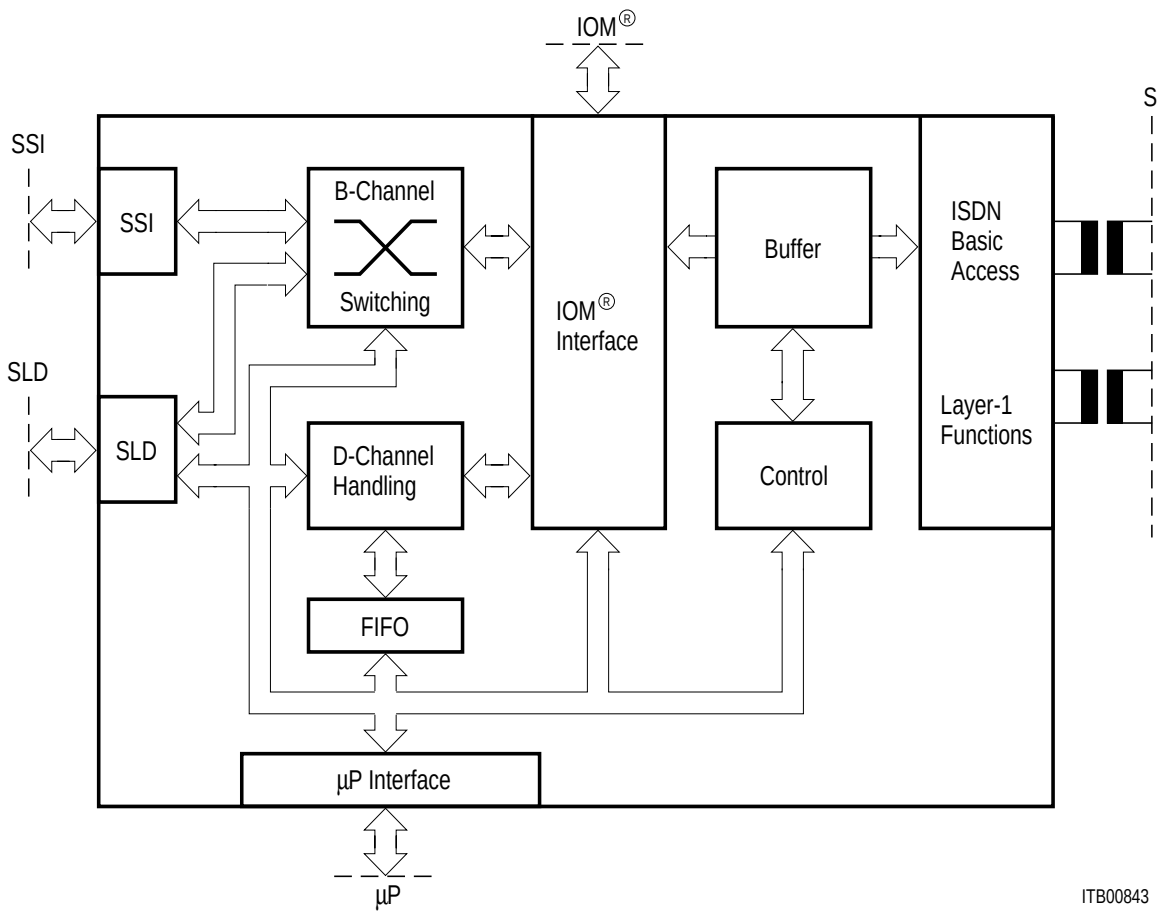


Figure 3
Block Diagram of the ISAC®-S

1.4 System Integration

1.4.1 ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

– an exchange and trunk line termination in the central office (ET, LT)

– a remote network termination in the user area (NT)

– a two-wire loop (U interface) between NT and LT

– a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in **figure 4.**

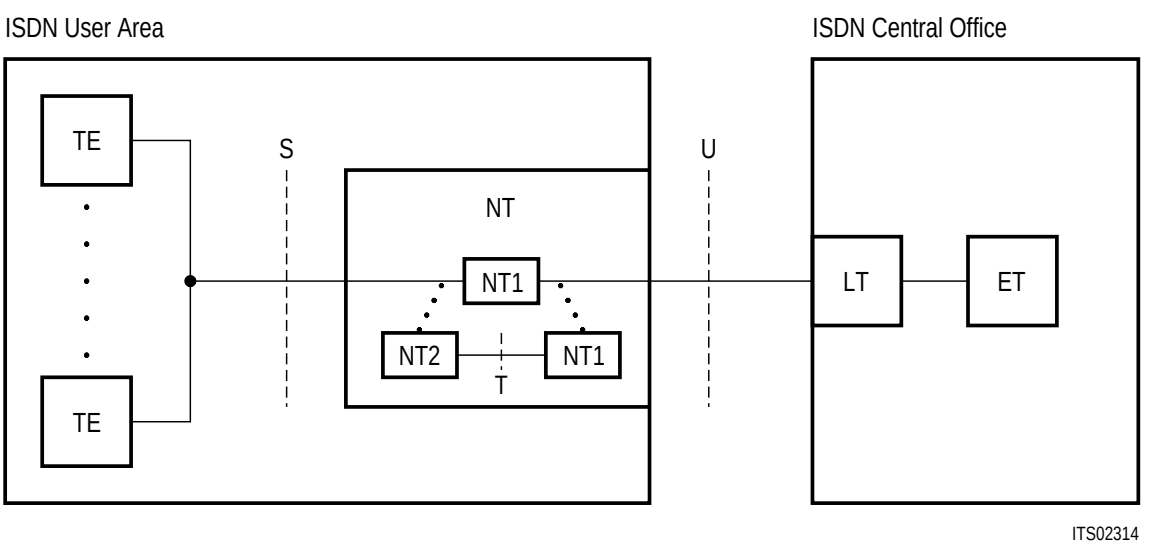


Figure 4
ISDN Basic Subscriber Access Architecture

The NT equipment serves as a converter between the U interface at the exchange and the S interface at the user premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transformation between layer 1 of S and layer 1 of U. NT2 may include higher level functions like multiplexing and switching as in a PABX.

The ISAC-S is designed for the user area of the ISDN basic access, especially for subscriber terminal equipment and for exchange equipment with S interfaces. **Figure 5** illustrates the general applications of the ISAC-S.