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Data Sheet, DS4, February 2001

QuadLIU™

Quad Line Interface Unit for E1/T1/J1

PEB 22504 Version 1.1

Datacom

Infineon technologies

Never stop thinking.

Edition 2001-02

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Revision History:	**2001-02**	DS4
Previous Version:	Data Sheet, DS3, 2000-09	
Page	Subjects (major changes since last revision)	
	5 V supply mode is not supported	
7	**e-mail address changed**	
60	**Global Configuration Register**	
99	**Power Supply Range**	
121	**External Line Frontend Calculator**	
100	**Transmiter output current**	
101	**Receiver sensitivity**	

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Preface

The Quad Line Interface Unit PEB 22504 (QuadLIU™) is a flexible line interface unit for a wide area of telecommunication and data communication applications. The device contains four complete channels on one chip to save board space and power consumption. This document provides complete reference information to configure E1, T1, and J1 applications.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Functional Description**
  This chapter describes the functional blocks and principal operation modes.

- **Chapter 4, Interface Description**
  Describes the various device interfaces.

- **Chapter 5, Operational Description**
  Shows the operation modes and how they are to be initialized.

- **Chapter 6, Register Description**
  Gives a detailed description of all implemented registers and how to use them in different applications/configurations.

- **Chapter 7, Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.

- **Chapter 8, Package Outlines**
  Shows the mechanical values of the device package.

- **Chapter 9, Appendix**
  Gives an example for overvoltage protection and information about application notes and other support.

- **Chapter 10**, **Glossary**
- **Index**

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656 (**page 119**)
ANSI T1.102 (**page 115**)
ANSI T1.231 (**page 71**, **page 89**, **page 90**)
ANSI T1.403 (**page 50**, **page 90**)
AT&T TR43802 (**page 40**)
AT&T TR62411 (**page 40**, **page 44**, **page 49**)
ESD Ass. Standard EOS/ESD-5.1-1993 (**page 98**)
ETSI ETS 300 011 (**page 40**)
ETSI ETS 300 233 (**page 39**, **page 40**, **page 89**)
ETSI TBR12 (**page 40**, **page 42**)
ETSI TBR13 (**page 40**, **page 42**)
FCC68 (**page 47**)
IEEE 1149.1 (**page 33**)
ITU-T G.703 (**page 40**)
ITU-T G.736-739 (**page 40**)
ITU-T G.775 (**page 39**, **page 39**, **page 89**, **page 89**)
ITU-T G.823 (**page 40**)
ITU-T G.824 (**page 40**)
ITU-T I.431 (**page 40**, **page 42**, **page 44**, **page 47**)
MIL-Std. 883D (**page 98**)
Telcordia TR-NWT-1089
TR-TSY 009 (**page 40**)
TR-TSY 253 (**page 40**)
TR-TSY 499 (**page 40**)
UL 1459

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Please provide in the *subject* of your e-mail:
device name (QuadLIU™), device number (PEB 22504), device version (Version 1.1),

and in the *body* of your e-mail:
document type (Data Sheet), issue date (2001-02) and document revision number (DS4).

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1 Overview

The QuadLIU™ PEB 22504 Quad Line Interface Unit is a device to connect four E1/T1/J1 framer devices to four analog or digital lines. The line interface is selectable for long-haul or short-haul applications and fulfills the relevant standards for E1, T1, and J1 systems.

The QuadLIU™ comes in a high-density P-TQFP-100-3 package (SMD) to save a significant amount of board space compared to a configuration using single line-interface circuits.

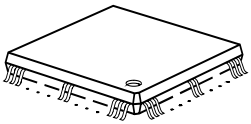
Crystal-less jitter attenuation with only one master clock source further reduces the amount of required external components.

Equipped with a flexible microcontroller interface, it fits to any control processor environment.

Quad Line Interface Unit for E1/T1/J1 **PEB 22504**
QuadLIU™

Version 1.1 **CMOS**

1.1 Features



P-TQFP-100-3

- High-density generic interface for all E1/T1/J1 applications
- Quad analog receive and transmit circuitry for long- and short-haul applications
- Clock and data recovery using an integrated digital phase-locked loop
- Programmable transmit pulse shapes for E1, T1 and J1 signals
- Maximum line attenuation up to -36 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Noise- and crosstalk-filter, line attenuation status
- Programmable Line Build-Out for CSU signals according to ANSI T1.403 and FCC68 0dB, -7.5dB, -15dB, -22.5 dB
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Jitter specifications of ITU-T I.431 , G.703 , G.736, G.823, ETS 300011, TBR12/13 and AT&T TR62411 met
- Tolerates more than 0.4 UI high frequency input jitter
- Crystal-less wander and jitter attenuation/compensation
- Flexible master clock frequency in the range of 1.02 to 20 MHz
- Power-down function per channel
- Dual- or single-rail digital inputs and outputs to the framer interface
- Unipolar CMI for interfacing fiber-optical transmission routes
- Selectable line codes (HDB3, B8ZS, AMI with zero code suppression)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233, ANSI T1. 403 and T1.231
- Clock generator for jitter-free system/transmit clocks per channel
- Local loop, remote loop and digital loop back for diagnostic purposes

Type	Package
PEB 22504	P-TQFP-100-3

- Alarm and performance monitoring per second
- Two 16-bit counters for code violations and PRBS bit errors
- Insertion and extraction of Alarm Indication Signals (AIS)
- Elastic store for receive or transmit clock wander and jitter compensation
- Controlled slip capability and slip indication
- Programmable elastic buffer size: 256 bits/128 bits/64 bits/32 bits/bypass
- Programmable in-band loop code detection and generation according to TR 62411
- Pseudo-Random Bit Sequence (PRBS) generator and monitor
- Flexible software controlled device configuration

Microprocessor Interface Mode

- 8-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible
- Multiplexed and non-multiplexed address bus operations
- Hardware and software reset options
- One-second timer

General

- Boundary scan standard IEEE 1149.1
- P-TQFP-100-3 package (body size 14 mm × 14 mm)
- Single power supply: 3.3 V
- Temperature range: -40°C to +85°C
- Low power device, typical power consumption 100 mW per channel

Applications

- Wireless Basestations
- ATM and frame relay gateways
- CSUs, DSUs
- Internet access equipment
- LAN/WAN Router
- ISDN-PRI, PABX
- Digital Access Cross-connect Systems (DACS)
- SDH/SONET ADD/DROP Multiplexer

1.2 Logic Symbol

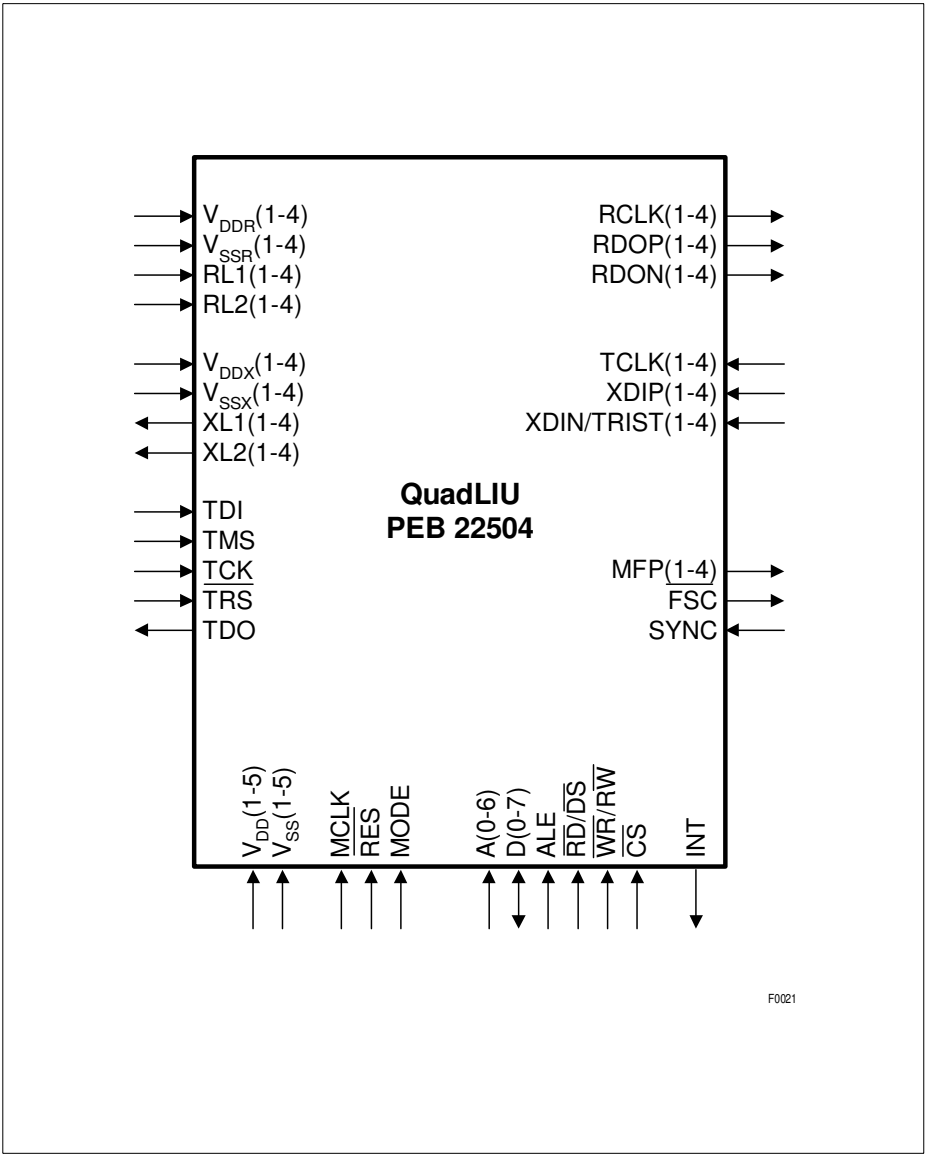


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 shows a multiple link application using the QuadLIU™. **Figure 3** shows a repeater application.

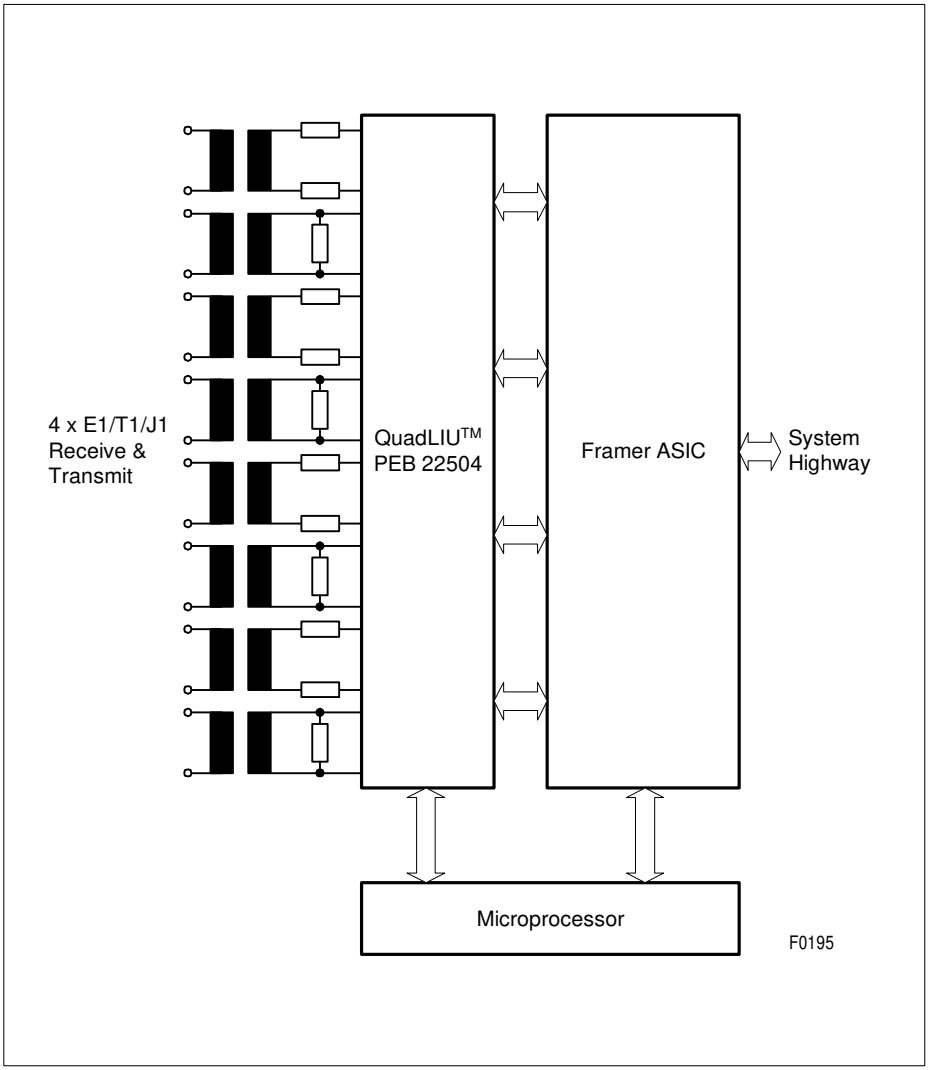


Figure 2 QuadLIU Application

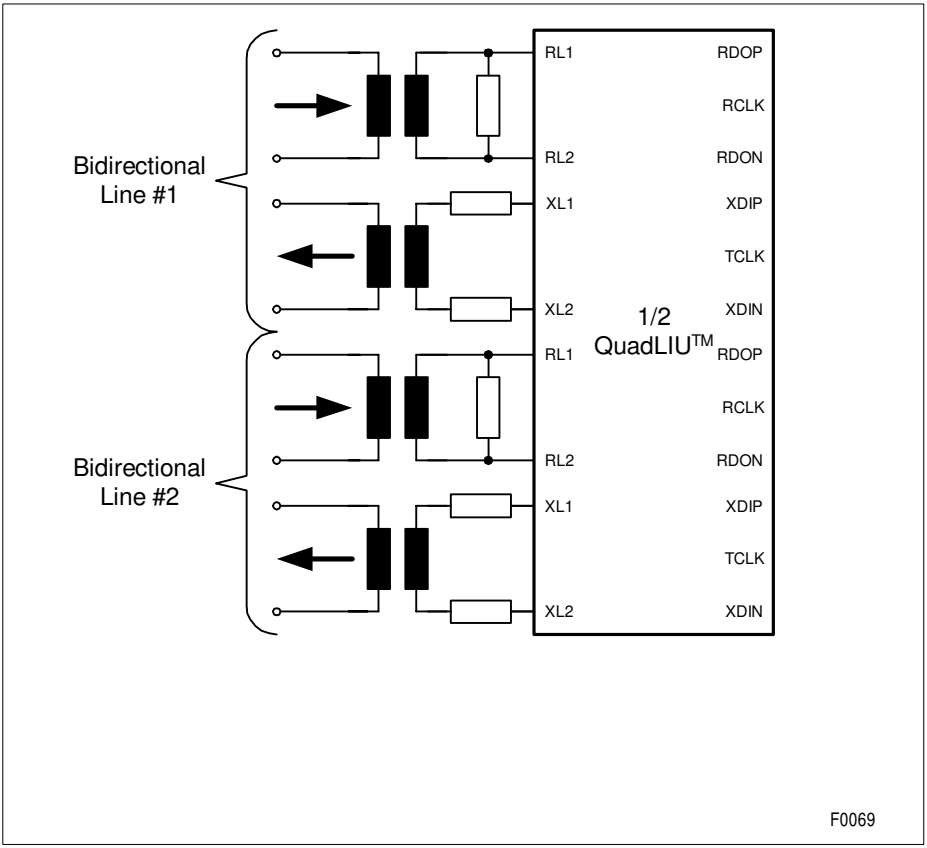


Figure 3 QuadLIU Repeater Application

2 Pin Descriptions

2.1 Pin Diagram

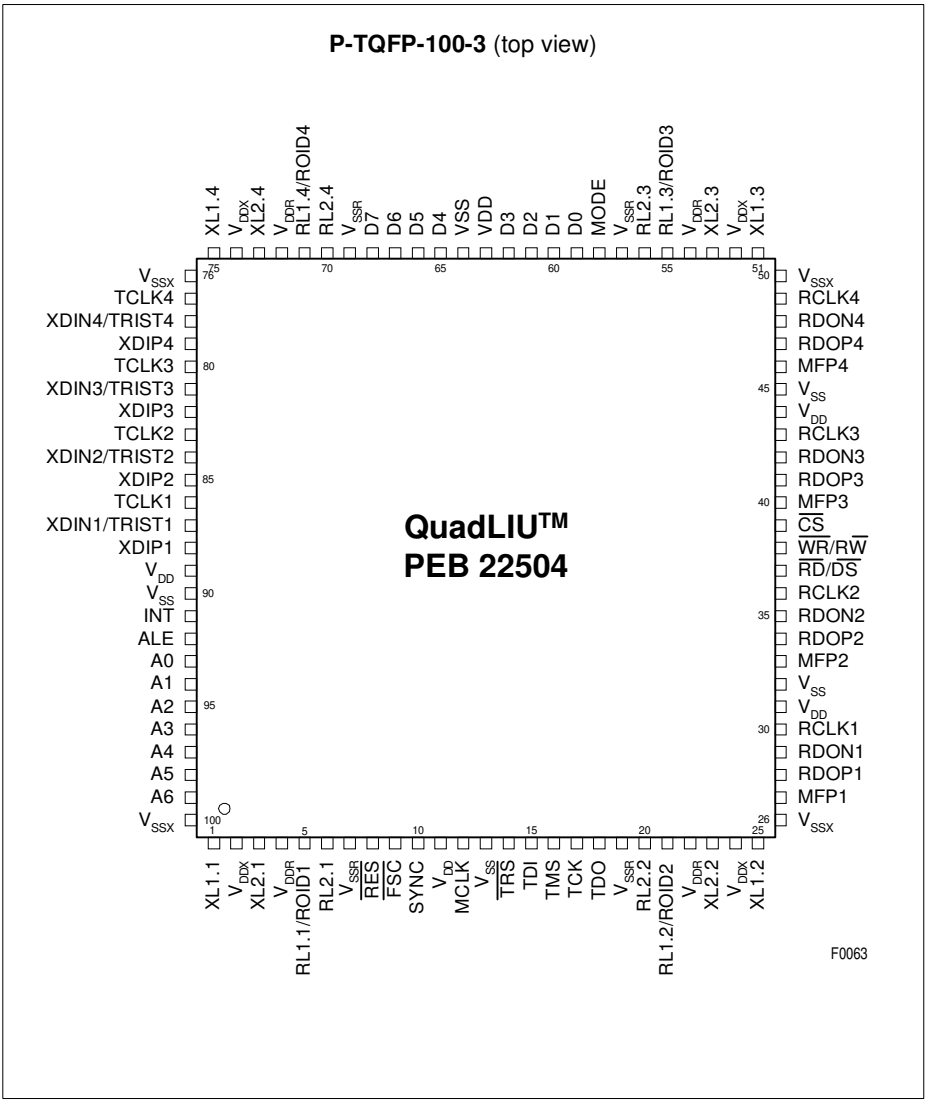


Figure 4 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Control Pin Functions

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
93...99	A(0:6)	I + PU	**Address Bus** Selects one of the internal registers for read or write.
59...62 65...68	D(0:3) D(4:7)	I/O + PU	**Data Bus** Eight-bit-wide bi-directional bus to be connected to the microprocessor data bus.
92	ALE	I + PU	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A(6:0) is internally latched with the falling edge of ALE. This function allows the device to be connected directly to a multiplexed address/data bus. In this case, pins A(6:0) must be connected externally to the data bus pins. In case of demultiplexed mode, this pin has to be connected to V_{SS} or V_{DD} directly.
39	$\overline{CS}$	I + PU	**Chip Select** A low signal selects the device for read/ write operations
37	$\overline{RD}$	I + PU	**Read Enable/Data Strobe** (Intel bus mode, MODE=low) This signal indicates a read operation. When the device is selected via $\overline{CS}$, the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed via A(6:0) on to Data Bus.
	$\overline{DS}$	I + PU	**Data Strobe** (Motorola bus mode, MODE=high) This pin serves as input to control read/ write operations.

Table 1 Control Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
38	$\overline{WR}$	I + PU	**WRite Enable/Read-Write Select** (Intel bus mode, MODE=low) This signal indicates a write operation. When $\overline{CS}$ is active the device loads an internal register with data provided via the Data Bus.
	R$\overline{W}$	I + PU	**Read/Write Enable** (Motorola bus mode, MODE=high) This signal distinguishes between read and write operations.
91	INT	O/oD	**INTerrupt Request** General interrupt request output for all interrupt sources. These interrupt sources can be masked individually via register IMR0/1. Interrupt status is reported via register CIS (Channel Interrupt Status) and ISR0/1. Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by using register IPC.

Table 1 Control Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
27, 33, 40, 46	MFP(1:4)		**Multi Function Port** Depending on programming of bits LIM4.PC(2:0) this multifunction port provides different status information of the device as shown in this table below. MFP1 corresponds to channel 1, MFP4 to channel 4.
	LOS(1:4)	O	**Loss-of-Signal Indication** LIM4.PC(2:0) = 000 Active high, if a loss-of-signal alarm is detected. This signal corresponds directly to bit LSR0.LOS.
	ALOS(1:4)	O	**Analog Loss-of-Signal Indication** LIM4.PC(2:0) = 001 Active high, if the input level at RL1/2 drops below the programmed receive input threshold which is defined by register LIM2.RIL(2:0).
	PRBSS (1:4)	O	**PRBS Synchronization Status** LIM4.PC(2:0) = 010 Active high if the Pseudo-Random Bit Sequence (PRBS) synchronization is achieved. This signal corresponds directly to bit LSR0.PRBSS.
	BPV(1:4)	O	**Bipolar Violation Indication** LIM4.PC(2:0) = 011 Active high if a bipolar violation is detected. This signal corresponds directly to the increment signal of the code violation error counter.

Table 1 Control Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
27, 33, 40, 46 (cont'd)	XLS(1:4)	O	**Transmit Line Status** LIM4.PC(2:0) = 100 Active high if the transmit line current limiter exceeds its maximum value. Pins XL1/2 are automatically tristated until the current drops below its maximum value (or the "short" disappears). This signal corresponds directly to bit LSR1.XLS.
	AIS(1:4)	O	**Alarm Indication Signal** LIM4.PC(2:0) = 101 Active high if the alarm indication signal is detected. This signal corresponds directly to bit LSR0.AIS.
10	SYNC	I + PU	**Clock Synchronization** Reference clock for the internal DCOs of the device. Selectable via register GCR.SSF(1:0). Active high pulse input.
9	$\overline{\text{FSC}}$	O	**Frame Synchronization Pulse** The synchronization pulse is active low for one 2.048 (E1)/1.544 MHz (T1/J1) cycle (pulse width = 488/648 ns). $\overline{\text{FSC}}$ is derived from the jitter attenuation DCO, which must be active for $\overline{\text{FSC}}$ output (8-kHz master mode only, GCR.SSF(1:0) = 10). Active low pulse output.
87, 84, 81, 78	TRIST(1:4)	I + PU	**Transmit Line Tristate** If the single-rail data stream is selected by bit LIM0.XC(1:0), a high at these pins set the appropriate XL1/2 outputs into tristate. TRISTi sets XL1.i/2.i of channel i into tristate, where i = 1 to 4.

Table 2 Signal Pin Functions

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
5, 21, 55, 71	RL1(1:4)	I (analog)	**Line Receiver 1** (LIM1.ECMIR = 0, default) Analog input from the external transformer (receive bipolar ring).
	ROID(1:4)	I	**Receive Optical Interface Data** (LIM1.ECMIR = 1) CMI data received from fiber-optical interface with 2048 (E1)/ 1544 kbit/s (T1/ J1). An internal DPLL extracts the receive route clock from the incoming data pulse. The duty cycle of the receiving signal has to be closely to 50 %. RL2 has to be connected to V_{SS} or V_{DD}.
6, 20, 56, 70	RL2(1:4)	I (analog)	**Line Receiver 2** (LIM1.ECMIR = 0, default) Analog input from the external transformer (receive bipolar tip).
1, 25, 51, 75	XL1(1:4)	O (analog)	**Transmit Line 1** (transmit bipolar ring) (LIM1.ECMIX = 0, default) Analog output to the external transformer.
	XOID(1:4)	O	(LIM1.ECMIX = 1) Single-ail CMI output
3, 23, 53, 73	XL2 (1:4)	O (analog)	**Transmit Line 2** (transmit bipolar tip) (LIM1.ECMIX = 0, default) Analog output to the external transformer. If single-rail CMI output is selected (LIM1.ECMIX = 1), this pis is undefined and has to be left open.

Table 2 Signal Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
28, 34, 41, 47	RDOP(1:4)	O	**Receive Data Output/Positive** Received data at RL1/2 is sent on RDOP/ RDON in NRZ format to the framer interface. Clocking of data is done with the rising or falling edge of RCLK(1:4), selected by bit LIM4.RPE. RDOP/RDON are set low if a loss-of-signal alarm is detected. The source of the received data is selected by bit LIM2.RD(1:0).
			LIM2.RD(1:0) = 00: Data recovered by the DPLL is AMI/HDB3/B8ZS decoded and output on RDOP; RDON is not defined.
			LIM2.RD(1:0) = 01: Dual-rail data recovered by the DPLL, not AMI/HDB3/ B8ZS decoded, is output on RDOP/RDON.
			LIM2.RD(1:0) = 10: Sliced data, not recovered by the DPLL is output on RDOP/ RDON. A "1" on RDOP corresponds to a positive pulse on RL1/RL2. A "1" on RDON corresponds to a negative pulse on RL1/ RL2.
29, 35, 42, 48	RDON(1:4)	O	**Receive Data Output/Negative** LIM1.RDON(1:0) = 00 (see above)
	BPV(1:4)	O	**Bipolar Violation Indication** LIM1.RDON(1:0) = 01
	SCLKO	O	**System Clock Output** LIM1.RDON(1:0) = 10
	SCLKI	I + PU	**System Clock Input** LIM1.RDON(1:0) = 11 Read clock for jitter attenuater buffer if internal DCO is not used (see **Figure 10** on **page 38**).

Table 2 Signal Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
88, 85, 82, 79	XDIP(1:4)	I + PU	**Transmit Data In Positive** Transmit data received from the framer interface is output on XL1/2. NRZ data has to be provided on XDIP. Latching of data is done with the rising or falling transitions of TCLK according to LIM4.TPE.
87, 84, 81, 78	XDIN(1:4)	I + PU	**Transmit Data In Negative** If the dual-rail data stream is selected by bits LIM0.XC(1:0) transmit data received from the framer interface is output on XL1/2. NRZ data (AMI negative data) has to be provided on XDIN. Latching of data is done with rising or falling transitions of TCLK according to bit LIM4.TPE.
30, 36, 43, 49	RCLK(1:4)	O	**Receive Clock** The output functions of these ports are defined by register CMR.RS(1:0): CMR.RS(1:0) = 00: Receive Clock extracted from the incoming data pulses. CMR.RS(1:0) = 01: Receive Clock extracted from the incoming data pulses. RCLK is set high in case of loss-of-signal (LSR0.LOS=1). Selected by GCR.R1S(1:0), one of the four RCLK(1:4) is output on RCLK1. The clock frequency is 2.048 (E1)/ 1.544 MHz (T1/J1)
	SCLKO (1:4)	O	CMR.RS(1:0) = 10: Output of de-jittered system clock sourced by DCO. Clock frequency: 2.048 (E1) or 1.544 MHz (T1/J1). See **Figure 10** on **page 38**.