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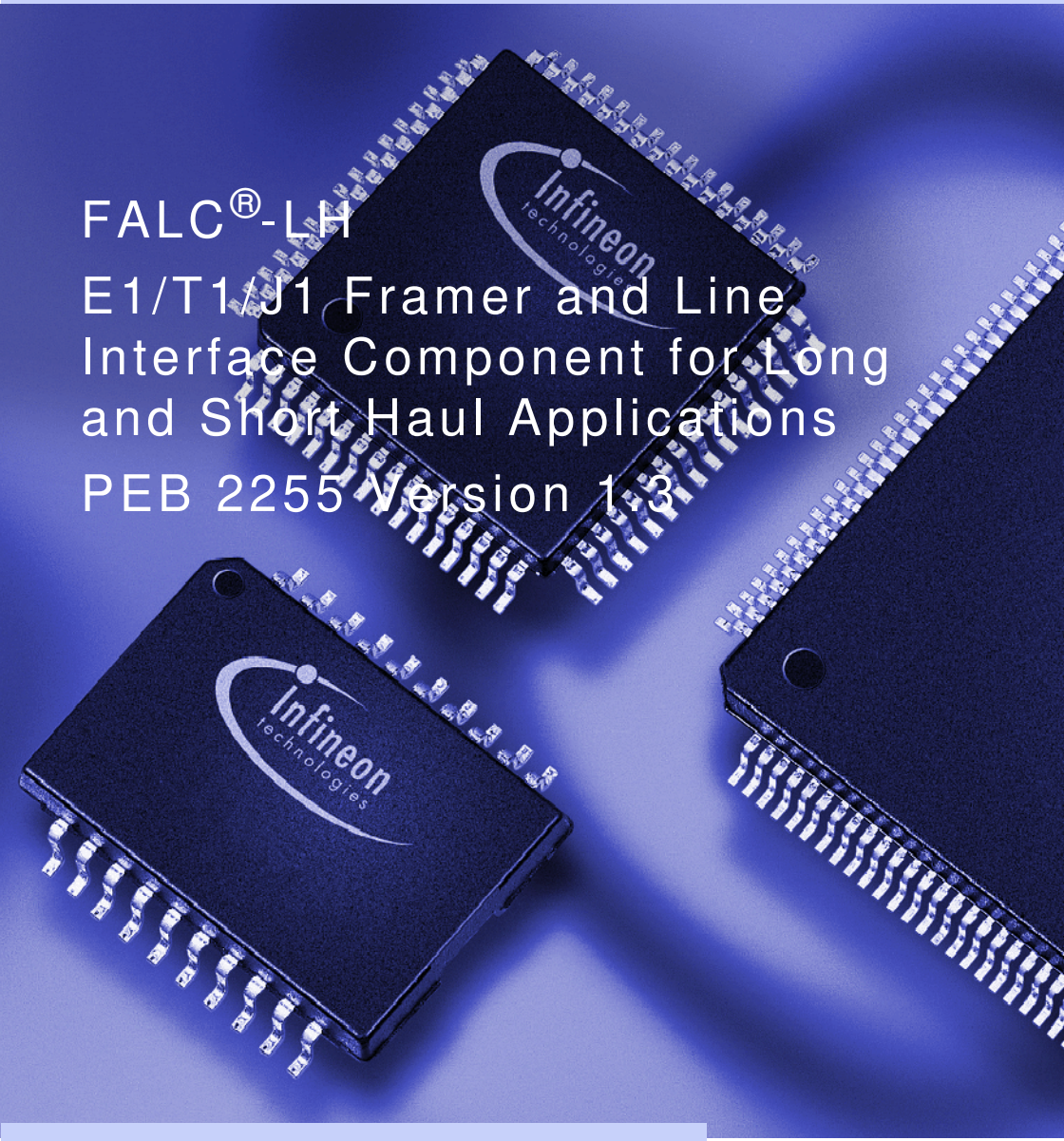
Data Sheet, DS 1, July 2000

FALC®-LH

E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications

PEB 2255 Version 1.3



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Preface

The FALC®-LH framer and line interface component is designed to fulfill all required interfacing between an analog E1/T1/J1 line and the digital PCM system highway/H.100 bus.

The digital functions as well as the analog characteristics are configured via a flexible microprocessor interface.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1**, **Introduction**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2**, **Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3** to **Chapter 5**, **Functional Description E1/T1/J1**
  These chapters describe the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation

- **Chapter 6** and **Chapter 7**, **Operational Description E1/T1/J1**
  Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).

- **Chapter 8**, **Signaling Controller Operating Modes**
  Describes signaling controller functions for both E1 and T1/J1 operation.

- **Chapter 9** and **Chapter 10**, **E1 Registers** and **T1/J1 Registers**
  Gives a detailed description of all implemented registers and how to use them in different applications/configurations.

- **Chapter 11**, **Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.

- **Chapter 12**, **Package Outlines**
  Shows the mechanical values of the device package.

- **Chapter 13**, **Appendix**
  Gives an example for overvoltage protection and information about application notes and other support.

- **Chapter 14**, **Glossary**

- **Index**

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETIS ETS 300 166
ETSI ETS 300 233
ETSI ETS 300 324
ETSI ETS 300 347
ETSI TBR12
ETSI TBR13
FCC Part68
GR-253-CORE
GR-499-CORE
GR-1089-CORE
H.100
H-MVIP
IEEE 1149.1
ITU-T G.703
ITU-T G.704
ITU-T G.705
ITU-T G.706
ITU-T G.732
ITU-T G.735
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU-T G.823
ITU-T G.824
ITU-T G.962
ITU-T G.963
ITU-T G.964
ITU-T I.431
ITU-Q.703
JT-G703
JT-G704
JT-G706
JT-I431
MIL-Std. 883D
TR-TSY-000009
UL 1459

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and in the *body* of your e-mail:
document type (Data Sheet), issue date (2000-07) and document revision number (DS 1).

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1 Introduction

The FALC®-LH framer and line interface component is designed to fulfill all required interfacing between an analog E1/T1/J1 line and the digital PCM system highway, H.100 or H-MVIP bus for world market telecommunication systems.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards. The FALC®-LH offers a generic E1/T1/J1 analog line interface without the need to change external components. Optional crystal-less jitter attenuation reduces the amount of required external components.

Equipped with a flexible microprocessor interface, it connects to any control processor environment. A standard boundary scan interface is provided to support board level testing. Flat pack device packaging, small number of external components and low power consumption lead to reduced overall system costs.

Other members of the FALC® family are the FALC®54 for short haul applications, the FALC®56 for long haul and short haul applications as well as the QuadFALC™ supplying four long haul and short haul interfaces on one single chip.

E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications
FALC®-LH

PEB 2255

Version 1.3

1.1 Features

P-MQFP-80-1

Line Interface

- High density, generic interface for all E1/T1/J1 applications
- Analog receive and transmit circuitry for long haul and short haul applications
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to -43 dB at 1024 kHz (E1)
  and up to -36 dB at 772 kHz (T1/J1)
- Programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1.403 + FCC68 in steps of 0 dB, -7.5 dB, -15 dB and -22.5 dB (T1/J1)
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) are met
- Optional crystal-less wander and jitter attenuation/compensation
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ or CMI coding for interfacing fibre optical transmission routes
- Selectable line codes (E1: HDB3, AMI - T1/J1: B8ZS, AMI with ZCS) for analog interface
- Loss of signal indication with programmable thresholds according to ITU-T G.775 and ETS300233 (E1)/ANSI T1.403, T1.231(T1/J1)
- Clock generator for jitter free system/transmit clocks
- Local loop and remote loop for diagnostic purposes
- Only one type of transformer (ratio 1:$\sqrt{2}$) for E1 75/120 Ω and T1/J1 100/110 Ω

Type	Package
PEB 2255	P-MQFP-80-1

Frame Aligner

- Frame alignment/synthesis for 2048 kbit/s according to ITU-T G.704 (E1) and for 1544 kbit/s according to ITU-T G.704 and JT G.704 (T1/J1)
- Programmable frame formats :
  E1: Doubleframe, CRC Multiframe (E1)
  T1: 4-Frame Multiframe (F4,FT), 12-Frame Multiframe (F12, D3/4), Extended Superframe (F24, ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for recover/loss of frame alignment
- CRC4 to non-CRC4 interworking of ITU-T G. 706 Annex B (E1)
- Error checking via CRC4 procedures according to ITU-T G. 706 (E1)
- Error checking via CRC6 procedures according to ITU-T G. 706 and JT G.706 (T1/J1)
- Performs synchronization in ESF format according to NTT requirements (J1)
- Alarm and performance monitoring per second
  16 bit counter for CRC-, framing errors, code violations, error monitoring via E bit and SA6 bit (E1), errored blocks, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS, Remote/Yellow Alarm, AUXP)
- IDLE code insertion for selectable channels
- 8.192 MHz/2.048 MHz (E1) or 8.192 MHz/1.544 MHz (T1/J1) system clock frequency
- Selectable 2048/4096 kbit/s backplane interface with programmable receive/transmit timeslot offset
- Programmable tristate function of 4096 kbit/s output via RDO
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Supports fractional E1 or T1 access
- Flexible transparent modes
- Programmable In-Band Loop Code detection and generation (TR62411)
- Channel loop back, line loop back or payload loop back capabilities (TR54016)
- Pseudo random bit sequence (PRBS) generator and monitor
- Provides loop-timed mode
- Clear channel capabilities (T1/J1)

Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions, programmable preamble
- DL-channel protocol for ESF format according to ANSI T1.403 or according to AT&T TR54016 (T1/J1)
- DL-channel protocol for F72 (SLC96) format
- CAS controller with last look capability, enhanced CAS- register access and freeze signaling indication
- Robbed bit signaling capability (T1/J1)

- Provides access to serial signaling data streams
- CAS Multiframe synchronization and synthesis according to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in Timeslot 16)
- Transparent mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets.
- Time-slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode

Microprocessor Interface

- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Multiplexed and non-multiplexed address bus operations
- Extended interrupt capabilities
- Hardware and software reset
- One second timer

General

- Boundary scan standard IEEE 1149.1
- P-MQFP-80 package; body size 14x14; pitch 0.65
- 5V power supply
- Typical power consumption 450 mW

Applications

- Wireless Basestations
- E1/T1/J1 ATM Gateways, Multiplexer
- E1/T1/J1 Channel & Data Service Units (CSU, DSU)
- E1/T1/J1 Internet Access Equipment
- LAN/WAN Router
- ISDN PRI, PABX
- Digital Access Cross Connect Systems (DACS)
- SONET/SDH Add/Drop Multiplexer

1.2 Logic Symbol

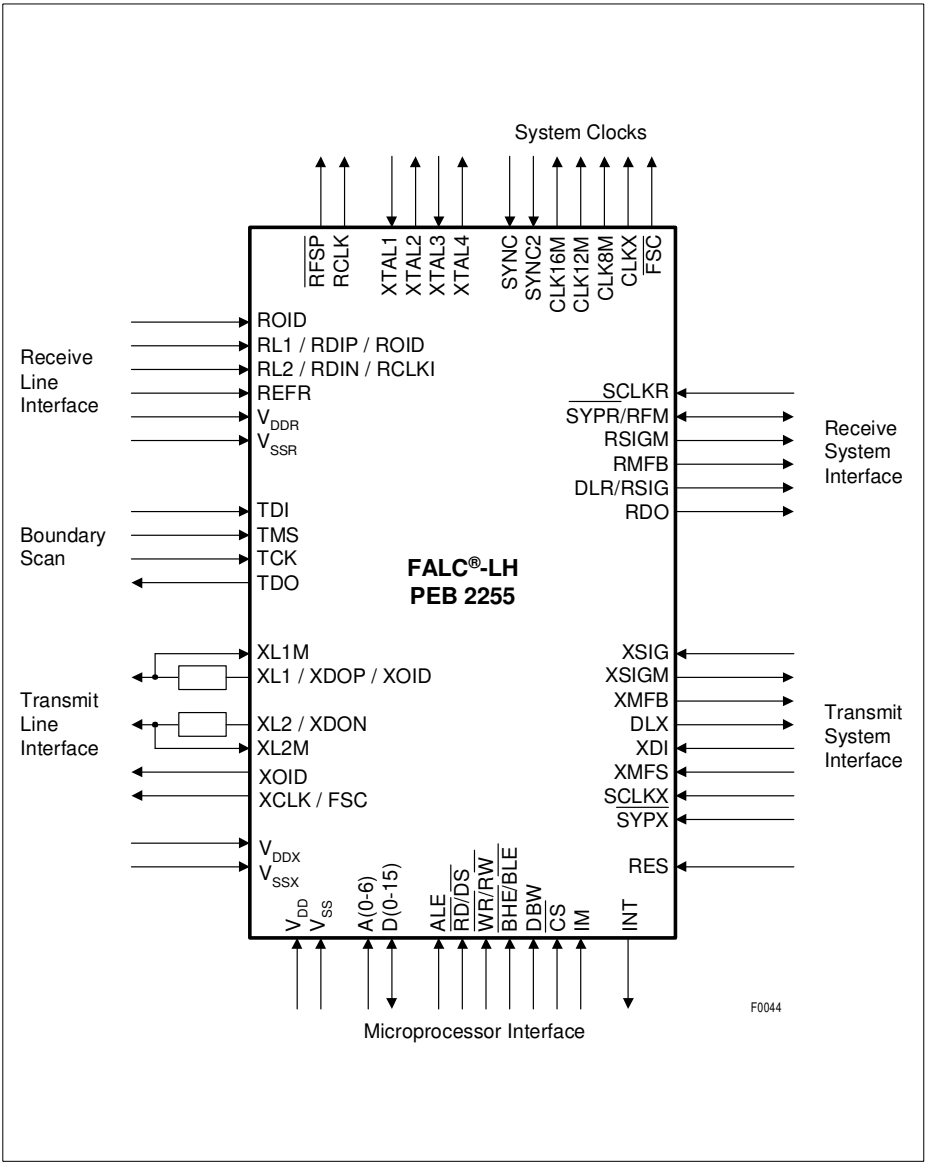

Figure 1 Logic Symbol

1.3 Typical Applications

The figures show a multiple link circuit for Frame Relay applications using the FALC-LH together with the 128 channel HDLC controller M128X and the Memory Timeswitch MTLS as well as an 8 channel interface to the ATM layer combined with n IWE8 device.

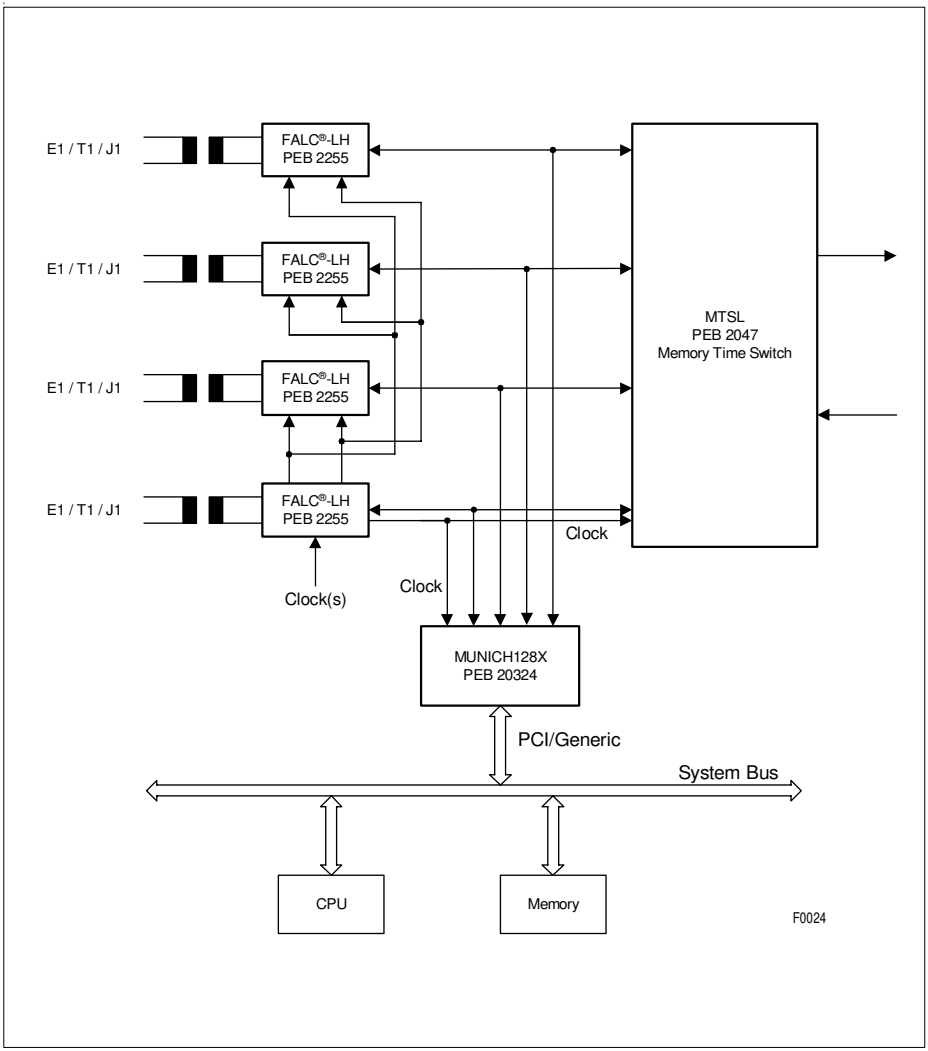

Figure 2 Multiple E1/T1/J1 Link over Frame Relay

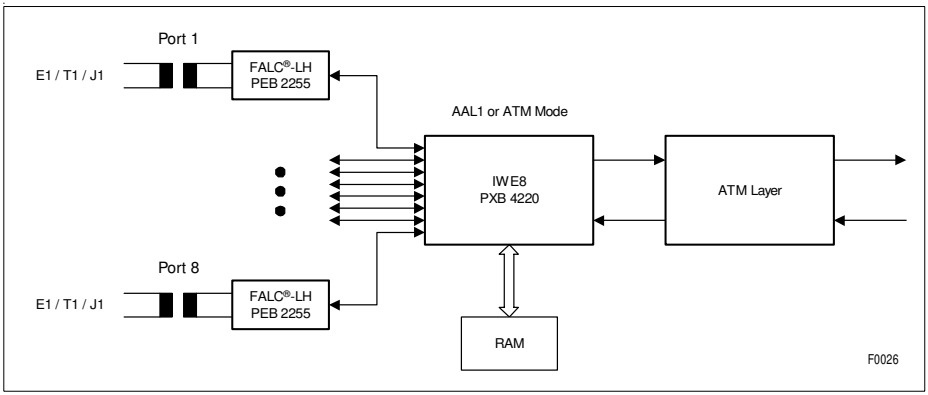

Figure 3 8 Channel E1/T1/J1 Interface to the ATM Layer

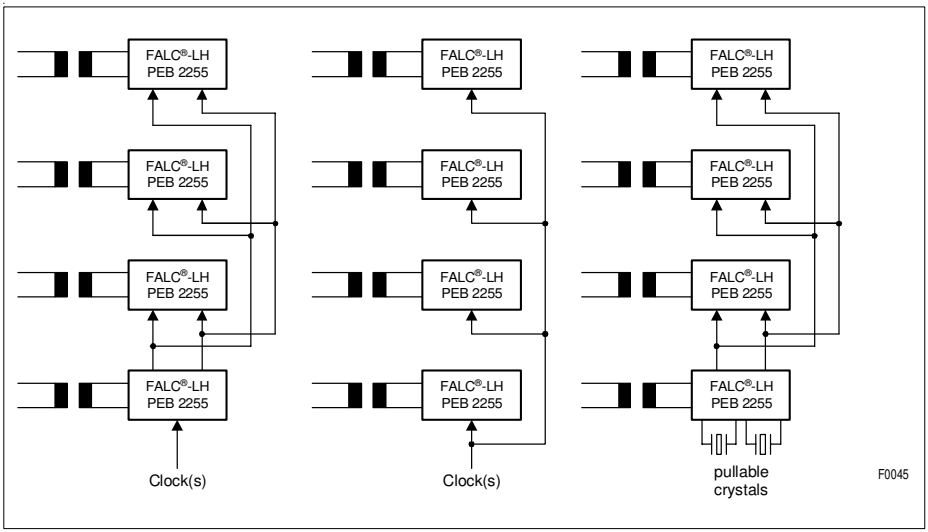

Figure 4 Multiple FALC Clocking Options

2 Pin Descriptions

2.1 Pin Diagram

(top view)

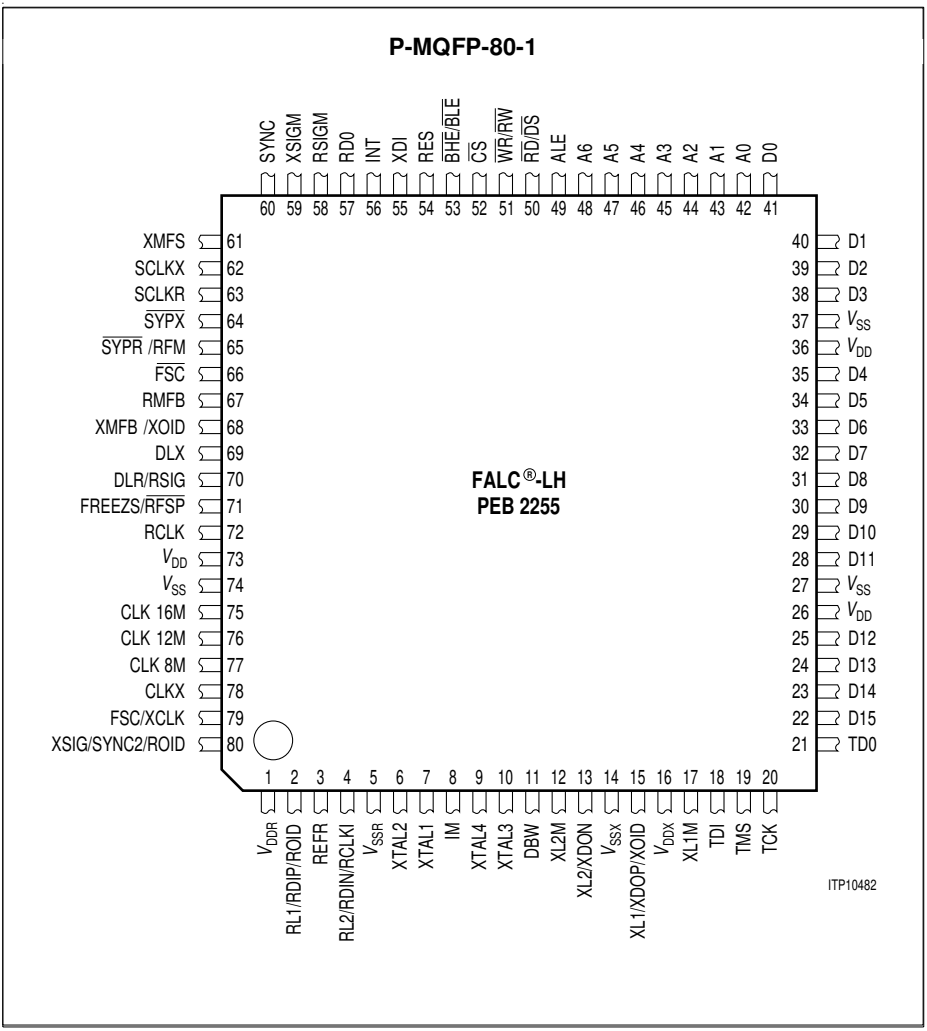

Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Pin Definitions - Microprocessor Interface

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
42...48	A0 … A6	I	**Address Bus** These inputs interface to seven bits of the system's address bus to select one of the internal registers for read or write.
41…38 35…28 25…22	D0…D3 D4…D11 D12..D15	I/O	**Data Bus** Bidirectional tristate data lines which interface to the system's data bus. Their configuration is controlled by the level of pin DBW: 8-bit mode (DBW = 0): D0 … D7 are active. D8 … D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. 16-bit mode (DBW = 1): D0 … D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is in high impedance state.
49	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A0 … A6 is internally latched with the falling edge of ALE. This function allows the FALC®-LH to be connected to a multiplexed address/data bus directly. In this case, pins A0 … A6 must be connected to the Data Bus pins externally. In case of demultiplexed mode this pin has to be connected to V_{DD} or V_{SS} directly.
52	$\overline{CS}$	I	**Chip Select** A low signal selects the FALC®-LH for read and write operations.