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FALC56

E1/T1/J1 Framer and Line
Interface Component for Long-
and Short-Haul Applications

PEB 2256 HT Version 1.2

PEB 2256 E Version 1.2

Wired
Communications



Never stop thinking.

Data Sheet

Revision History: **2002-08-27**

DS 3

Previous Version: DS 2

Page	Subjects (major changes since last revision)
479	P-LBGA-81-1 Package Outline

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Preface

The FALC56 framer and line interface component is designed to fulfill all required interfacing between an analog E1/T1/J1 line and the digital PCM system highway/H.100 bus.

The digital functions as well as the analog characteristics are configured via a flexible microprocessor interface.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1, Introduction**
Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- **Chapter 2, Pin Descriptions**
Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
- **Chapter 3 to Chapter 5, Functional Description E1/T1/J1**
These chapters describe the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation
- **Chapter 6 and Chapter 7, Operational Description E1/T1/J1**
Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).
- **Chapter 8, Signaling Controller Operating Modes**
Describes signaling controller functions for both E1 and T1/J1 operation.
- **Chapter 9 and Chapter 10, E1 Registers and T1/J1 Registers**
Gives a detailed description of all implemented registers and how to use them in different applications/configurations.
- **Chapter 11, Electrical Characteristics**
Specifies maximum ratings, DC and AC characteristics.
- **Chapter 12, Package Outlines**
Shows the mechanical values of the device packages.
- **Chapter 13, Appendix**
Gives an example for overvoltage protection and information about application notes and other support.
- **Chapter 14, Glossary**
- **Index**

Related Documentation

A detailed description of changes from version 1.1 to 1.2 is given in the "PEB 2256 Version 1.2 Delta Sheet".

This document refers to the following international standards
(in alphabetical/numerical order):

ANSI/EIA-656	ITU-T G.705
ANSI T1.102	ITU-T G.706
ANSI T1.403	ITU-T G.732
AT&T PUB 43802	ITU-T G.735
AT&T PUB 54016	ITU-T G.736
AT&T PUB 62411	ITU-T G.737
ESD Ass. Standard EOS/ESD-5.1-1993	ITU-T G.738
ETSI ETS 300 011	ITU-T G.739
ETIS ETS 300 166	ITU-T G.823
ETSI ETS 300 233	ITU-T G.824
ETSI ETS 300 324	ITU-T G.962
ETSI ETS 300 347	ITU-T G.963
ETSI TBR12	ITU-T G.964
ETSI TBR13	ITU-T I.431
FCC Part68	ITU-Q.703
GR-253-CORE	JT-G703
GR-499-CORE	JT-G704
GR-1089-CORE	JT-G706
H.100	JT-I431
H-MVIP	MIL-Std. 883D
IEEE 1149.1	TR-TSY-000009
ITU-T G.703	UL 1459
ITU-T G.704	

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Please provide in the subject of your e-mail:

device name (FALC56), device number (PEB 2256 HT), device version (Version 1.2),

and in the body of your e-mail:

document type (Data Sheet), issue date (2002-08-27) and document revision number (DS 3).

1 Introduction

The FALC56 framer and line interface component is designed to fulfill all required interfacing between analog E1/T1/J1 lines and the digital PCM system highway, H.100/H.110 or H-MVIP bus for world market telecommunication systems.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards. An integrated signaling controller including Signaling System #7 (SS7) support reduces software overhead.

Crystal-less jitter attenuation with only one master clock source reduces the amount of required external components.

Equipped with a flexible microprocessor interface, it connects to any control processor environment. A standard boundary scan interface is provided to support board level testing. Flat pack or BGA device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

Other members of the FALC[®] family are the FALC[®]54 for short-haul applications, the FALC[®]-LH for long-haul and short-haul applications as well as the QuadFALC supporting four channels on a single chip.

E1/T1/J1 Framer and Line Interface Component for Long- and Short-Haul Applications FALC56

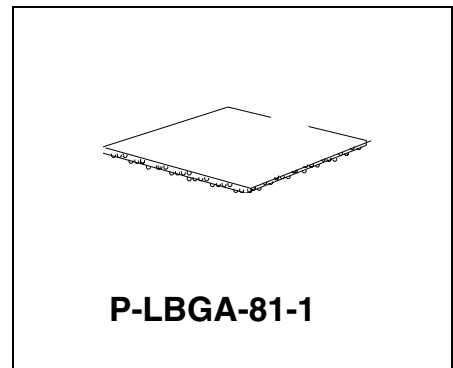
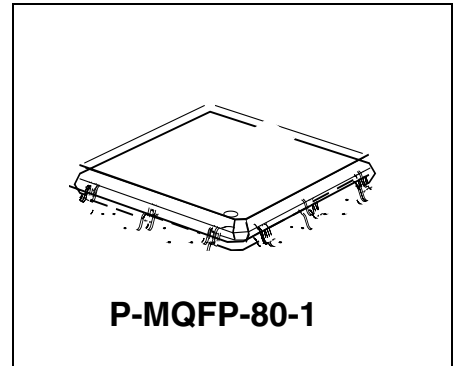
PEB 2256 HT

Version 1.2

1.1 Features

Line Interface

- High-density, generic interface for all E1/T1/J1 applications
- Analog receive and transmit circuits for long-haul and short-haul applications
- E1 or T1/J1 mode selectable
- Data and clock recovery using an integrated digital phase-locked loop
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1. 403 and FCC68: 0dB, -7.5dB, -15dB, -22.5 dB (T1/J1)
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Receive line monitor mode
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) are met
- Crystal-less wander and jitter attenuation/compensation
- Common master clock reference for E1 and T1/J1 (any frequency within 1.02 and 20 MHz)
- Power-down function



Type	Package
PEB 2256 HT	P-MQFP-80-1
PEB 2256 E	P-LBGA-81-1

- Support of automatic protection switching
- Dual-rail or single-rail digital inputs and outputs
- Unipolar NRZ or CMI for interfacing fiber-optical transmission routes
- Selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold
- Clock generator for jitter-free system/transmit clocks per channel
- Local loop and remote loop for diagnostic purposes
- Low power device, single power supply: 3.3 V with 5 V tolerant digital inputs

Frame Aligner

- Frame alignment/synthesis for 2048 kbit/s according to ITU-T G.704 (E1) and for 1544 kbit/s according to ITU-T G.704 and JT G.704 (T1/J1)
- Programmable frame formats:
 - E1: Doubleframe, CRC multiframe (E1)
 - T1: 4-frame multiframe (F4,FT), 12-frame multiframe (F12, D3/4), extended superframe (F24, ESF), remote switch mode (F72, SLC96)
- Selectable conditions for recover/loss of frame alignment
- CRC4 to non-CRC4 interworking according to ITU-T G. 706 Annex B (E1)
- Error checking via CRC4 procedures according to ITU-T G. 706 (E1)
- Error checking via CRC6 procedures according to ITU-T G. 706 and JT G.706 (T1/J1)
- Performs synchronization in ESF format according to NTT requirements (J1)
- Alarm and performance monitoring per second
 - 16 bit counter for CRC-errors, framing errors, code violations, error monitoring via E-bit and SA6-bit (E1), errored blocks, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS, remote/yellow alarm,...)
- Remote alarm generation/checking according to ITU JT-G.704 in ESF-format (J1)
- IDLE code insertion for selectable channels
- Single-bit defect insertion
- Flexible system clock frequency for receiver and transmitter
- Supports programmable system data rates with independent receive/transmit shifts:
 - E1: 2.048, 4.096, 8.192 and 16.384 Mbit/s (according to H.100/H.110 bus)
 - T1/J1: 2.048, 4.096, 8.192, 16.384 Mbit/s and 1.544, 3.088, 6.176, 12.352 Mbit/s
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Provides different time slot mapping modes
- Supports fractional E1 or T1/J1 access
- Flexible transparent modes
- Programmable in-band loop code detection and generation (TR62411)

- Channel loop back, line loop back or payload loop back capabilities (TR54016)
- Pseudo-random binary sequence generator and monitor (framed or unframed)
- Clear channel capabilities (T1/J1)
- Loop-timed mode

Signaling Controller

- Three HDLC controllers
Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- Supports signaling system #7
delimitation, alignment and error detection according to ITU-Q.703
processing of fill in signaling units, processing of errored signaling units
- CAS/CAS-BR controller with last look capability, enhanced CAS-register access and freeze signaling indication
- DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016 (T1/J1)
- DL-bit access for F72 (SLC96) format (T1/J1)
- Generates periodical performance report according to ANSI T1. 403
- Provides access to serial signaling data streams
- Multiframe synchronization and synthesis according to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in time slot 16)
- Transparent mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets
- Time slot assignment
Any combination of time slots selectable for data transfer independent of signaling mode (useful for fractional T1/J1 applications)
- Time-slot 0 S_a 8...4-bit handling via FIFOs (E1)
- HDLC access to any S_a -bit combination (E1)

Microprocessor Interface

- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Multiplexed and non-multiplexed address bus operations
- Hard/software reset options
- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

General

- Boundary scan standard IEEE 1149.1
- P-LBGA-81-1 package; body size 10 mm × 10 mm; ball pitch 1.0 mm or
- P-MQFP-80-1 package; body size 14 mm × 14 mm; lead pitch 0.5 mm
- Temperature range from -40 to +85 °C
- 3.3 V power supply, digital inputs 5V tolerant
- Typical power consumption 250 mW

Applications

- Wireless basestations
- E1/T1/J1 ATM gateways, multiplexer
- E1/T1/J1 **Channel & Data Service Units** (CSU, DSU)
- E1/T1/J1 Internet access equipment
- LAN/WAN router
- ISDN PRI, PABX
- **Digital Access Crossconnect Systems** (DACS)
- SONET/SDH add/drop multiplexer

1.2 Logic Symbol

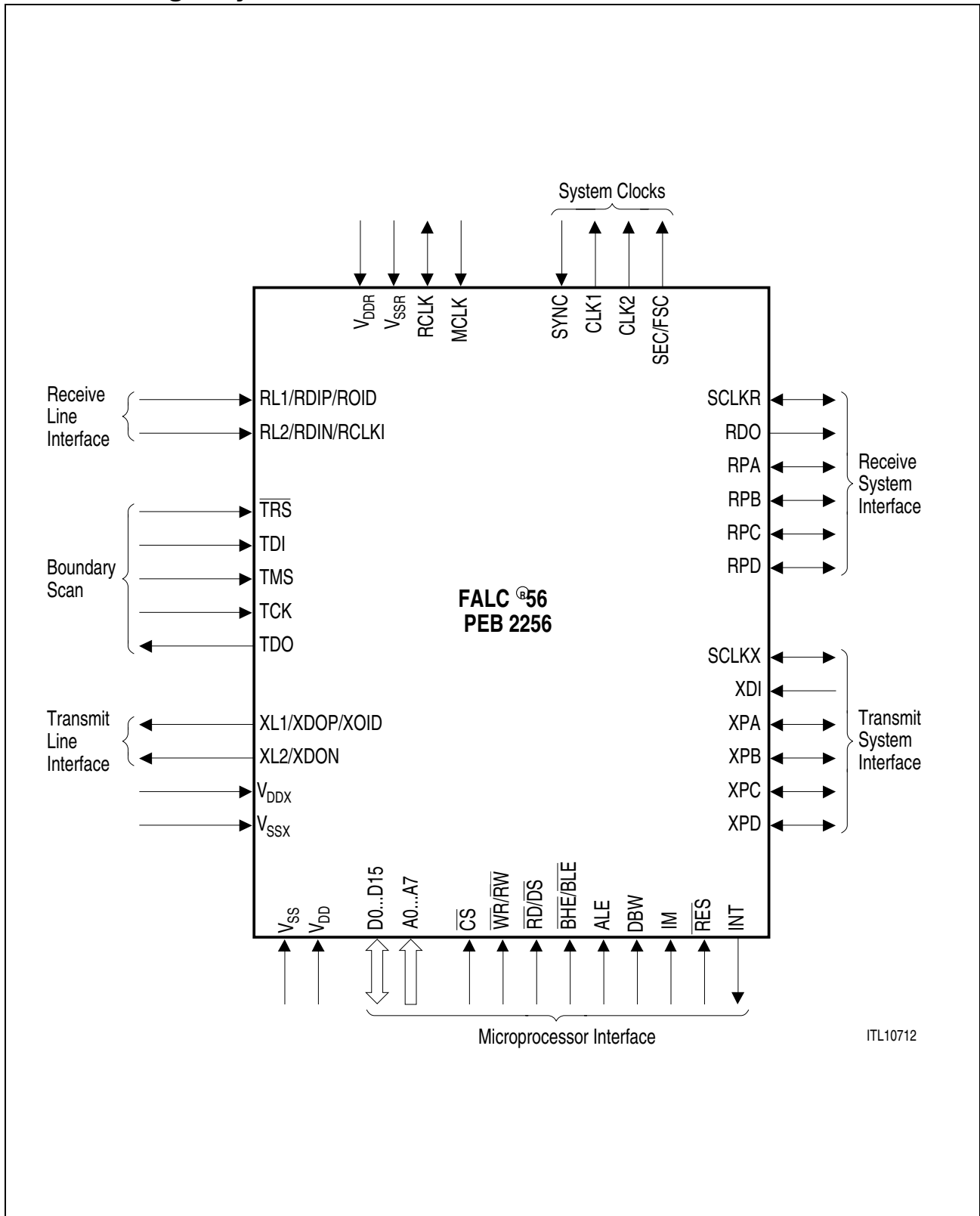


Figure 1 Logic Symbol

1.3 Typical Applications

The figures show a multiple link application for Frame Relay applications using the FALC[®]56 together with the 128-channel HDLC controller M128X and the Memory Timeswitch MTL5 as well as an 8-channel interface to the ATM layer.

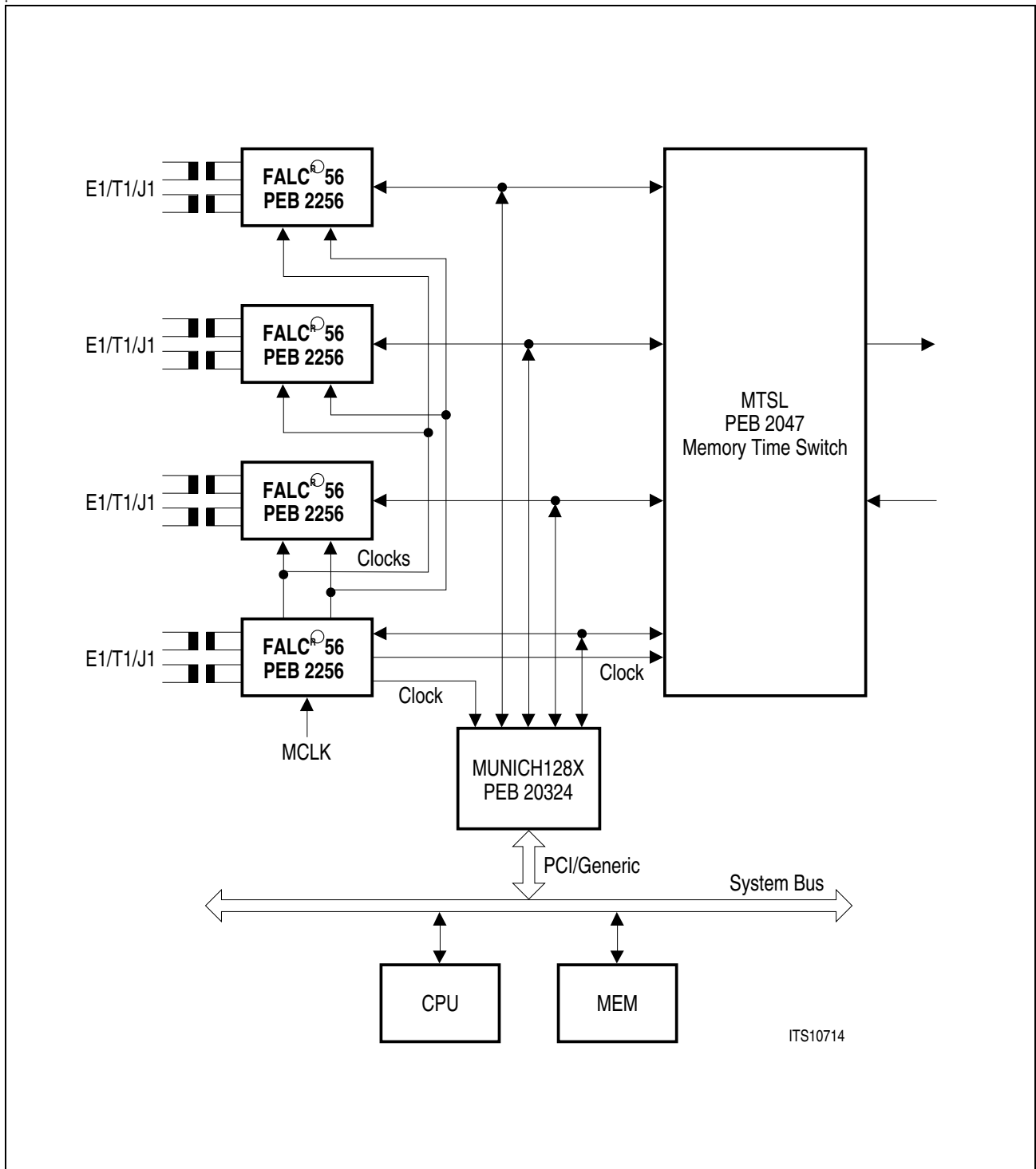


Figure 2 Multiple E1/T1/J1 Link over Frame Relay

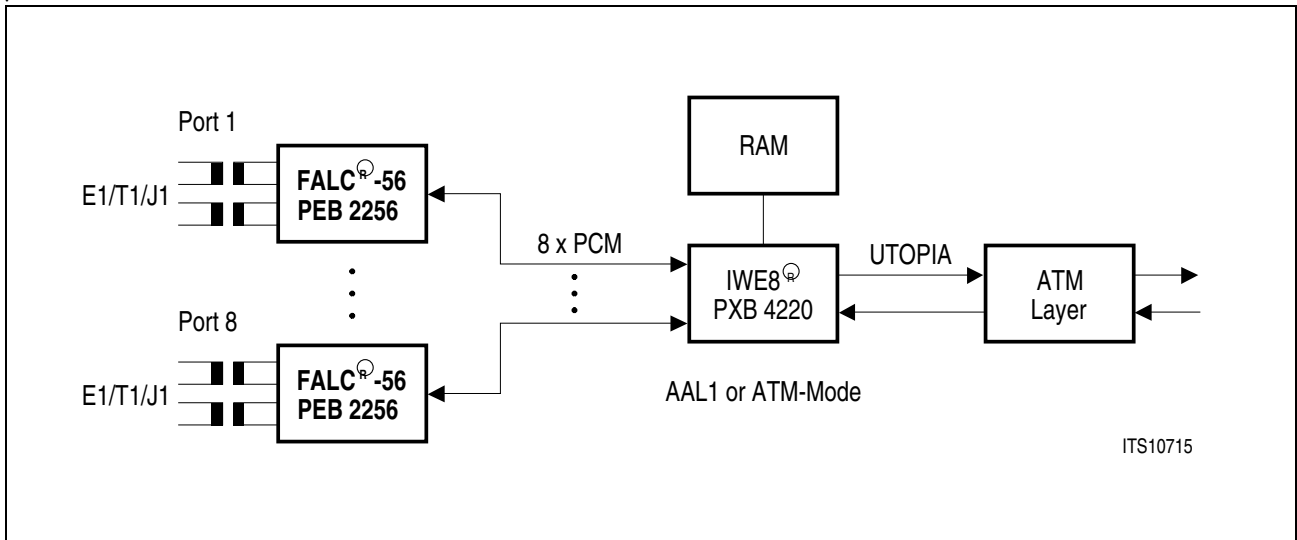


Figure 3 8-Channel E1/T1/J1-Interface to the ATM Layer