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Preliminary Data Sheet, DS 1, Nov. 2001

SWITI
Switching IC

PEF 20451 HTSI
PEF 20471 HTSI-L
PEF 24471 HTSI-XL
Version 1.3

Wired
Communications

Infineon
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Never stop thinking.

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Page	Content
20	**Table 6** updated
35	**Chapter 3.4.4** updated, added **Figure 14**
43	**Chapter 3.7.1** and **Chapter 3.7.2** updated
49	**Chapter 4.3** reworked
68	Description of Configuration Command Register 1 and 2 (**CMD1** and **CMD2**) updated
78	Description of Interrupt Status Register 1 (**ISTA1**) reworked
79	Description of Interrupt Error Status Register 1 and 2 (**IESTA1** and **IESTA2**) reworked
83	Description of Interrupt Error Mask Register (**INTEM2**) reworked
91	Description of Source Address (**SA**) and Destination Address (**DA**) Registers updated
97	**Chapter 6.2** reworked
112	**Chapter 6.8.3** reworked
128	**Chapter 7.1** and **Table 27** “PCM timing” updated
131	**Table 28** “PCM Parallel Mode Timing”
144	**Table 35** and **Figure 57** updated
146	Added **Chapter 7.8, “Hardware Reset Timing”**

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PRELIMINARY

PRELIMINARY

Preface

The Switching IC (SWITI) is a family of switching devices for a wide area of telecommunication and data communication applications. This document provides complete reference information according to chip interfaces, programming, internal architecture and applications.

Organization of this Document

This Preliminary Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and of the SWITI family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Description**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Architectural Description**
  Rough overview of the internal architecture and clock fallback feature.

- **Chapter 4, Description of Interfaces**
  Short introduction of used interfaces.

- **Chapter 5, Register Description**
  Gives information about all registers accessible via the microprocessor interface according to address, short name, access, reset value and value range.

- **Chapter 6, Programming the Device**
  Gives a variety of examples how to programm the device, lists all available command and parameter values.

- **Chapter 7, Timing Diagrams**
  Contains timing diagrams.

- **Chapter 8, Electrical Characteristics**
  Specification of the electrical parameters.

- **Chapter 9, Package Outlines**
  Outlines of the available packages (P-BGA-217-1).

PRELIMINARY

Table 1 Who should read what?

Addressed Person	Relevant Chapters
Programmer	3, 5, 6
Board Designer	2, 3, 4, 7, 8, 9

Related Documentation

H.100 Hardware Compatibility Specification: CT Bus, revision 1.0

H.110 Hardware Compatibility Specification: CT Bus, revision 1.0

PCI Specification, revision 2.1, PCI special interest group

Compact PCI Specification - PICMG 2.0, revision 2.1

Compact PCI Hot Swap Specification - PICMG 2.1, revision 1.0

H-MVIP Standard, Release 1.1a, GO-MVIP Inc., January 1997

MVIP-90 Standard, Release 1.1, GO-MVIP Inc., October 1994

SC-Bus Specification, ANSI/VITA 6-1994

1 Overview

The new switching family, called SWITI, provides a complete and cost-effective solution for all switching systems. The family is divided in two sub-families, the MTSI family and the HTSI family. The Preliminary Data Sheet describes the functionality and characteristic of the HTSI devices.

The devices can be used in today's switching applications, e.g. conventional PBXs and central offices (CO's), as well as in H.100/H.110 applications (only the HTSI family), which are the key to high performing CTI- and Voice-over-IP-applications, one of the most important future technologies in telecommunications.

The main requirements of today's switching applications are met by the following features:

- Constant delay e.g. to support wide band data switching, or channel bundling
- Bit switching/subchannel switching to support applications such as mobile base stations, DECT, computer telephony

In addition, the SWITI family provides new features to ensure a broad range of configurations to make it possible to adapt the device to all switching applications:

- A compliant H.100/H.110 interface (HTSI)
- 8-channel stream-to-stream switching capability (HTSI)
- Message mode, which allows to assign a preset value to any output time-slot
- GPIO (General Purpose I/O) port, which is controlled from the external µP

SWITI family. The SWITI family consists of 6 ICs with different switching capacities. The possible configurations are shown in **Table 2**. The HTSI versions provide an additional H.100 / H.110 interface, while the MTSIs are standard switching devices. All devices can be programmed easily, thus helping the designer/programmer to integrate the device into his application comfortably.

Table 2 SWITI Family Tree

Name	Package	Sales code	Connec-tions	Local bus IN/OUT	H-Bus I/O
HTSI-XL (H-Mode)	P-BGA-217-1	PEF24471 HTSI-XL	2048	16/16	32
HTSI-XL (M-Mode)		PEF24471 HTSI-XL		32/32	-
HTSI-L (H-Mode)	P-BGA-217-1	PEF20471 HTSI-L	1024	16/16	32
HTSI-L (M-Mode)		PEF20471 HTSI-L		32/32	-

Table 2 SWITI Family Tree (cont'd)

Name	Package	Sales code	Connec-tions	Local bus IN/OUT	H-Bus I/O
HTSI (H-Mode)	P-BGA-217-1	PEF20451 HTSI	512	16/16	32
HTSI (M-Mode)		PEF20451 HTSI		32/32	-
MTSI-XL	P-MQFP-100-2	PEF24470 MTSI-XL	2048	16/16	-
MTSI-L	P-MQFP-100-2	PEF20470 MTSI-L	1024	16/16	-
MTSI	P-MQFP-100-2	PEF20450 MTSI	512	16/16	-

HTSI devices.

The HTSI devices can be operated in two different modes, H-Mode and M-Mode.

In H-Mode the device offers 16 local I/Os and additionally a compliant H.100/H.110 interface (32 bidirectional I/Os). The complete number of available connections can be assigned as H-bus to H-bus, local bus to local bus connection, or mixed.

In M-Mode all lines are configured as local I/Os, so that in total 32 local I/Os are provided. Thus e.g. the HTSI-XL device can be used as 2K non-blocking switch operating with all 32 I/Os at 4.096 Mbit/s.

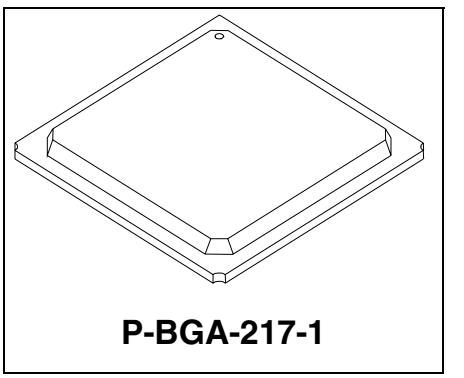
PRELIMINARY

Switching IC SWITI

PEF 20451 / 20471 / 24471

Version 1.3 **CMOS**

1.1 Overview of Features



P-BGA-217-1

General

- Switching capacity of 512, 1024, or up to 2048 connections of different types between different buses
- Programmable data rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s on per stream basis
- Constant delay or minimum delay programmable on per connection basis
- Subchannel switching ability of 1-bit, 2-bit, 4-bit wide time-slots
- Programmable clock shift for local bus
- 8-channel stream-to-stream switching for H.100/H.110 and interoperability bus
- Automatic data rate adaption
- Optional 8-bit parallel input and/or 8-bit parallel output for first 8 lines of local bus
- Broadcast capabilities
- Multipoint switching ability
- Read and write access to all time-slots
- Message mode (time-slot write access)
- Programmable framing group
- GPIO port
- 8-bit µP-interface supports both Intel and Motorola mode
- Optional 16-bit µP interface mode (instead of GPIO port)
- On chip PLL for H.100/H.110, SCbus, MVIP, MVIP-H clock operation (master/slave) and for local bus clock operation (master/slave)
- JTAG interface
  - Boundary scan according to IEEE 1149.1
- 3.3 V power supply
- 5 V tolerant inputs/outputs

Type	Package
PEF 20451 / 20471 / 24471	P-BGA-217-1

HTSI in H-Mode

- H.100/H.110 compliant interface with all mandatory signals
- Local bus of up to 16 PCM ports (16 In/16 Out)
- Hot swapping

HTSI in M-Mode

- Local bus of up to 32 PCM ports (32 In/32 Out).

1.2 Features in Detail

Flexible Data Rates

Each input and each output line of the local bus is programmable to operate at different data rates. The possible data rates are 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s. Even for the HTSI in M-Mode all of the 32 input lines and 32 output lines are configureable, except for the bit rate of 16.384 Mbit/s.

In case of 16.384 Mbit/s only 24 lines can be used.

The possible data rate for the data lines of the H-Bus are 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Constant and Minimum Delay

Each connection independent of the addressed buses can be determined to be a constant delay or minimum delay connection. Constant delay means that any input time-slot or subchannel is available on the programmed output after 2 frames. Minimum delay means that the time-slot or subchannel appears at the output as soon as possible. The minimum delay depends on the chosen connections and the possible range is between 0 and 2 frames.

Subchannel Switching

Each connection can be a 1-bit, 2-bit, 4-bit, or 8-bit connection. Subchannel switching is applicable to both the local bus and the H-Bus and has a constant delay of 2 frames. Sub-Channel switching is supported only for data rate of 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Programmable Clock Shift

The position of time-slot 0 of each local bus input line can be programmed within the time-slot before and after the PFS rising edge in half clock steps. Also the position of time-slot 0 of all local bus output lines can be programmed within the first time-slot after the PFS rising edge.

8-Channel Stream-to-Stream Switching

This feature offers the possibility to efficiently switch one data stream to another at the same or different data rates without occupying switching memory capacity. It mainly supports interoperability between CT-bus (Computer Telephony) devices such as SCbus and MVIP-90 running at different data rates. It is possible to use up to 8 lines from the H.1x0 data lines to establish the connections. Input and output frequency can be configured differently.

Automatic Data Rate Adaption

Connections are also possible between lines operating at different data rates. The programmer just specifies input and output line, time-slot, and if necessary, the subchannel.

Parallel Mode

The first 8 local bus input and output lines can be configured to one parallel input or output port respectively. In serial mode a time-slot is determined by 8 consecutive data clock cycles according to each line. In parallel mode a time-slot is determined by 1 data clock cycle according to the first 8 lines.

Broadcast

With this feature it is possible to distribute one incoming time-slot to different output time-slots.

Multipoint

Multipoint connections can be seen as the opposite of broadcast connections. Here it is possible to generate one output time-slot consisting of several input time-slots. The specified input time-slots are logically AND or OR connected (selectable) and have a constant delay of 2 frames.

Read Access

The programmer has access to any input time-slot. After issuing an appropriate command the arrival of the time-slot will be reported by interrupt. The value can be read from a dedicated register. For every read request the command has to be issued again.

Message Mode (Write Access)

This feature allows a constant value to be sent to any given output time-slot.

Framing Group

It is possible to specify up to 8 different framing signals of 8 kHz. The position of the rising edge and the pulse width can be programmed for each signal. The reference frame is determined by the PFS signal. The pulse parameters are programmed in half step resolution according to a 16.384 MHz clock.

General Purpose Clocks

All 8 GPCLK lines can be configured as individual clock outputs with 8 kHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz and for test purposes with the internal frequency or the input frequency of the analog PLL (APLL).

GPIO Port

Each line of the general purpose input/output port can be configured to be either input or output. According to an input an edge causes an interrupt. The outputs can be influenced by write access via the microprocessor interface. Thus the user has the possibility to observe and influence additional signals for his application.

Microprocessor Interface

All devices provide a standard 8-bit microprocessor interface operating in either Intel or Motorola mode. Optionally it is possible to configure the GPIO port as additional data lines to provide a 16-bit microprocessor interface. The use of the 16-bit µP interface reduces the number of write cycles required to configure a connection from 7 (in case of 8-bit µP interface) to 3 write cycles.

Input/Output Tolerance

The HTSI can be used in a 5 V environment with two additional 5 V (VDD) power supply pins. Local input and outputs are 3.3 V and 5 V tolerant. The outputs have TTL level driving capability. The H-Bus lines of the HTSI can be used in a 3.3 V signaling PCI environment.

1.3 Logic Symbol

The HTSI is dedicated to perform time-slot switching between the local bus and the H-Bus or to offer a solution for applications with a high number of local I/Os. The HTSI operates in two modes. In H-Mode (**Figure 1**) it works with the H-Bus and in M-Mode (**Figure 2**) it operates without the H-Bus.
The HTSI in H-Mode provides 16 PCM input lines and 16 PCM output lines and the complete H-Bus with 32 bidirectional H.100/H.110 data lines.

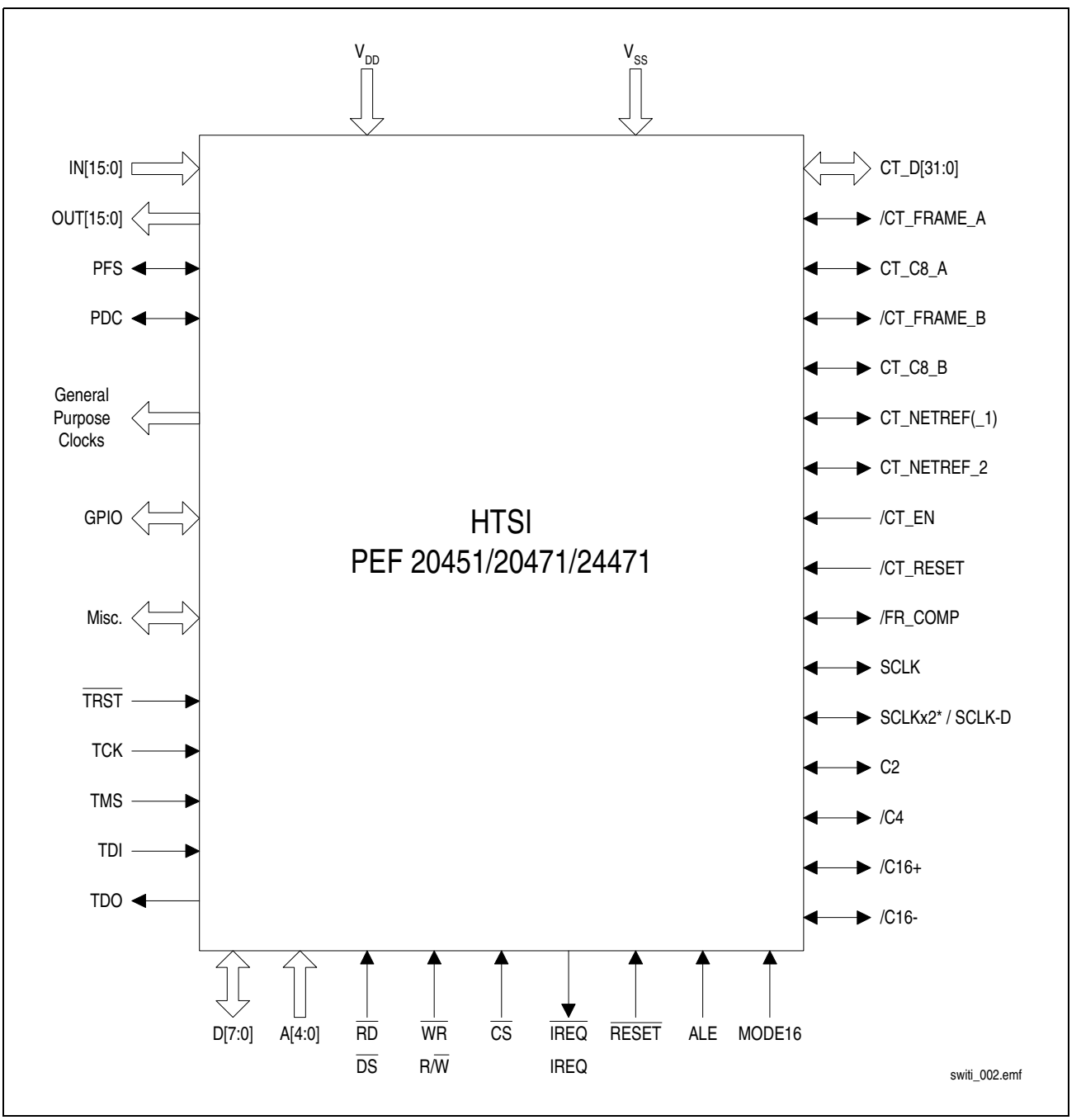


Figure 1 Logic Symbol: HTSI in H-Mode

If no H-Bus is needed it is possible to configure the HTSI in M-Mode. In this mode, the HTSI provides 32 PCM input lines and 32 PCM output lines.

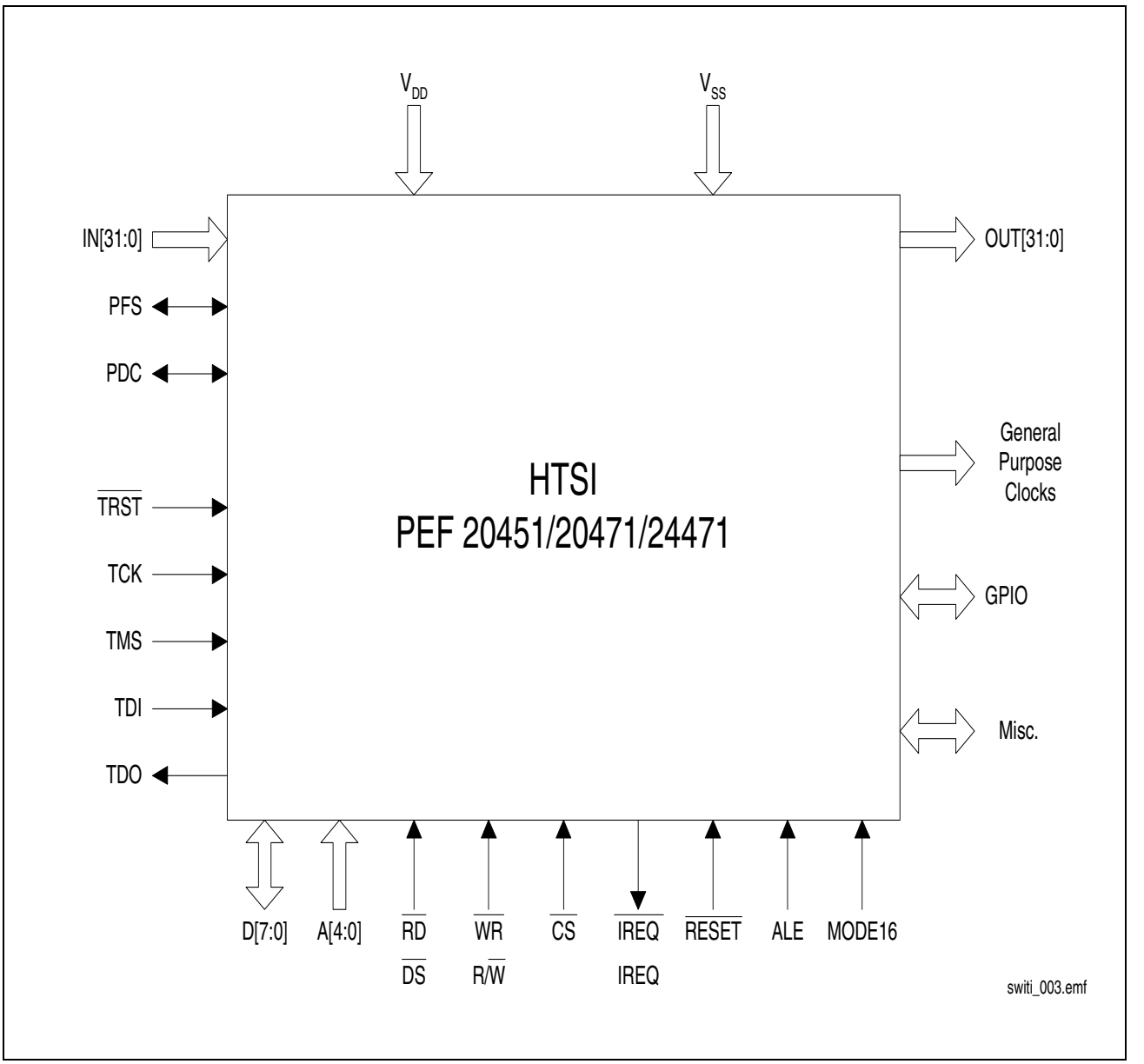


Figure 2 Logic Symbol: HTSI in M-Mode

1.4 Typical Applications

Typical applications of the SWITI family are:

- PCM switch, concentrator or multiplexer in PBXs, COs or mobile base stations
- H.100/H.110 interface in
  - Computer telephony systems
  - Internet telephony systems
  - LAN/WAN access devices
  - Enhanced service platforms

The following sections give a general overview of the system integration of the SWITI family.

1.4.1 Standard PBX or CO Application

The MTSI or the HTSI in M-Mode can be used, just as the MTSC or MTSL, in standard private branch exchange or central office applications (**Figure 3**), e.g. in the switching network.

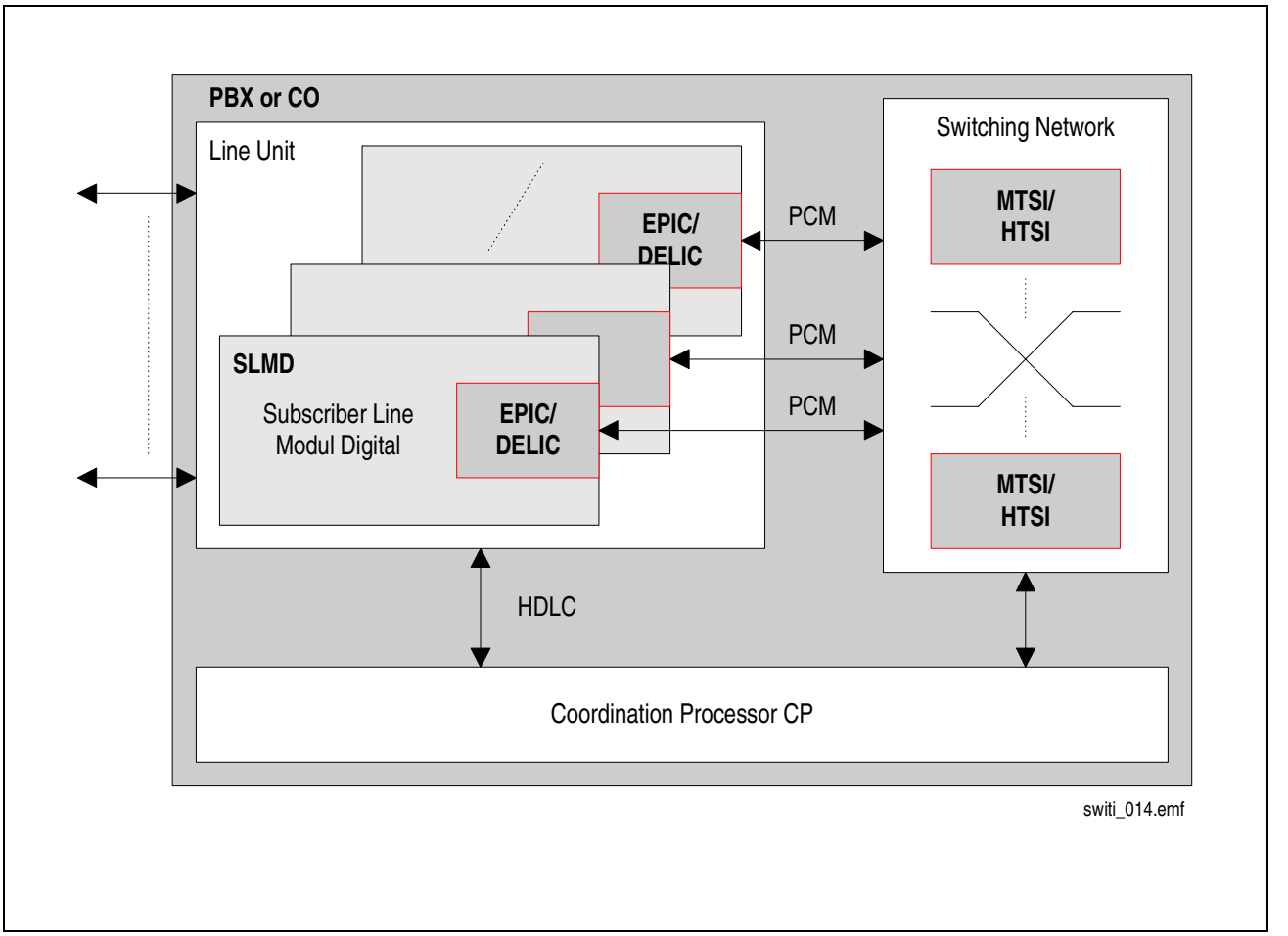


Figure 3 Standard PBX or CO Application

1.4.2 Computer Telephony Application

In Computer Telephony Integration (CTI) applications, resources such as the analog telephone line cards, ISDN ports, switching controllers, FAX firmware, or voice processing modules are in the form of plug-in cards that sit on the ISA or PCI slots of a PC. Resource sharing is established by connecting the top of the plug-in cards with cables. This Time Division Multiplex (TDM) bus has evolved from the original H-MVIP, MVIP-90, Dialogic's SC-Bus, into the latest H.100/H.110 bus or H-Bus developed by the Enterprise Computer Telephony Forum (ECTF). By connecting to the H.100/H.110 interface devices, system modules may send and receive data to and from any one of the 4096 TDM time-slots of the H-Bus. The H-Bus also offers the ideal solution for routers to provide a bridge between the data communication and telecommunication system modules.

In Computer Telephony (CT) environment, resource sharing is accomplished by passing data back and forth through the H.100/H.110 bus. **Figure 4** shows the example.

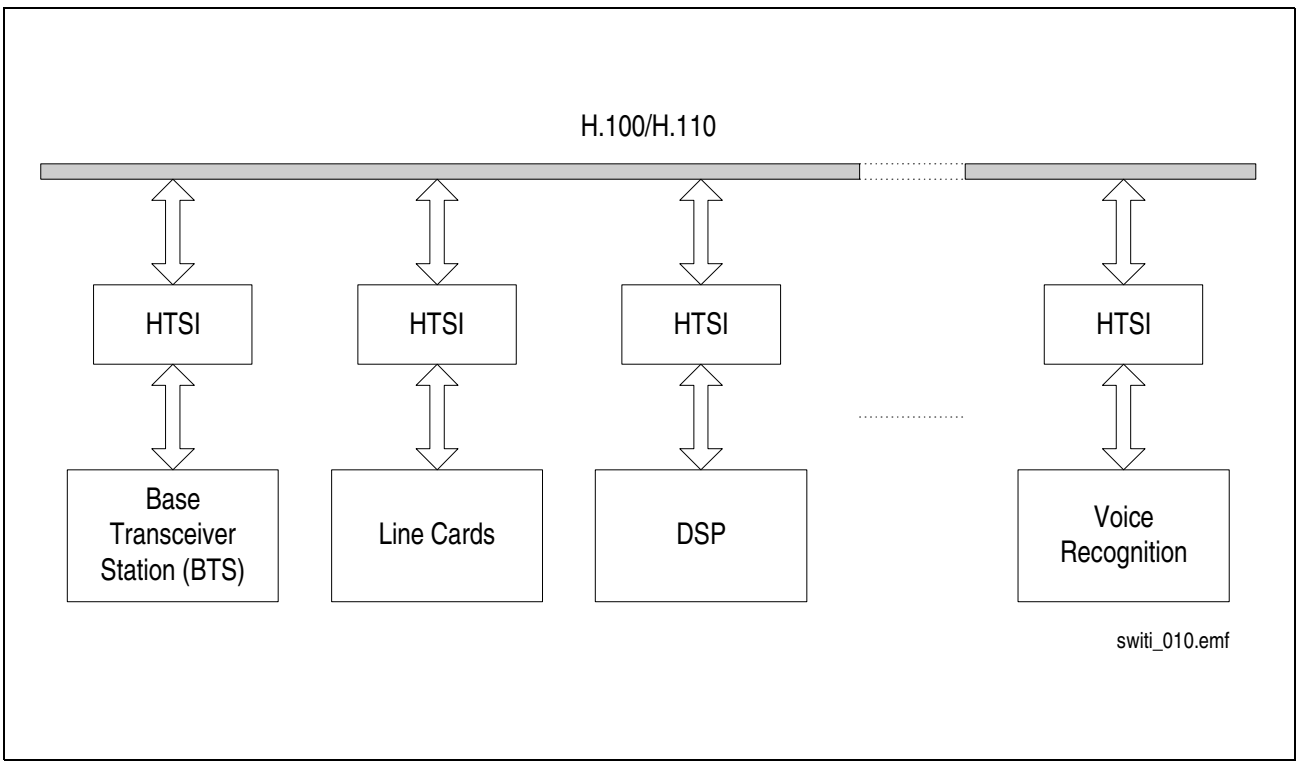


Figure 4 CT Application

1.4.3 Router / Remote Access Application

The HTSI (H-Mode) or also the MTSI (if no H-Bus interface is used in the system) is used in multivoice applications as the bridge connecting the data communication modules to the telecommunication modules in a router/remote access design. **Figure 5** shows the example.

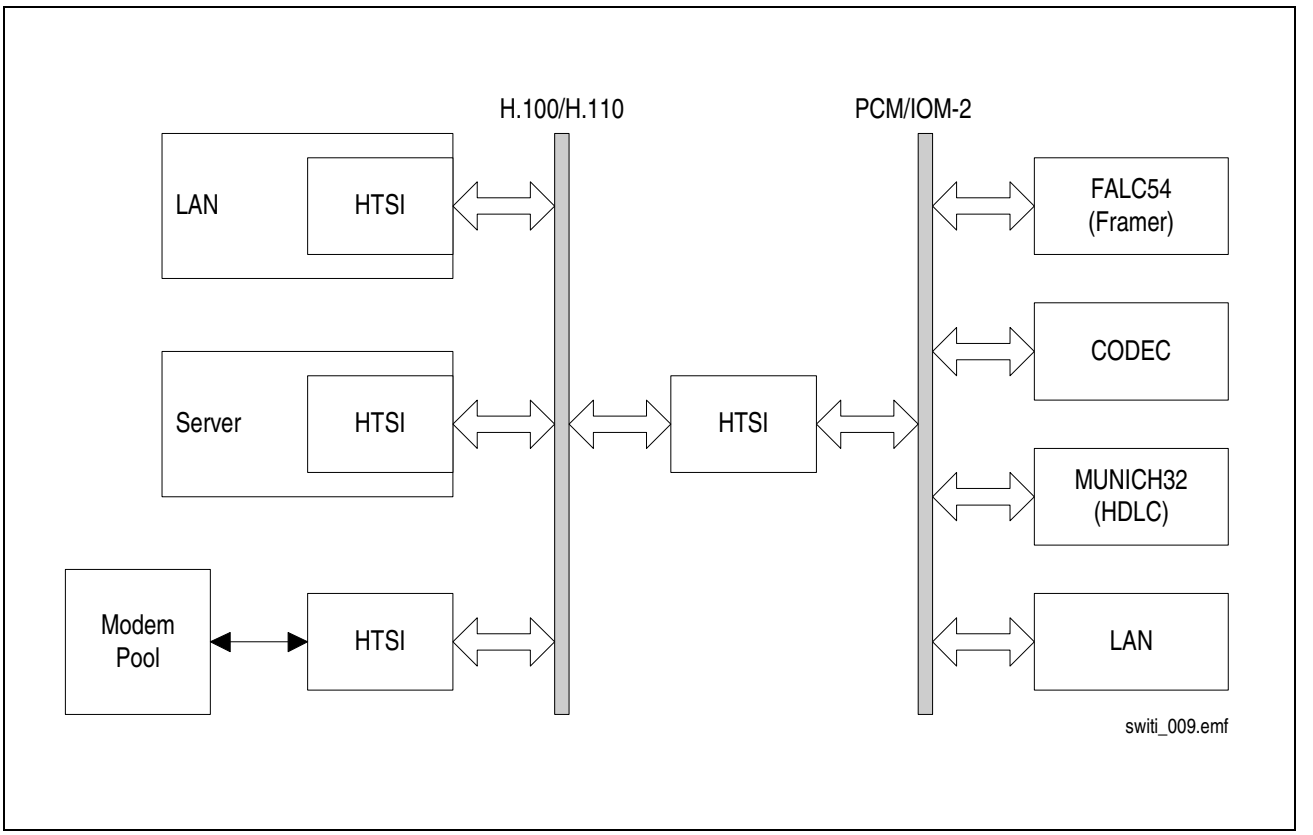


Figure 5 Router / Remote Access Applications

1.4.4 Voice over IP Application

In a voice over IP application (**Figure 6**) the HTSI (in H-Mode) may be used to connect a conventional PBX to the H-Bus. A Vocoder card, also connected to the H-Bus, performs speech compression and decompression whereas an Ethernet card transmits and receives the compressed data over the network.

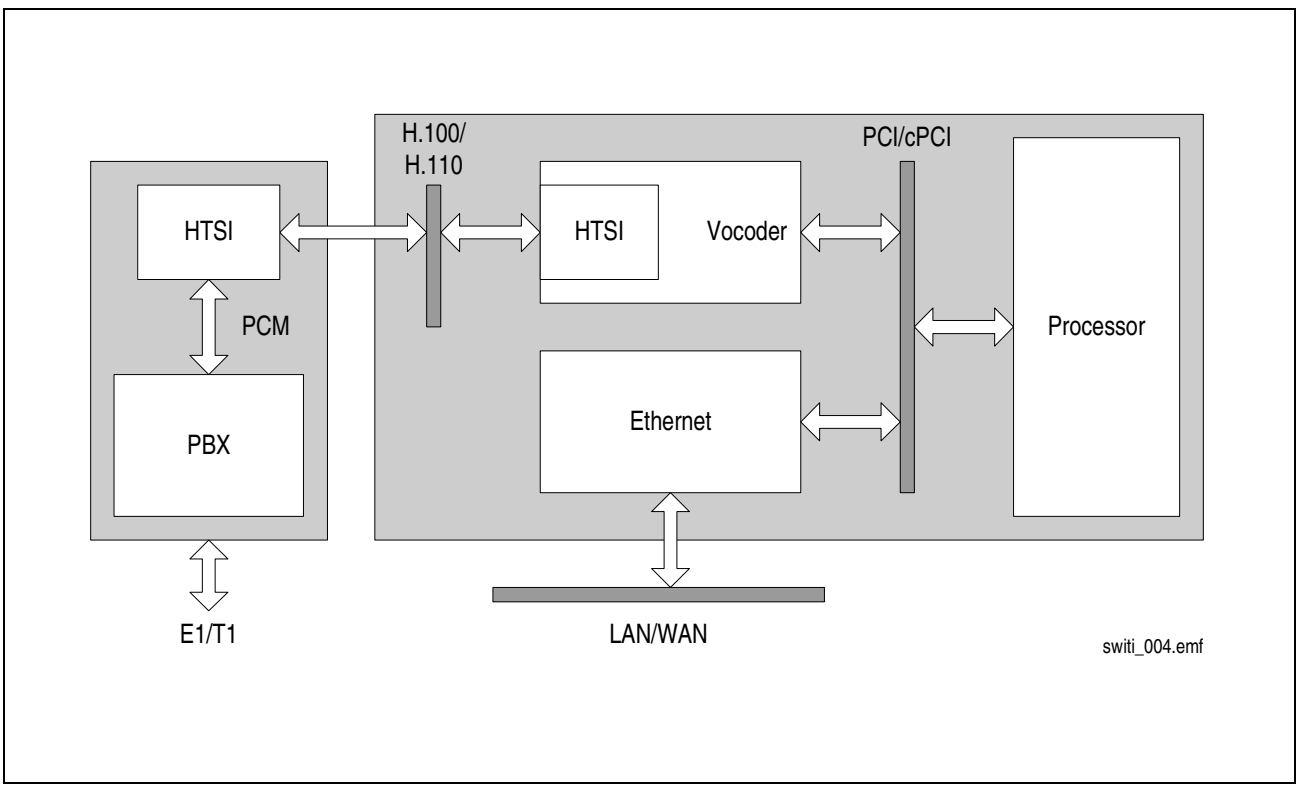


Figure 6 Voice over IP Application