



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



SWITCHING IC

PEF 20451 HTSI
PEF 20471 HTSI-L
PEF 24471 HTSI-XL
Version 1.3

Wired
Communications



Never stop thinking.

Edition 2001-11-16

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**

**© Infineon Technologies AG 2001.
All Rights Reserved.**

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

SWITI

Switching IC

PEF 20451 HTSI

PEF 20471 HTSI-L

PEF 24471 HTSI-XL

Version 1.3

Wired

Communications



Table of Contents		Page
1	Overview	3
1.1	Overview of Features	5
1.2	Features in Detail	6
1.3	Logic Symbol	9
1.4	Typical Applications	11
1.4.1	Standard PBX or CO Application	11
1.4.2	Computer Telephony Application	12
1.4.3	Router / Remote Access Application	13
1.4.4	Voice over IP Application	14
2	Pin Description	15
2.1	Pin Diagram	15
2.2	Pin Definitions and Functions	16
2.2.1	H-Bus Interface	16
2.2.2	Local Bus Interface (PCM)	19
2.2.3	General Purpose Port	19
2.2.4	Clock Signals	20
2.2.5	JTAG Interface	20
2.2.6	Microprocessor Interface	21
2.2.7	Power Supply	22
3	Architectural Description	23
3.1	Functional Block Diagram	23
3.2	Overview of Functional Blocks	24
3.3	Switching Factory	25
3.3.1	Switching Modes	25
3.3.1.1	Minimum and Constant Delay	25
3.3.1.2	Subchannel Switching	25
3.3.1.3	Multipoint Switching	25
3.3.1.4	Broadcast Switching	26
3.3.1.5	Bidirectional Switching	26
3.3.1.6	Stream-to-Stream Switching	27
3.3.1.7	Message Mode	29
3.3.2	Parallel Mode for Local Bus	29
3.3.3	Switching Block Error Handling	30
3.3.4	Analyze Connection and Data Memory	30
3.4	Clock Generator and PLL	31
3.4.1	General Overview	31
3.4.2	Analog PLL (APLL)	32
3.4.2.1	Functional Description	33
3.4.2.2	Jitter-Transfer-Function	34
3.4.3	Master-Slave Selection	35
3.4.4	Phase Alignment	35
3.4.5	PLL Synchronization	36

Table of Contents		Page
3.4.5.1	PLL Synchronization H-Mode	36
3.4.5.2	PLL Synchronization M-Mode	37
3.4.6	PLL Error Handling	37
3.4.7	Clock Fallback	37
3.4.7.1	Clock Signal Monitoring	38
3.4.7.2	Clock Fallback Mechanism	39
3.5	Loops	42
3.6	Read SWITL Configuration with Indirect Register Addressing	42
3.7	Power-On and Reset Behavior	43
3.7.1	Hardware Reset	43
3.7.2	Software Reset	43
4	Description of Interfaces	44
4.1	Local Bus Interface (PCM)	44
4.2	H-Bus Interface	46
4.2.1	CT_C8(A/B) and $\overline{\text{CT_FRAME}}(A/B)$	47
4.2.2	Dataports	47
4.2.3	$\overline{\text{CT_EN}}$	48
4.2.4	$\overline{\text{CT_RESET}}$	48
4.2.5	H-MVIP C16 Signals	48
4.3	Data Rate	49
4.4	Microprocessor Interface	50
4.4.1	Intel/Siemens or Motorola Mode	50
4.4.2	De-multiplexed or Multiplexed Mode	50
4.5	General Purpose Port (GPIO)	52
4.6	General Purpose Clocks	53
4.6.1	Frame Group Outputs	53
4.6.2	GPCLK as Clock Outputs	53
4.7	JTAG (Boundary Scan)	54
4.7.1	Boundary Scan	54
4.7.2	Test-Access-Port (TAP)	54
4.7.3	TAP Controller	55
4.8	Identification Code via μP Read Access	57
5	Register Description	58
5.1	Register Overview For 8-Bit Interface	59
5.2	Detailed Register Description For 8-bit Interface	61
5.3	Register Overview For 16-Bit Interface	90
5.4	Detailed Register Description For 16-Bit Interface	91
6	Programming the Device	95
6.1	Read and Write Access	96
6.2	Interrupt Handling	97
6.3	Command and Register Overview	99

Table of Contents		Page
6.4	Indirect Configuration Register Access	106
6.5	Initialization Procedure	107
6.6	H.1x0 Clocking Unit	108
6.7	PCM Clocking Unit	110
6.8	H.1x0/PCM Line Interface	110
6.8.1	Standby Command	110
6.8.2	Determining Clock Rates	111
6.8.3	Performing Bit Shifting	112
6.8.3.1	Input Bit Shifting	112
6.8.3.2	Output Bit Shifting	113
6.9	Global Clock Signals	114
6.9.1	Framing Groups	114
6.10	Read Time-Slot Value	115
6.11	Establish Connections	116
6.11.1	Establish 8-bit Connections	116
6.11.2	Subchannel Switching	117
6.11.2.1	Establish 4-bit Connections	117
6.11.2.2	Establish 2-bit Connections	118
6.11.2.3	Establish 1-bit Connections	119
6.11.3	Establish Broadcast Connections	120
6.11.4	Establish Subchannel Broadcast Connection	121
6.11.5	Establish Multipoint Connection	122
6.12	Send Messages	123
6.13	Release Connections	124
6.13.1	Release 8-bit Connections	124
6.13.2	Release 4-bit Connections	124
6.13.3	Release 2-bit Connections	124
6.13.4	Release 1-bit Connections	125
6.13.5	Release Broadcast Connection	126
6.13.6	Release Subchannel Broadcast Connection	126
6.13.7	Release Multipoint Connection	127
6.14	Stop Sending Messages	127
7	Timing Diagrams	128
7.1	PCM Interface Timing	128
7.2	PCM Parallel Mode Timing	131
7.3	H-Bus and PCM (Local Bus) Frame Structure	132
7.4	H-Bus Timing	134
7.5	Clock Interoperability	137
7.6	Microprocessor Interface Timing	138
7.6.1	Infineon/Intel Timing in De-Multiplexed Mode	138
7.6.2	Infineon/Intel Timing in Multiplexed Mode	139
7.6.3	Motorola Microprocessor Timing	142

Table of Contents		Page
7.7	JTAG Interface Timing	144
7.8	Hardware Reset Timing	146
8	Electrical Characteristics	147
8.1	Absolute Maximum Ratings	147
8.2	Operating Range	148
8.3	Crystal Oscillator	149
8.4	DC Characteristics	150
8.5	Capacitances	151
8.6	AC Characteristics	151
9	Package Outlines	152

List of Figures		Page
Figure 1	Logic Symbol: HTSI in H-Mode	9
Figure 2	Logic Symbol: HTSI in M-Mode	10
Figure 3	Standard PBX or CO Application	11
Figure 4	CT Application	12
Figure 5	Router / Remote Access Applications	13
Figure 6	Voice over IP Application	14
Figure 7	Pin Configuration	15
Figure 8	Block Diagram	23
Figure 9	Bidirectional Mode	27
Figure 10	Example for Stream-to-Stream Switching	29
Figure 11	SWITI Clock Generator	31
Figure 12	Block Diagram of APLL	33
Figure 13	APLL - Jitter Transfer Function	34
Figure 14	Example of Phase Alignment.	35
Figure 15	Clock Fallback of Primary Master	39
Figure 16	Clock Fallback of Secondary Master	40
Figure 17	Clock Fallback of Slave	41
Figure 18	PCM Interface Configurations	44
Figure 19	PCM Bit Shifting.	45
Figure 20	H-Bus Interface in H.100 Mode	46
Figure 21	H-Bus Interface in H.110 Mode	47
Figure 22	Multiplexed and in De-multiplexed Bus Mode	51
Figure 23	GPIO Port Configuration Example	52
Figure 24	Frame Signal Example.	53
Figure 25	Order of Register Access.	95
Figure 26	8-bit μ P Access Interrupt Structure	97
Figure 27	16-bit μ P Access Interrupt Structure	98
Figure 28	Initialization Procedure after Reset	107
Figure 29	H.100 Master and Slave Configuration Process	109
Figure 30	Example: Input Bit Shifting.	112
Figure 31	Example: Output Bit Shifting	113
Figure 32	Example Framing Groups	114
Figure 33	Example: 8-bit Connection.	116
Figure 34	Subchannel Address in Time-Slot	117
Figure 35	Example: 4-bit Connection.	117
Figure 36	Example: 2-bit Connection.	118
Figure 37	Example: 1-bit Connection.	119
Figure 38	Example: Broadcast Connection	120
Figure 39	Example: Subchannel Broadcast Connection	121
Figure 40	Example: Multipoint Connection	122
Figure 41	Example: Send Message	123
Figure 42	PCM Timing	128
Figure 43	Parallel Mode Timing	131

List of Figures	Page
Figure 44 H-Bus and PCM (Local Bus) Clock Alignment	132
Figure 45 H-Bus Frame Structure	133
Figure 46 H.1x0 Detailed Functional Timing	133
Figure 47 H.1x0 Functional Timing for 8, 4 and 2 MBit/s Data Streams	133
Figure 48 Detailed Data Bus Timing	134
Figure 49 Clock Skew Timing	136
Figure 50 SCLK-D Timing for SCbus Operating at 8.192 Mbit/s	137
Figure 51 Infineon/Intel Read Cycle in De-Multiplexed Mode	139
Figure 52 Infineon/Intel Write Cycle in De-Multiplexed Mode	139
Figure 53 Infineon/Intel Read Cycle in Multiplexed Mode	140
Figure 54 Infineon/Intel Write Cycle in Multiplexed Mode	141
Figure 55 Motorola Read Cycle	143
Figure 56 Motorola Write Cycle	143
Figure 57 Boundary Scan Timing	145
Figure 58 Hardware Reset Timing	146
Figure 59 External Crystal	149
Figure 60 I/O Wave Form for AC-Test	151
Figure 61 Outlines of P-BGA-217-1	152

PRELIMINARY

Table 1	Who should read what?	2
Table 2	SWITI Family Tree	3
Table 3	H.100/H.110 Bus Interface (H-mode only)	16
Table 4	Local Bus Interface	19
Table 5	GPIO	19
Table 6	Clock Pins	20
Table 7	JTAG Interface	20
Table 8	Microprocessor Interface	21
Table 9	Power Supply Pins	22
Table 10	Stream-to-Stream Connection Mapping	28
Table 11	Data Rates for Local and H-Bus	49
Table 12	Maximum possible data rates for HTSI in M-mode	49
Table 13	Maximum possible data rates for HTSI in H-mode	49
Table 14	TAP Controller Instructions	55
Table 15	Boundary Scan IDCODE	56
Table 16	IDCODE via μ P Read Access	57
Table 17	Register Overview For 8-Bit Interface	59
Table 18	Value Range for SPA/DPA	60
Table 19	Value Range for ITSA/OTSA	60
Table 20	Value Range for SCA	60
Table 21	Register Overview For 16-Bit Interface	90
Table 22	Affected Registers for Connection Commands	99
Table 23	Affected Registers for Configuration Commands	100
Table 24	Connection Command and Parameter Codes	102
Table 25	Configuration Command 1 and Parameter Codes	103
Table 26	Configuration Command 2 and Parameter Code	104
Table 27	PCM Timing	129
Table 28	PCM Parallel Mode Timing	131
Table 29	Component Timing Specification	135
Table 30	Clock Skew Timing	136
Table 31	SCLK-D Timing at 8.192 Mbit/s	137
Table 32	Infineon/Intel Timing in De-Multiplexed Mode	138
Table 33	Infineon/Intel Timing in Multiplexed Mode	140
Table 34	Motorola Timing	142
Table 35	JTAG Interface Timing	144
Table 36	Hardware Reset Timing	146
Table 37	Absolute Maximum Ratings	147
Table 38	Operating Range	148
Table 39	External Capacitances for Crystal (Recommendation)	149
Table 40	DC Characteristics	150
Table 41	Input/Output Capacitances	151

PRELIMINARY

Preface

The Switching IC (SWITI) is a family of switching devices for a wide area of telecommunication and data communication applications. This document provides complete reference information according to chip interfaces, programming, internal architecture and applications.

Organization of this Document

This Preliminary Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1, Overview**
Gives a general description of the product and of the SWITI family, lists the key features, and presents some typical applications.
- **Chapter 2, Pin Description**
Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
- **Chapter 3, Architectural Description**
Rough overview of the internal architecture and clock fallback feature.
- **Chapter 4, Description of Interfaces**
Short introduction of used interfaces.
- **Chapter 5, Register Description**
Gives information about all registers accessible via the microprocessor interface according to address, short name, access, reset value and value range.
- **Chapter 6, Programming the Device**
Gives a variety of examples how to program the device, lists all available command and parameter values.
- **Chapter 7, Timing Diagrams**
Contains timing diagrams.
- **Chapter 8, Electrical Characteristics**
Specification of the electrical parameters.
- **Chapter 9, Package Outlines**
Outlines of the available packages (P-BGA-217-1).

PRELIMINARY**Table 1 Who should read what?**

Addressed Person	Relevant Chapters
Programmer	3, 5, 6
Board Designer	2, 3, 4, 7, 8, 9

Related Documentation

H.100 Hardware Compatibility Specification: CT Bus, revision 1.0

H.110 Hardware Compatibility Specification: CT Bus, revision 1.0

PCI Specification, revision 2.1, PCI special interest group

Compact PCI Specification - PICMG 2.0, revision 2.1

Compact PCI Hot Swap Specification - PICMG 2.1, revision 1.0

H-MVIP Standard, Release 1.1a, GO-MVIP Inc., January 1997

MVIP-90 Standard, Release 1.1, GO-MVIP Inc., October 1994

SC-Bus Specification, ANSI/VITA 6-1994

1 Overview

The new switching family, called SWITI, provides a complete and cost-effective solution for all switching systems. The family is divided in two sub-families, the MTSI family and the HTSI family. The Preliminary Data Sheet describes the functionality and characteristic of the HTSI devices.

The devices can be used in today’s switching applications, e.g. conventional PBXs and central offices (CO’s), as well as in H.100/H.110 applications (only the HTSI family), which are the key to high performing CTI- and Voice-over-IP-applications, one of the most important future technologies in telecommunications.

The main requirements of today’s switching applications are met by the following features:

- Constant delay e.g. to support wide band data switching, or channel bundling
- Bit switching/subchannel switching to support applications such as mobile base stations, DECT, computer telephony

In addition, the SWITI family provides new features to ensure a broad range of configurations to make it possible to adapt the device to all switching applications:

- A compliant H.100/H.110 interface (HTSI)
- 8-channel stream-to-stream switching capability (HTSI)
- Message mode, which allows to assign a preset value to any output time-slot
- GPIO (General Purpose I/O) port, which is controlled from the external μ P

SWITI family. The SWITI family consists of 6 ICs with different switching capacities. The possible configurations are shown in [Table 2](#). The HTSI versions provide an additional H.100 / H.110 interface, while the MTSIs are standard switching devices. All devices can be programmed easily, thus helping the designer/programmer to integrate the device into his application comfortably.

Table 2 SWITI Family Tree

Name	Package	Sales code	Connections	Local bus IN/OUT	H-Bus I/O
HTSI-XL (H-Mode)	P-BGA-217-1	PEF24471 HTSI-XL	2048	16/16	32
HTSI-XL (M-Mode)		PEF24471 HTSI-XL		32/32	-
HTSI-L (H-Mode)	P-BGA-217-1	PEF20471 HTSI-L	1024	16/16	32
HTSI-L (M-Mode)		PEF20471 HTSI-L		32/32	-

Table 2 SWITI Family Tree (cont'd)

Name	Package	Sales code	Connections	Local bus IN/OUT	H-Bus I/O
HTSI (H-Mode)	P-BGA-217-1	PEF20451 HTSI	512	16/16	32
HTSI (M-Mode)		PEF20451 HTSI		32/32	-
MTSI-XL	P-MQFP-100-2	PEF24470 MTSI-XL	2048	16/16	-
MTSI-L	P-MQFP-100-2	PEF20470 MTSI-L	1024	16/16	-
MTSI	P-MQFP-100-2	PEF20450 MTSI	512	16/16	-

HTSI devices.

The HTSI devices can be operated in two different modes, H-Mode and M-Mode.

In H-Mode the device offers 16 local I/Os and additionally a compliant H.100/H.110 interface (32 bidirectional I/Os). The complete number of available connections can be assigned as H-bus to H-bus, local bus to local bus connection, or mixed.

In M-Mode all lines are configured as local I/Os, so that in total 32 local I/Os are provided. Thus e.g. the HTSI-XL device can be used as 2K non-blocking switch operating with all 32 I/Os at 4.096 Mbit/s.

PRELIMINARY

**Switching IC
SWITI**

PEF 20451 / 20471 / 24471

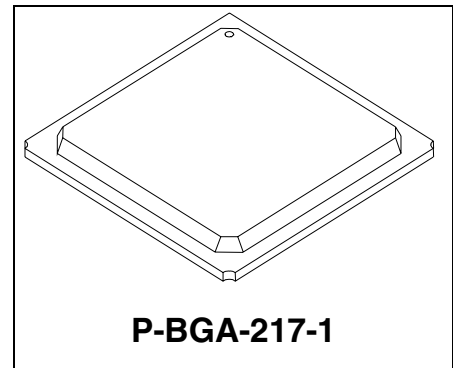
Version 1.3

CMOS

1.1 Overview of Features

General

- Switching capacity of 512, 1024, or up to 2048 connections of different types between different buses
- Programmable data rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s on per stream basis
- Constant delay or minimum delay programmable on per connection basis
- Subchannel switching ability of 1-bit, 2-bit, 4-bit wide time-slots
- Programmable clock shift for local bus
- 8-channel stream-to-stream switching for H.100/H.110 and interoperability bus
- Automatic data rate adaption
- Optional 8-bit parallel input and/or 8-bit parallel output for first 8 lines of local bus
- Broadcast capabilities
- Multipoint switching ability
- Read and write access to all time-slots
- Message mode (time-slot write access)
- Programmable framing group
- GPIO port
- 8-bit μ P-interface supports both Intel and Motorola mode
- Optional 16-bit μ P interface mode (instead of GPIO port)
- On chip PLL for H.100/H.110, SCbus, MVIP, MVIP-H clock operation (master/slave) and for local bus clock operation (master/slave)
- JTAG interface
 - Boundary scan according to IEEE 1149.1
- 3.3 V power supply
- 5 V tolerant inputs/outputs



Type	Package
PEF 20451 / 20471 / 24471	P-BGA-217-1

HTSI in H-Mode

- H.100/H.110 compliant interface with all mandatory signals
- Local bus of up to 16 PCM ports (16 In/16 Out)
- Hot swapping

HTSI in M-Mode

- Local bus of up to 32 PCM ports (32 In/32 Out).

1.2 Features in Detail**Flexible Data Rates**

Each input and each output line of the local bus is programmable to operate at different data rates. The possible data rates are 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s. Even for the HTSI in M-Mode all of the 32 input lines and 32 output lines are configureable, except for the bit rate of 16.384 Mbit/s.

In case of 16.384 Mbit/s only 24 lines can be used.

The possible data rate for the data lines of the H-Bus are 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Constant and Minimum Delay

Each connection independent of the addressed buses can be determined to be a constant delay or minimum delay connection. Constant delay means that any input time-slot or subchannel is available on the programmed output after 2 frames. Minimum delay means that the time-slot or subchannel appears at the output as soon as possible. The minimum delay depends on the chosen connections and the possible range is between 0 and 2 frames.

Subchannel Switching

Each connection can be a 1-bit, 2-bit, 4-bit, or 8-bit connection. Subchannel switching is applicable to both the local bus and the H-Bus and has a constant delay of 2 frames. Sub-Channel switching is supported only for data rate of 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Programmable Clock Shift

The position of time-slot 0 of each local bus input line can be programmed within the time-slot before and after the PFS rising edge in half clock steps. Also the position of time-slot 0 of all local bus output lines can be programmed within the first time-slot after the PFS rising edge.

8-Channel Stream-to-Stream Switching

This feature offers the possibility to efficiently switch one data stream to another at the same or different data rates without occupying switching memory capacity. It mainly supports interoperability between CT-bus (Computer Telephony) devices such as SCbus and MVIP-90 running at different data rates. It is possible to use up to 8 lines from the H.1x0 data lines to establish the connections. Input and output frequency can be configured differently.

Automatic Data Rate Adaption

Connections are also possible between lines operating at different data rates. The programmer just specifies input and output line, time-slot, and if necessary, the subchannel.

Parallel Mode

The first 8 local bus input and output lines can be configured to one parallel input or output port respectively. In serial mode a time-slot is determined by 8 consecutive data clock cycles according to each line. In parallel mode a time-slot is determined by 1 data clock cycle according to the first 8 lines.

Broadcast

With this feature it is possible to distribute one incoming time-slot to different output time-slots.

Multipoint

Multipoint connections can be seen as the opposite of broadcast connections. Here it is possible to generate one output time-slot consisting of several input time-slots. The specified input time-slots are logically AND or OR connected (selectable) and have a constant delay of 2 frames.

Read Access

The programmer has access to any input time-slot. After issuing an appropriate command the arrival of the time-slot will be reported by interrupt. The value can be read from a dedicated register. For every read request the command has to be issued again.

Message Mode (Write Access)

This feature allows a constant value to be sent to any given output time-slot.

Framing Group

It is possible to specify up to 8 different framing signals of 8 kHz. The position of the rising edge and the pulse width can be programmed for each signal. The reference frame is determined by the PFS signal. The pulse parameters are programmed in half step resolution according to a 16.384 MHz clock.

General Purpose Clocks

All 8 GPCLK lines can be configured as individual clock outputs with 8 kHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz and for test purposes with the internal frequency or the input frequency of the analog PLL (APLL).

GPIO Port

Each line of the general purpose input/output port can be configured to be either input or output. According to an input an edge causes an interrupt. The outputs can be influenced by write access via the microprocessor interface. Thus the user has the possibility to observe and influence additional signals for his application.

Microprocessor Interface

All devices provide a standard 8-bit microprocessor interface operating in either Intel or Motorola mode. Optionally it is possible to configure the GPIO port as additional data lines to provide a 16-bit microprocessor interface. The use of the 16-bit μ P interface reduces the number of write cycles required to configure a connection from 7 (in case of 8-bit μ P interface) to 3 write cycles.

Input/Output Tolerance

The HTSI can be used in a 5 V environment with two additional 5 V (VDD) power supply pins. Local input and outputs are 3.3 V and 5 V tolerant. The outputs have TTL level driving capability. The H-Bus lines of the HTSI can be used in a 3.3 V signaling PCI environment.

1.3 Logic Symbol

The HTSI is dedicated to perform time-slot switching between the local bus and the H-Bus or to offer a solution for applications with a high number of local I/Os. The HTSI operates in two modes. In H-Mode (**Figure 1**) it works with the H-Bus and in M-Mode (**Figure 2**) it operates without the H-Bus.

The HTSI in H-Mode provides 16 PCM input lines and 16 PCM output lines and the complete H-Bus with 32 bidirectional H.100/H.110 data lines.

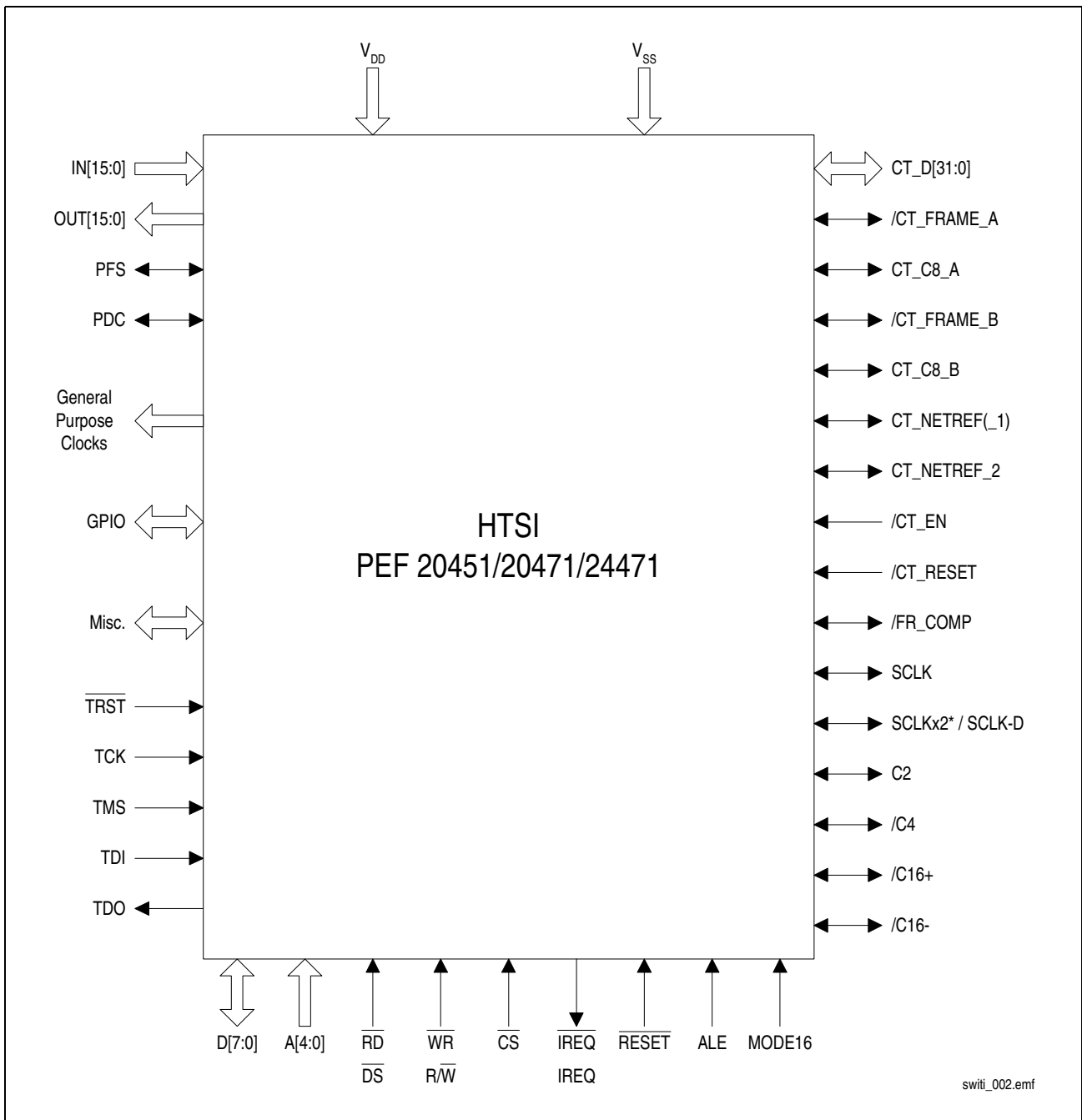


Figure 1 Logic Symbol: HTSI in H-Mode

If no H-Bus is needed it is possible to configure the HTSI in M-Mode. In this mode, the HTSI provides 32 PCM input lines and 32 PCM output lines.

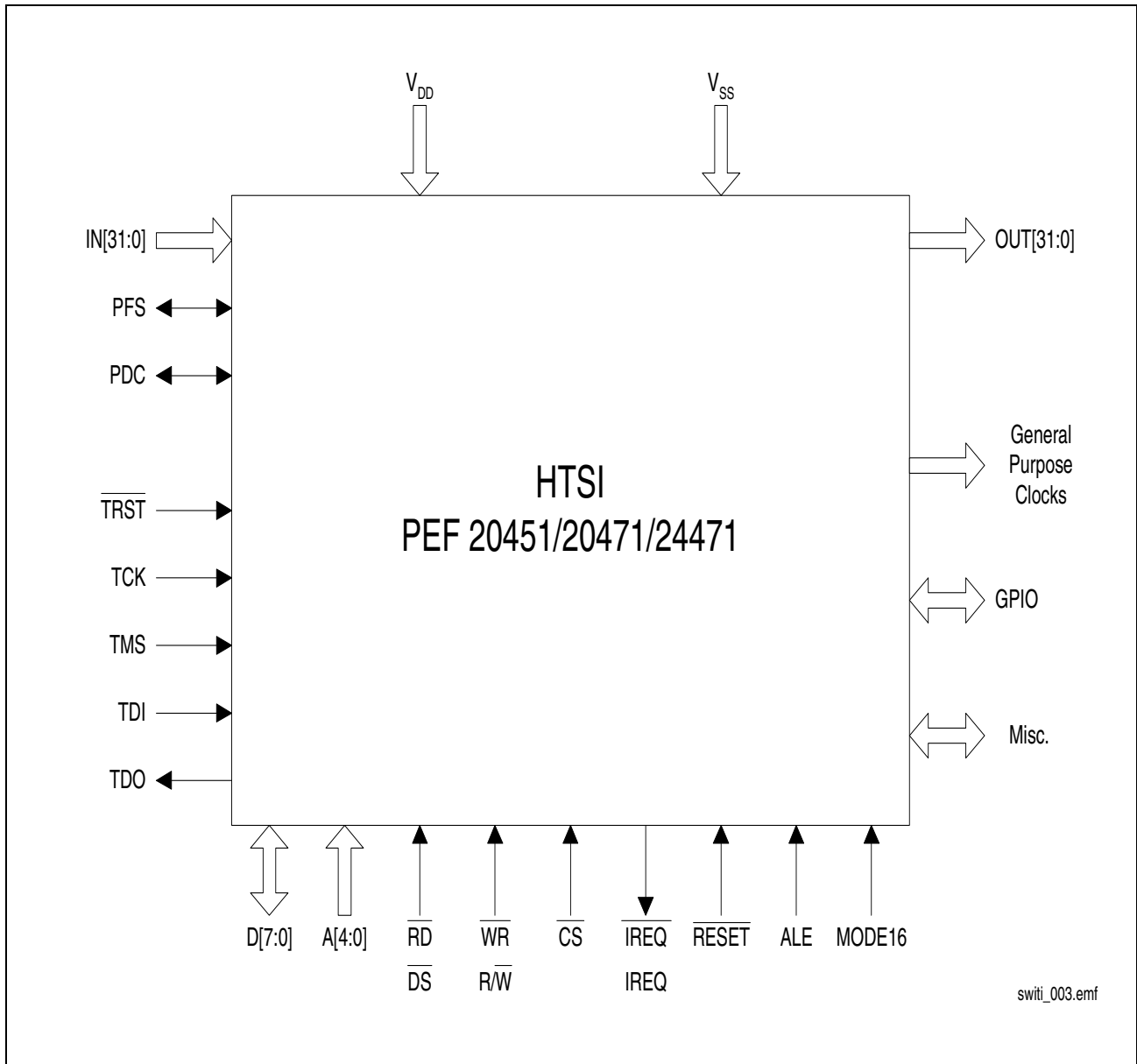


Figure 2 Logic Symbol: HTSI in M-Mode

1.4 Typical Applications

Typical applications of the SWITI family are:

- PCM switch, concentrator or multiplexer in PBXs, COs or mobile base stations
- H.100/H.110 interface in
 - Computer telephony systems
 - Internet telephony systems
 - LAN/WAN access devices
 - Enhanced service platforms

The following sections give a general overview of the system integration of the SWITI family.

1.4.1 Standard PBX or CO Application

The MTSI or the HTSI in M-Mode can be used, just as the MTSC or MTSL, in standard private branch exchange or central office applications ([Figure 3](#)), e.g. in the switching network.

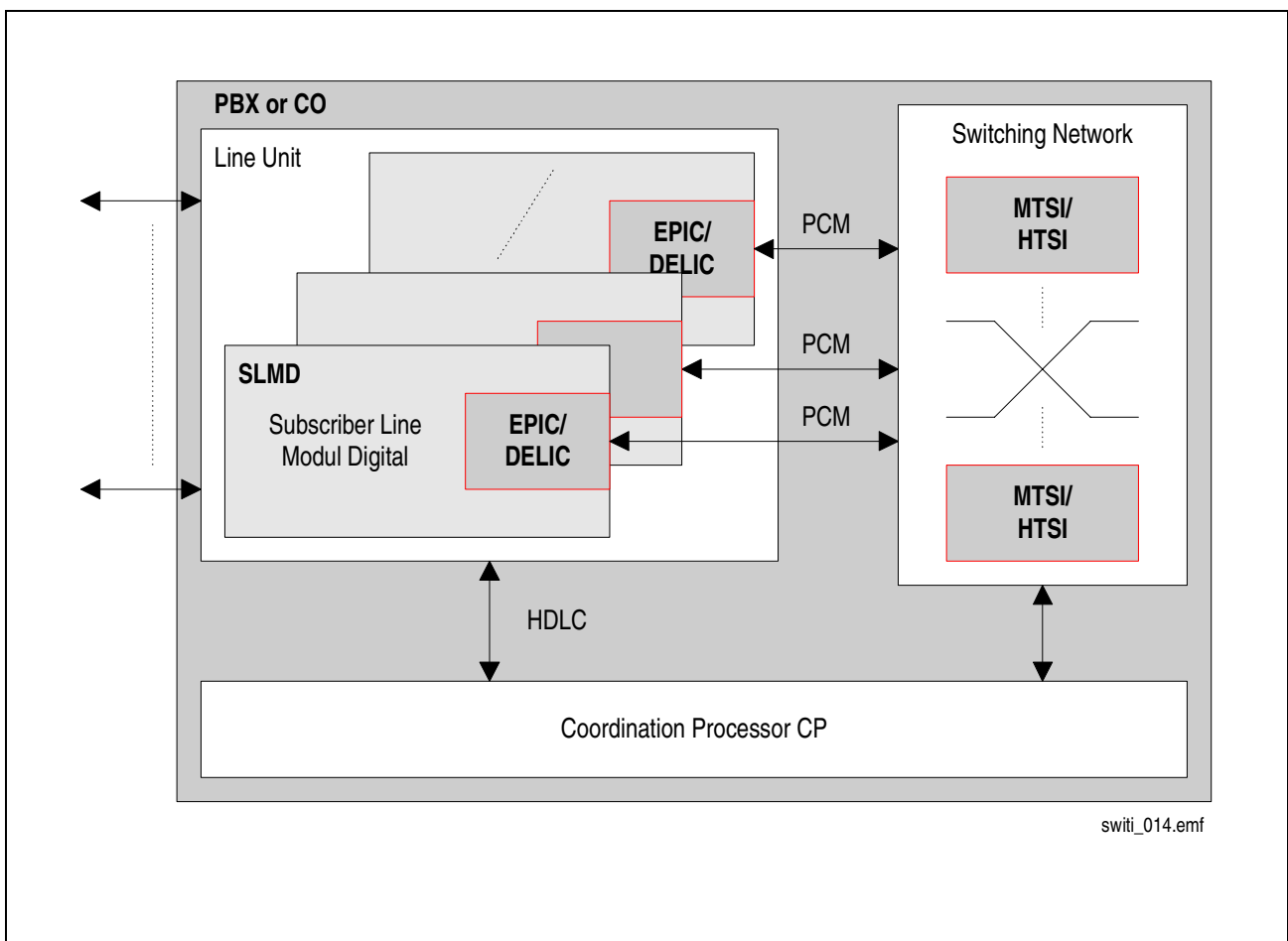


Figure 3 Standard PBX or CO Application

1.4.2 Computer Telephony Application

In Computer Telephony Integration (CTI) applications, resources such as the analog telephone line cards, ISDN ports, switching controllers, FAX firmware, or voice processing modules are in the form of plug-in cards that sit on the ISA or PCI slots of a PC. Resource sharing is established by connecting the top of the plug-in cards with cables. This Time Division Multiplex (TDM) bus has evolved from the original H-MVIP, MVIP-90, Dialogic's SC-Bus, into the latest H.100/H.110 bus or H-Bus developed by the Enterprise Computer Telephony Forum (ECTF). By connecting to the H.100/H.110 interface devices, system modules may send and receive data to and from any one of the 4096 TDM time-slots of the H-Bus. The H-Bus also offers the ideal solution for routers to provide a bridge between the data communication and telecommunication system modules.

In Computer Telephony (CT) environment, resource sharing is accomplished by passing data back and forth through the H.100/H.110 bus. **Figure 4** shows the example.

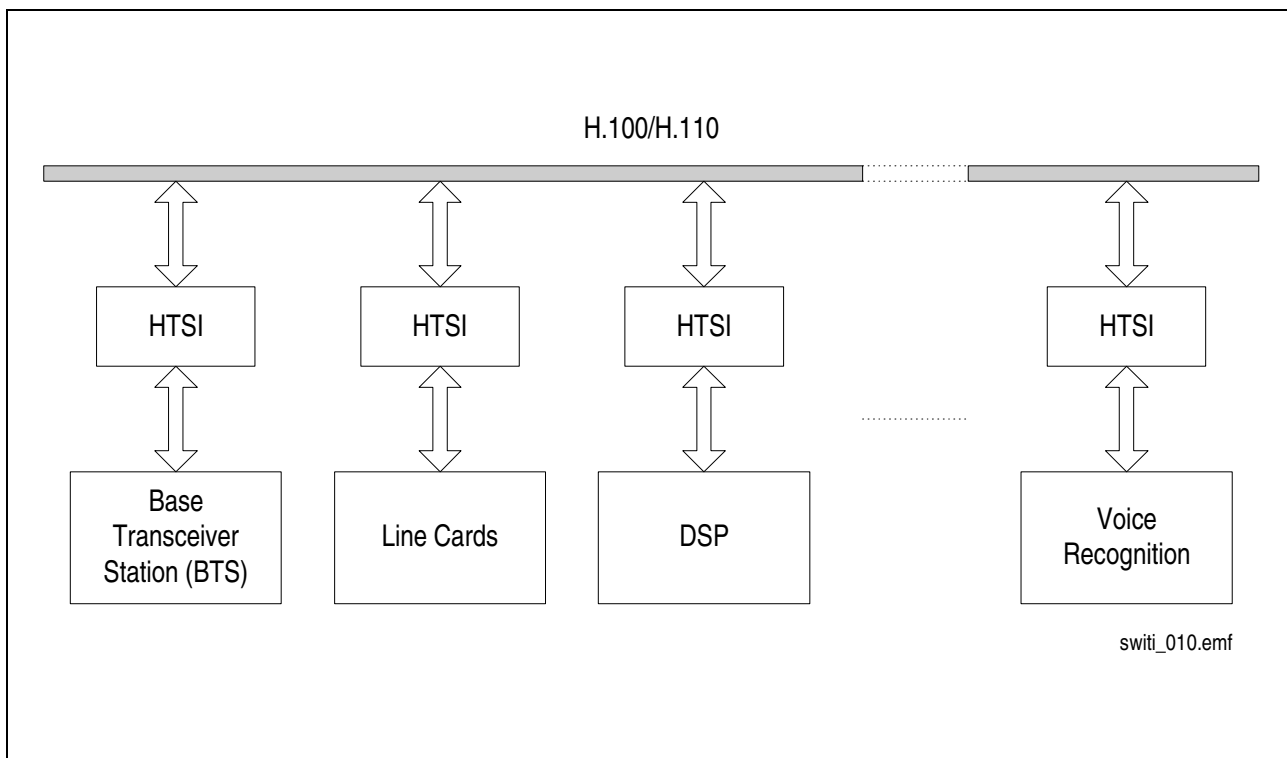


Figure 4 CT Application

1.4.3 Router / Remote Access Application

The HTSI (H-Mode) or also the MTSI (if no H-Bus interface is used in the system) is used in multivoice applications as the bridge connecting the data communication modules to the telecommunication modules in a router/remote access design. **Figure 5** shows the example.

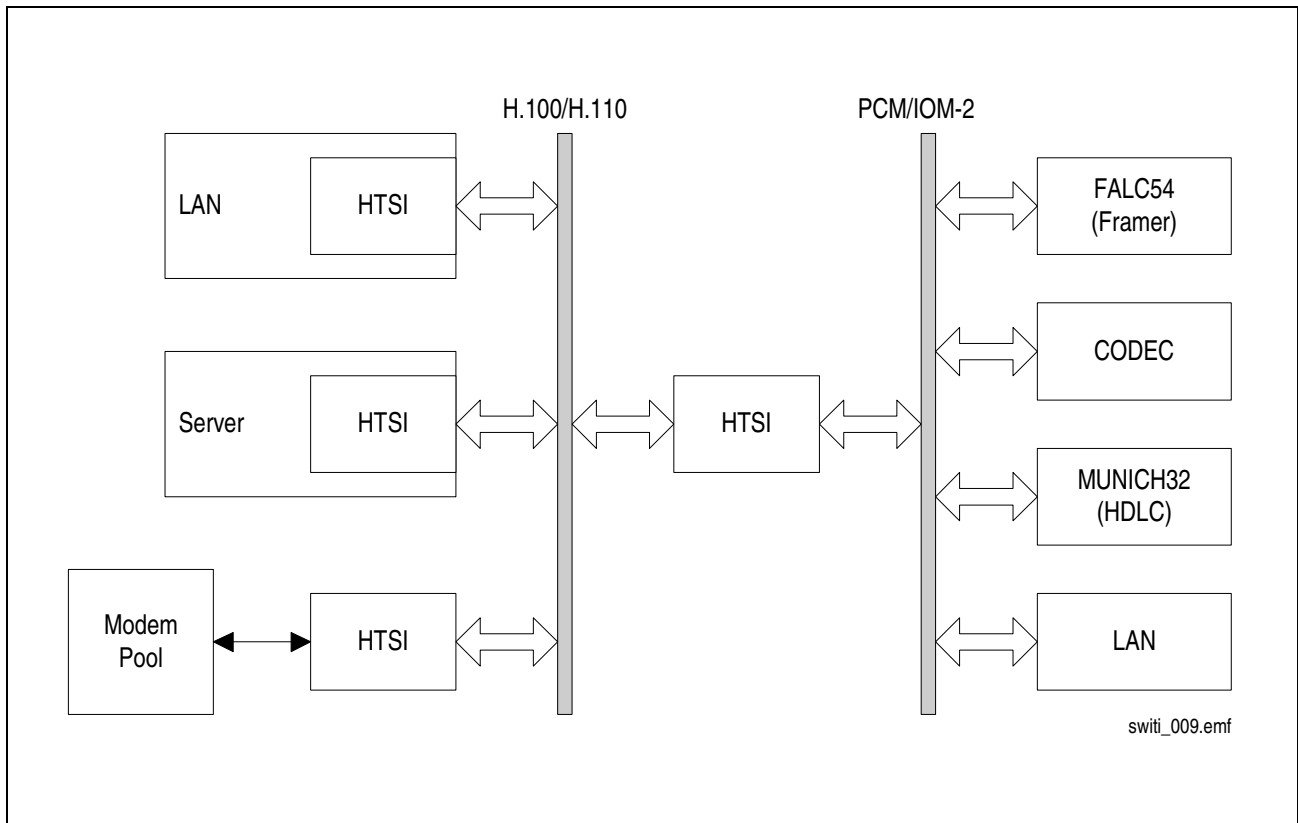


Figure 5 Router / Remote Access Applications

1.4.4 Voice over IP Application

In a voice over IP application (**Figure 6**) the HTSI (in H-Mode) may be used to connect a conventional PBX to the H-Bus. A Vocoder card, also connected to the H-Bus, performs speech compression and decompression whereas an Ethernet card transmits and receives the compressed data over the network.

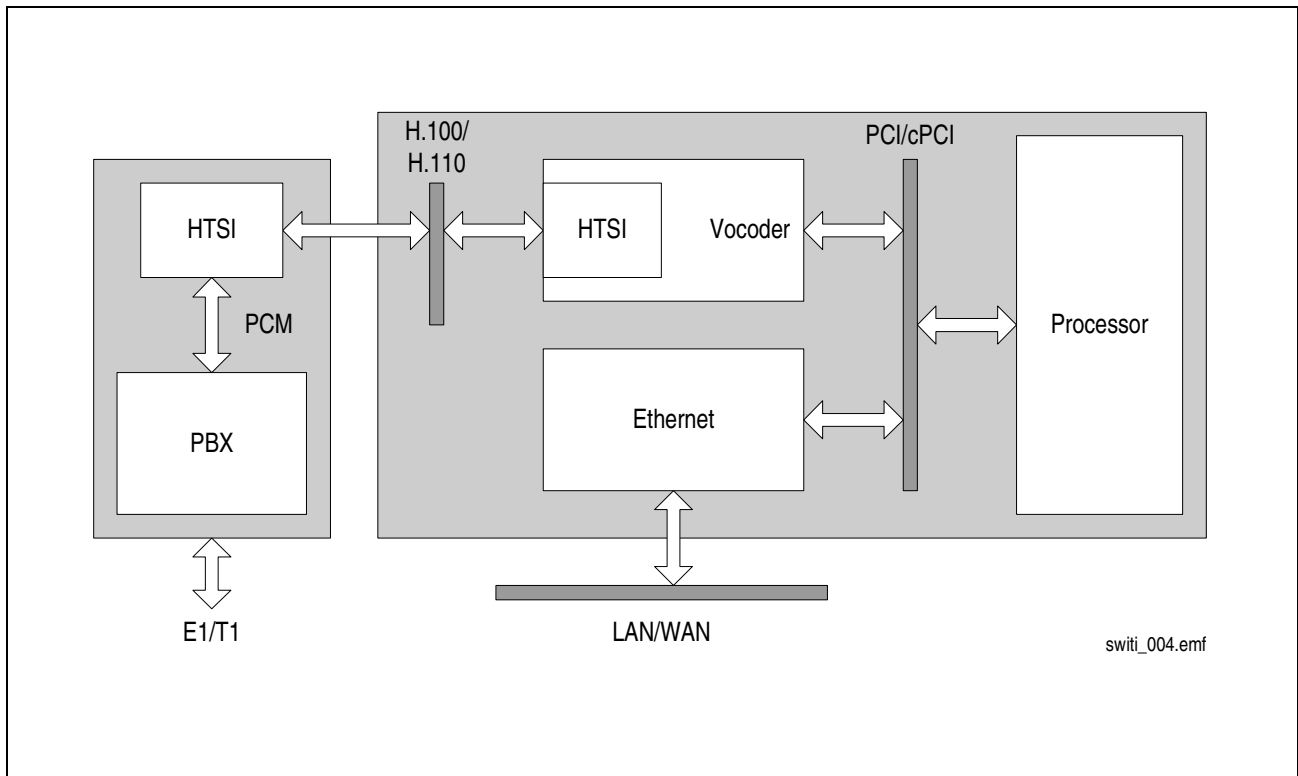


Figure 6 Voice over IP Application