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SIEMENS

ICs for Communications

Extended PCM Interface Controller

EPIC®-1
PEB 2055 / PEF 2055 Versions A3

EPIC®-S
PEB 2054 / PEF 2054 Versions 1.0

User's Manual 02.97

PEB 2055 PEF 2055 Revision History:		User's Manual 02.97
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1 Overview

The PEB 2055 (**E**xtended **P**CM **I**nterface **C**ontroller) is a highly integrated controller circuit optimized for analog and ISDN line card and central switches applications. The EPIC-1 provides the circuitry necessary to manage up to 32 digital (ISDN or proprietary) or 64 analog subscribers.

The EPIC-1 is dedicated to switch PCM data between two serial interfaces, the system interface (PCM interface) and the configurable interface (CFI). The EPIC-1 performs non-blocking time and space switching for up to 128 channels.

Since the system cost of the EPIC-1 is divided by the number of lines it controls, an highly economical implementation of digital or analog subscriber lines can be performed.

The EPIC-S (PEB 2054) is a pin compatible device offering half the switching capacity of the EPIC-1. Therefore the EPIC-S is capable of handling up to 16 ISDN or 32 analog subscribers. It is programmable according to the EPIC-1 with respect of the pins not available.

The EPIC is implemented in a Siemens advanced CMOS-technology and manufactured in a P-LCC-44-1 package.

The EPIC is member of a chip family supporting a highly economical implementation of line cards and subscriber terminals.

Chip Family

Line Cards:

PEB 2055	Extended PCM Interface Controller	(EPIC)
PEB 20550	Extended Line Card Controller	(ELIC)
PEB 2096	Octal U_{PN} Transceiver	(OCTAT-P)
PEB 2095	ISDN Burst Transceiver Circuit	(IBC)
PEB 2084	Quadruple S_0 Transceiver	(QUAT-S)
PEB 2465	Quadruple DSP based Codec Filter	(SICOFI-4)
PEB 2075	ISDN D-Channel Exchange Controller	(IDEC)

Terminals:

PSB 2196	Digital Subscriber Access Controller for U_{PN} Interface	(ISAC-P TE)
PEB 2081 (V3.2)	S/T-Bus Interface Circuit Extended	(SBCX)

SIEMENS

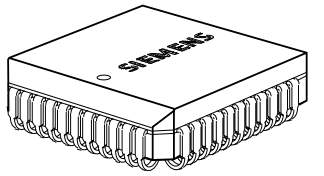
Extended PCM Interface Controller
EPIC®-1, EPIC®-S

PEB 2055
PEF 2055
PEB 2054
PEF 2054

Versions A3 (PEB 2055), V1.0 (PEB 2054)

CMOS

1.1 Features



P-LCC-44-1

Switching

- Board Controller for up to
  - 32 ISDN or 64 analog subscribers (PEB 2055)
  - 16 ISDN or 32 analog subscribers (PEB 2054)
- Non-blocking switch for
  - 128 channels (PEB 2055)
  - 64 channels (PEB 2054)
- Switching of 16-, 32-, or 64-kbit/s channels
- Two consecutive 64-kbit/s channels can be switched as a single 128-kbit/s channel
- Freely programmable time slot assignment for all subscribers
- Two serial interfaces (PCM and CFI) programmable over a wide data range (128 - 8192 kbit/s)
- Data rates of PCM and configurable interface independent from each other (data rate adaptation)
- PCM-interface
  - Tristate control signals for external drivers
  - Programmable clock shift
  - Single or double data clock
- Configurable interface
  - Configurable for IOM-, SLD- and PCM-applications
  - High degree of flexibility for datastream adaptation
  - Programmable clockshift
  - Single or double data clock
- Synchronous µP-access to two selected channels

Type	Ordering Code	Package
PEB 2055	Q67100-H6035	P-LCC-44-1
PEF 2055	Q67100-H6216	P-LCC-44-1
PEB 2054	Q67100-H6420	P-LCC-44-1
PEF 2054	Q67100-H6534-B701	P-LCC-44-1

Handling of Layer-1 Functions

- Change detection for C/I-channel (IOM-configuration) or feature control (SLD-configuration)
- Double last-look logic for C/I-channel (IOM-2 analog configuration)
- Additional last-look logic for feature control (SLD-configuration)
- Buffered monitor (IOM-configuration) or signaling channel (SLD-configuration)

Bus Interface

- Siemens/Intel or Motorola type µP-interface
- 8-bit demultiplexed bus interface
- FIFO-access interrupt or DMA controlled

1.2 Pin Configuration

(top view)

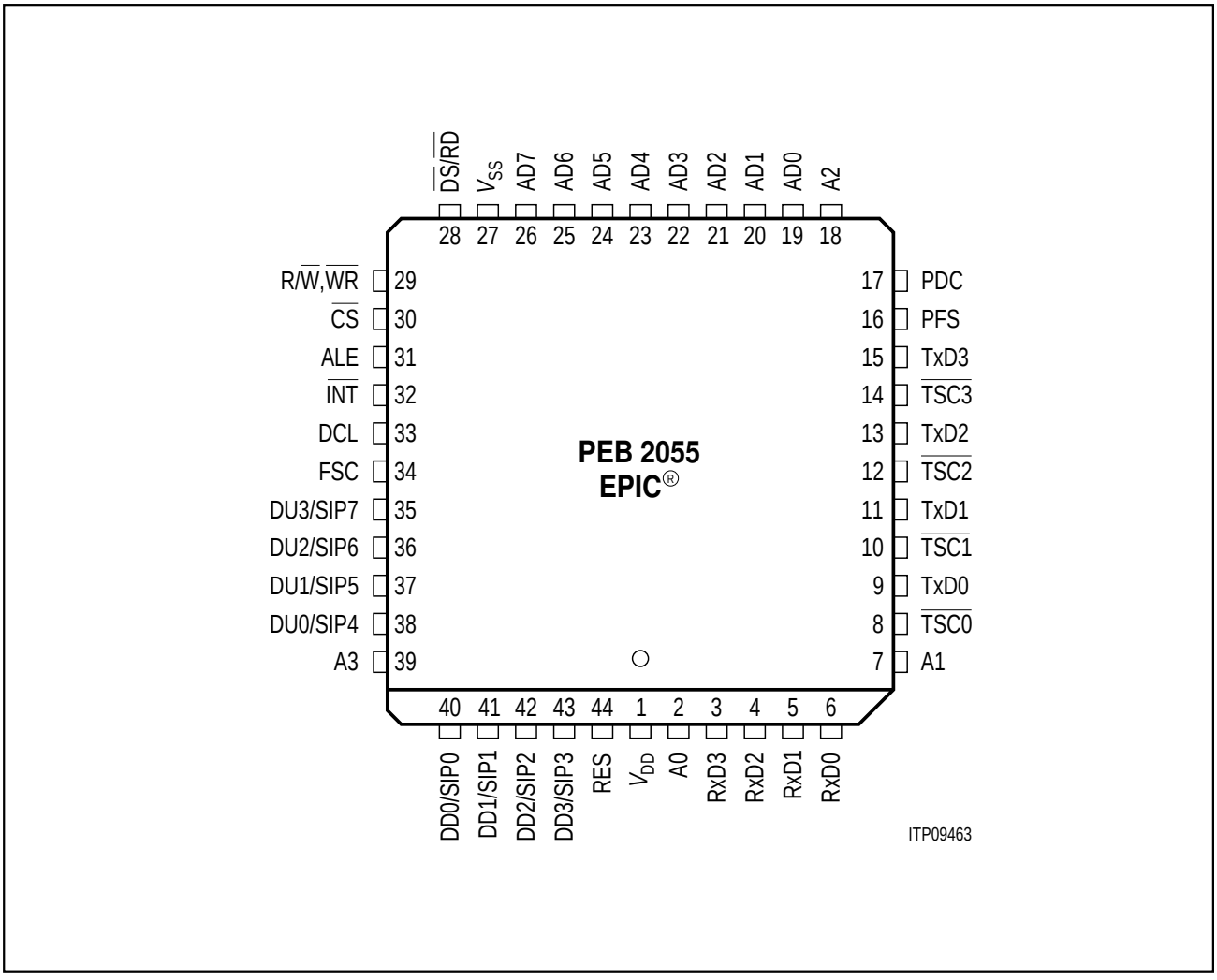


Figure 1
Pin Configuration EPIC®-1

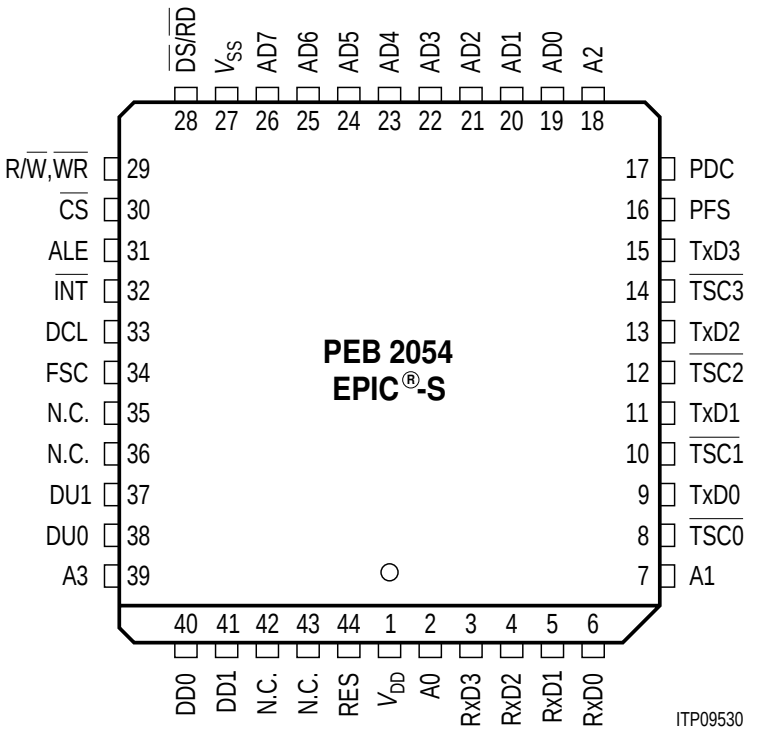


Figure 2
Pin Configuration EPIC®-S

1.3 Pin Definitions and Functions

Pin No. EPIC-S	Pin No. EPIC	Symbol	Input (I) Output (O)	Function
30	30	$\overline{CS}$	I	**C**hip **S**elect; active low. A “low” on this line selects the EPIC for read/write operations.
29	29	$\overline{WR}$, R/$\overline{W}$	I	**Wr**ite, active low, Siemens/Intel bus mode. When “low”, a write operation is indicated. **R**ead/**W**rite, Motorola bus mode. When “high” a valid µP-access identifies a read operation, when “low” it identifies a write access.
28	28	$\overline{RD}$, $\overline{DS}$	I	**R**ea**d**, active low, Siemens/Intel bus mode. When “low” a read operation is indicated. **D**ata **S**trobe, Motorola bus mode. A rising edge marks the end of a read or write operation.
19 20 21 22 23 24 25 26	19 20 21 22 23 24 25 26	AD0, D0 AD1, D1 AD2, D2 AD3, D3 AD4, D4 AD5, D5 AD6, D6 AD7, D7	I/O I/O I/O I/O I/O I/O I/O I/O	**A**ddress/**D**ata Bus; multiplexed bus mode. Transfers addresses from the µP-system to the EPIC and data between the µP and the EPIC. **D**ata Bus; demultiplexed bus mode. Transfers data between the µP and the EPIC. **When driving data the pins have push pull characteristic, otherwise they are in high impedance state.**
31	31	ALE	I	**A**ddress **L**atch **E**nable ALE controls the on chip address latch in multiplexed bus mode. While ALE is “high”, the latch is transparent. The falling edge latches the current address. During the first read/write access following reset ALE is evaluated to select the bus mode.
32	32	$\overline{INT}$	O (OD)	**Int**errupt Request, active low. This signal is activated when the EPIC requests an interrupt. Due to the open drain (OD) characteristic of $\overline{INT}$ multiple interrupt sources can be connected together.
44	44	RES	I	**Res**et A “high” forces the EPIC into reset state.
16	16	PFS	I	**P**CM Interface **F**rames **S**ynchronization

1.3 Pin Definitions and Functions (cont'd)

Pin No. EPIC-S	Pin No. EPIC	Symbol	Input (I) Output (O)	Function
17	17	PDC	I	**P**CM Interface **D**ata **C**lock Single or double data rate.
6 5 4 3	6 5 4 3	RxD0 RxD1 RxD2 RxD3	I I I I	**R**eceive PCM Interface **D**ata Time-slot oriented data is received on this pins and forwarded into the downstream data memory of the EPIC.
9 11 13 15	9 11 13 15	TxD0 TxD1 TxD2 TxD3	O O O O	**T**ransmit PCM Interface **D**ata Time slot oriented data is shifted out of the EPIC's upstream data memory on this lines. **For time-slots which are flagged in the tristate data memory or when bit OMDR:PSB is reset the pins are set to high impedance state.**
8 10 12 14	8 10 12 14	$\overline{\text{TSC0}}$ $\overline{\text{TSC1}}$ $\overline{\text{TSC2}}$ $\overline{\text{TSC3}}$	O O O O	**T**ri**s**tate **C**ontrol Supplies a control signal for an external driver. These lines are "low" when the corresponding TxD outputs are valid. During reset these lines are "high".
34	34	FSC	I/O	**F**rame **S**yn**c**hronization Input or output in IOM configuration. Direction indication signal in SLD mode.
33	33	DCL	I/O	**D**ata **Cl**ock Input or output in IOM, slave clock in SLD configuration. In IOM configuration single or double data rate, single data rate in SLD mode.
38 37 - -	38 37 36 * 35 *	DU0/SIP4 DU1/SIP5 DU2/SIP6 DU3/SIP7	I/IO (OD) I/IO (OD) I/IO (OD) I/IO (OD)	**D**ata **U**pstream Input; IOM or PCM configuration. **S**erial **I**nterface **P**ort, SLD configuration. **Depending on the bit OMDR:COS these lines have push pull or open drain characteristic. For unassigned channels or when bit OMDR:CSB is reset the pins are in the state high impedance.** *** Note: EPIC-1 only**

1.3 Pin Definitions and Functions (cont'd)

Pin No. EPIC-S	Pin No. EPIC	Symbol	Input (I) Output (O)	Function
40 41 - -	40 41 42 * 43 *	DD0/SIP0 DD1/SIP1 DD2/SIP2 DD3/SIP3	O/IO (OD) O/IO (OD) O/IO (OD) O/IO (OD)	**D**ata **D**ownstream Output, IOM or PCM configuration. **S**erial **I**nterface **P**ort, SLD configuration. **Depending on the bit OMDR:COS these lines have push pull or open drain characteristic. For unassigned channels or when bit OMDR:CSB is reset the pins are in the high impedance state.** *** Note: EPIC-1 only**
2 7 18 39	2 7 18 39	A0 A1 A2 A3	I/O	**A**ddress bus in the demultiplexed µP interface mode.
1	1	V_{DD}	I	Supply voltage: 5 V ± 5%
27	27	V_{SS}	I	Ground: 0 V

1.4 Logic Symbols

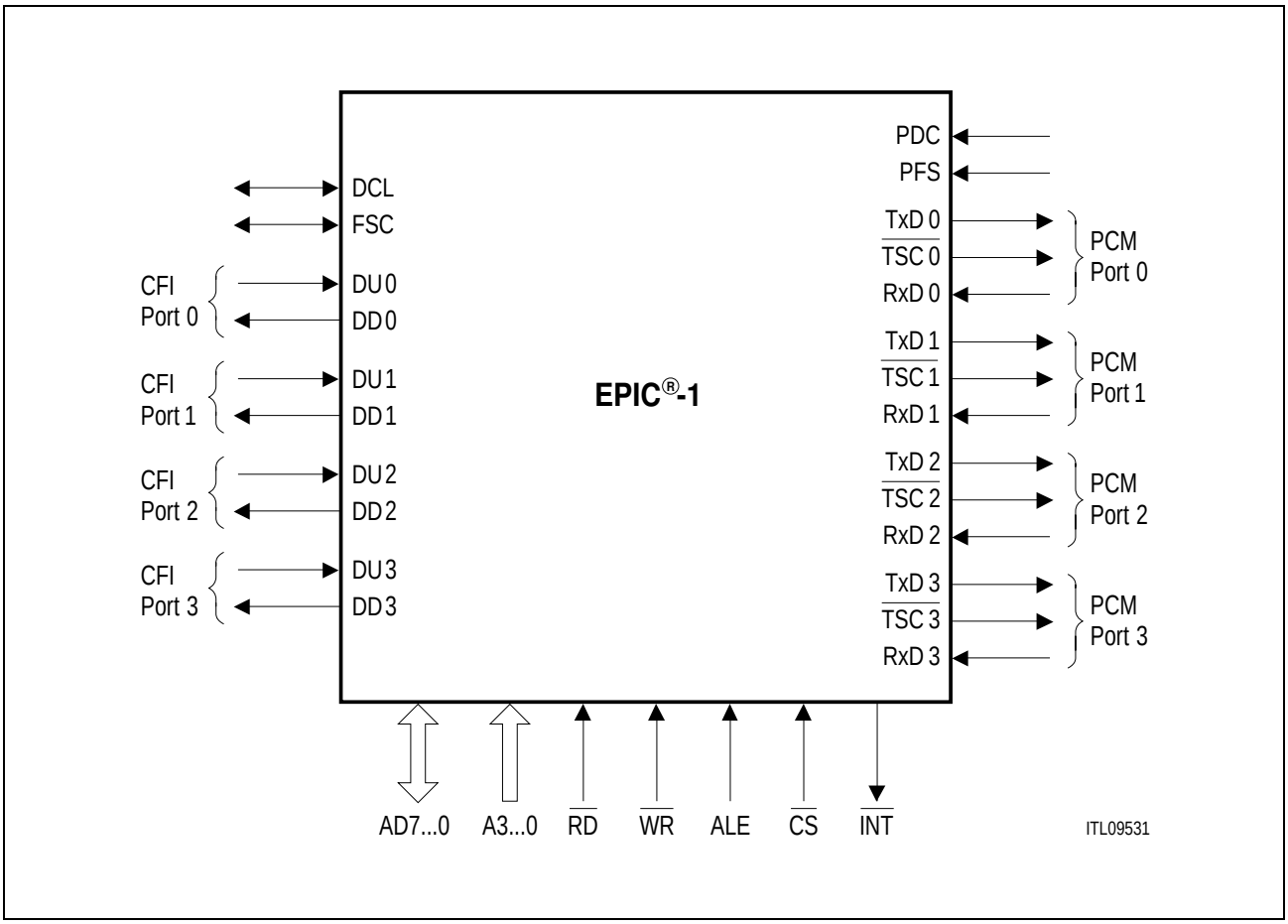


Figure 3
Logic Symbol of the EPIC®-1

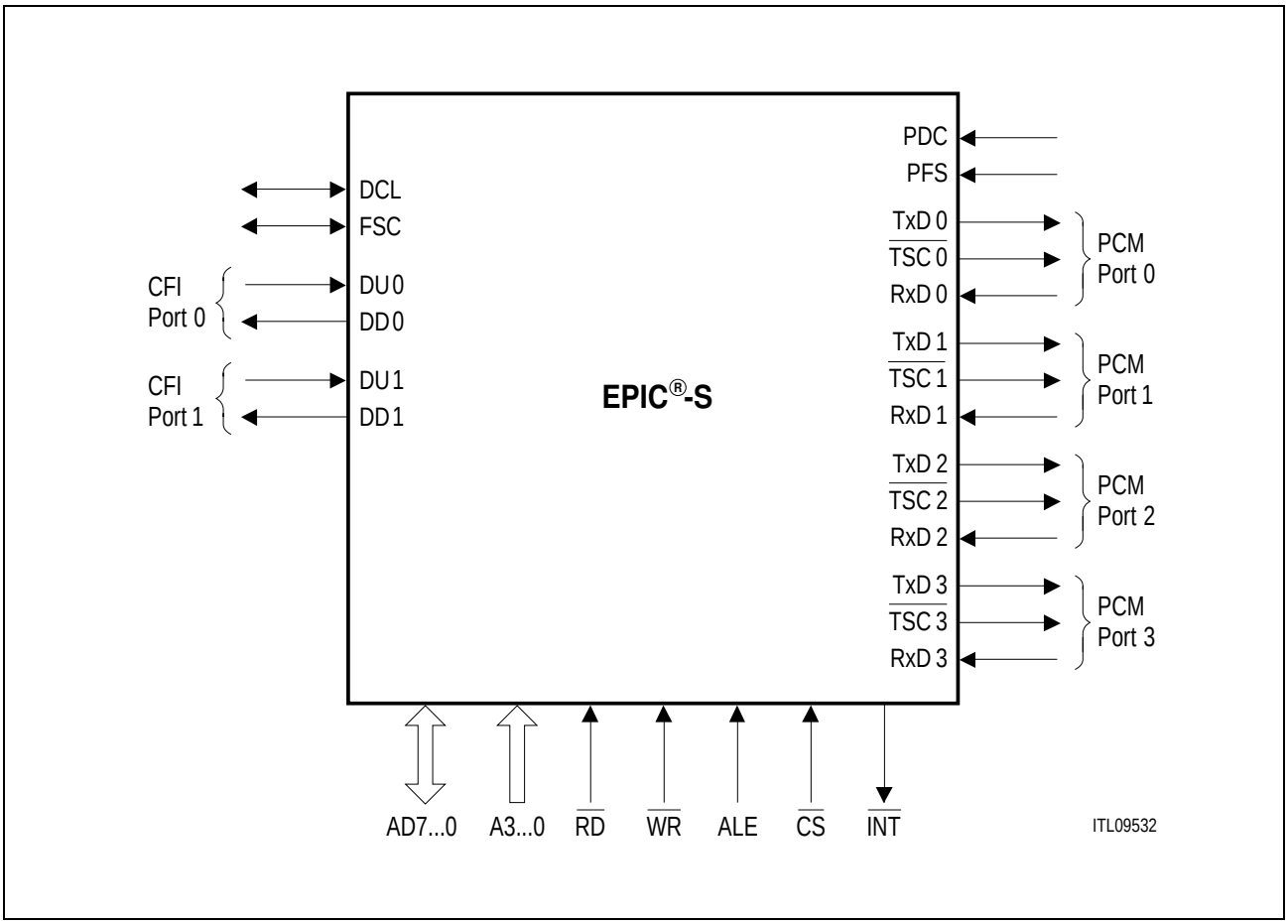


Figure 4
Logic Symbol of the EPIC®-S

1.5 Functional Block Diagram

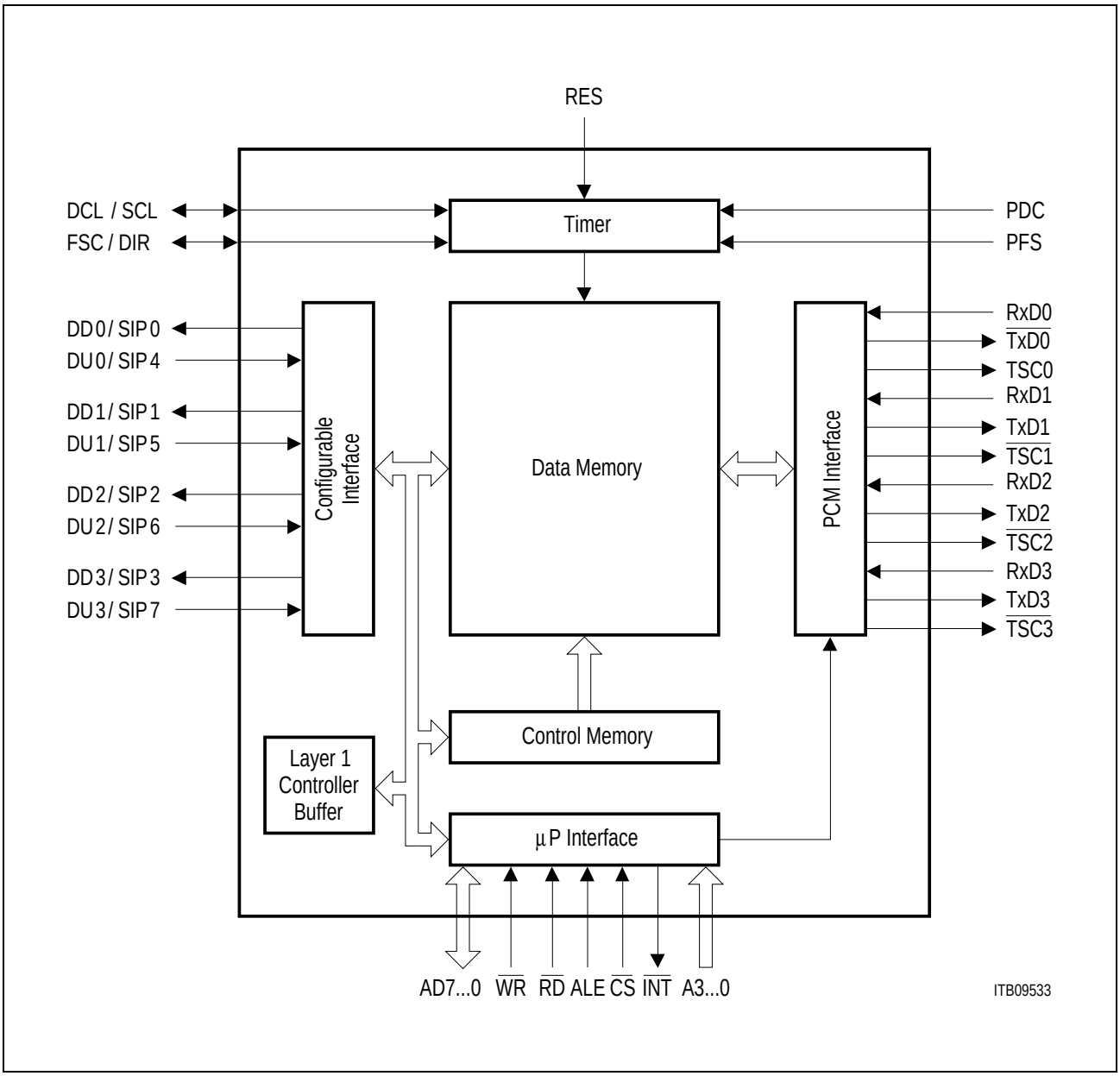


Figure 5
Functional Block Diagram EPIC®

1.6 Using the EPIC-S

The EPIC-S is based on the same technology as the EPIC-1 aside from only providing CFI port 0 and CFI port 1. Therefore this User's Manual applies to both, the EPIC-S and the EPIC-1.

When using the EPIC-S the user has to be aware not to program connections that would imply the not supported CFI ports.

The following points require specific attention:

1. During power up the EPIC-S must be supplied with an external Hardware Reset.
2. Register bit OMDR:CSB may be programmed to high (switch off standby of CFI interface) only after a Control Memory reset procedure with MACR:CMC3..0 = 0_H.
3. The pins not available with respect to the EPIC-1 (PEB 2055) must not be programmed as outputs.

1.7 System Integration and Application

The main application fields of the EPIC are:

- Digital line cards with different architectures,
- Central control units of key systems,
- Analog line cards,
- Concentrators.

1.7.1 Digital Line Card

1.7.1.1 Switching, Layer-1 Control

The EPIC provides a switching capability for up to 32 digital subscribers between the PCM system highway and the IOM-2 interface (64 B-channels). Typically it switches 64-kbit/s channels between the PCM and the IOM-interfaces. Moreover it is able to handle also 16-, 32- and 128-kbit/s channels.

The signaling handler supports the command/indication (C/I) channel which is used to exchange predefined layer-1 information with the transceiver device.

A monitor handler supports the handshake protocol defined on the IOM-monitor channel. It allows programming of layer-1 devices which do not have a dedicated µP interface.

The EPIC can be operated in tandem, i.e. one device is active, another one is a backup device. The backup device can instantaneously take over from the active device when the active device fails. Due to this tandem operation capability and the high number of ISDN subscribers which can be connected to one EPIC, the use of single line cards is feasible.

Several line card architectures are possible.

1.7.1.2 Decentralized D-Channel Handling

In completely decentral D-channel processing architectures (see **figure 6**), the processing capacity of the line card is usually designed to avoid blocking situations even under maximum conceivable D-channel traffic conditions. In such an architecture the EPIC switches the B-channels and performs C/I and monitor channel control.

The IDECs handle the layer 2 functions for signaling and data packets in the D-channel. They transfer the extracted data via the µP and an HDLC controller, e.g. the HSCX (High Level Serial Controller Extended SAB 82525) to the system. One of the channels of the HSCX may access either a time slot of programmable bandwidth on one of the system highways or a separate signalling highway.

In both cases the highway capacity used for packet traffic can be shared among several line cards due to the statistical multiplexing capabilities of the HSCX.

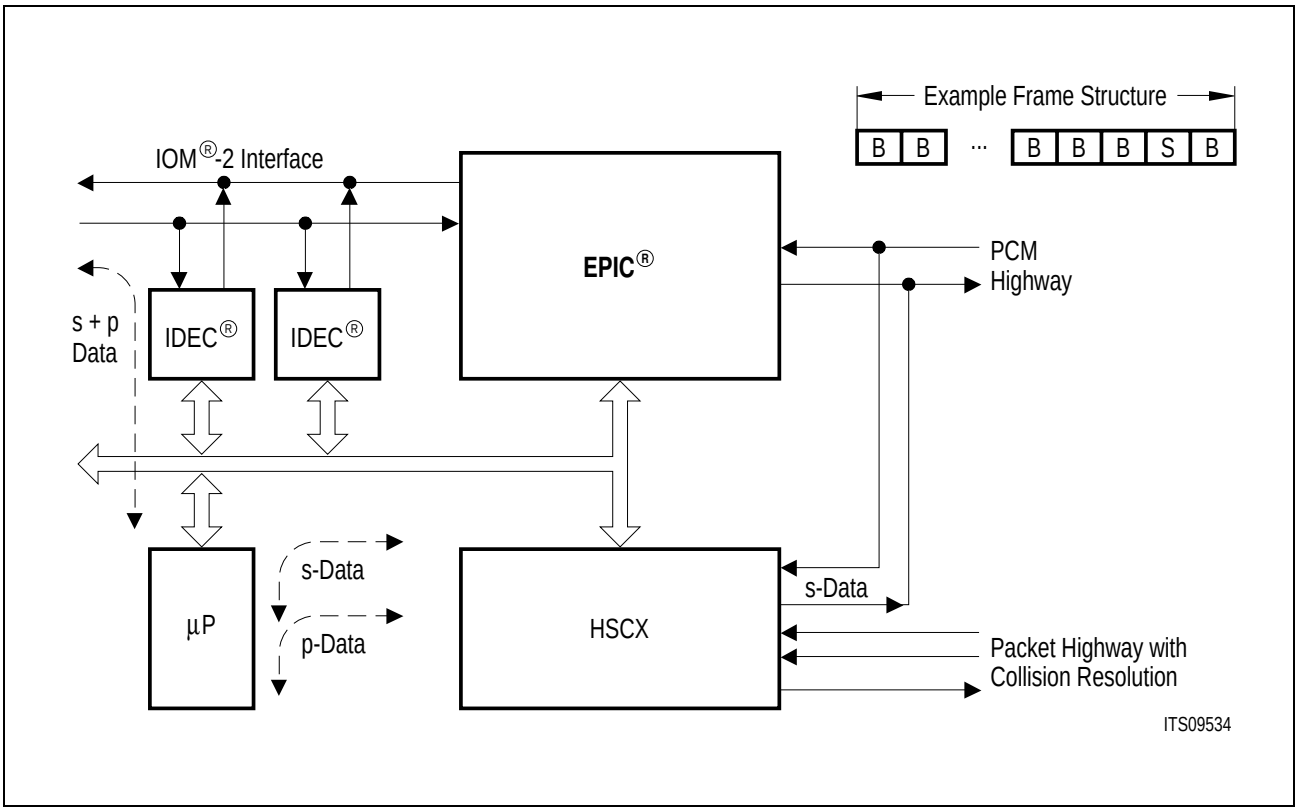


Figure 6
Line Card Architecture for Completely Decentral D-Channel Processing

1.7.1.3 Central D-Channel Processing

In this application the EPIC not only switches the B-channels and performs the C/I- and monitor channel control function, but switches also the D-channel data onto the system highway. In upstream direction the EPIC can combine up to four 16-kbit/s D-channels into one 64-kbit/s channel. In downstream direction it provides the capability to distribute one 64-kbit/s channel to four 16-kbit/s channels.

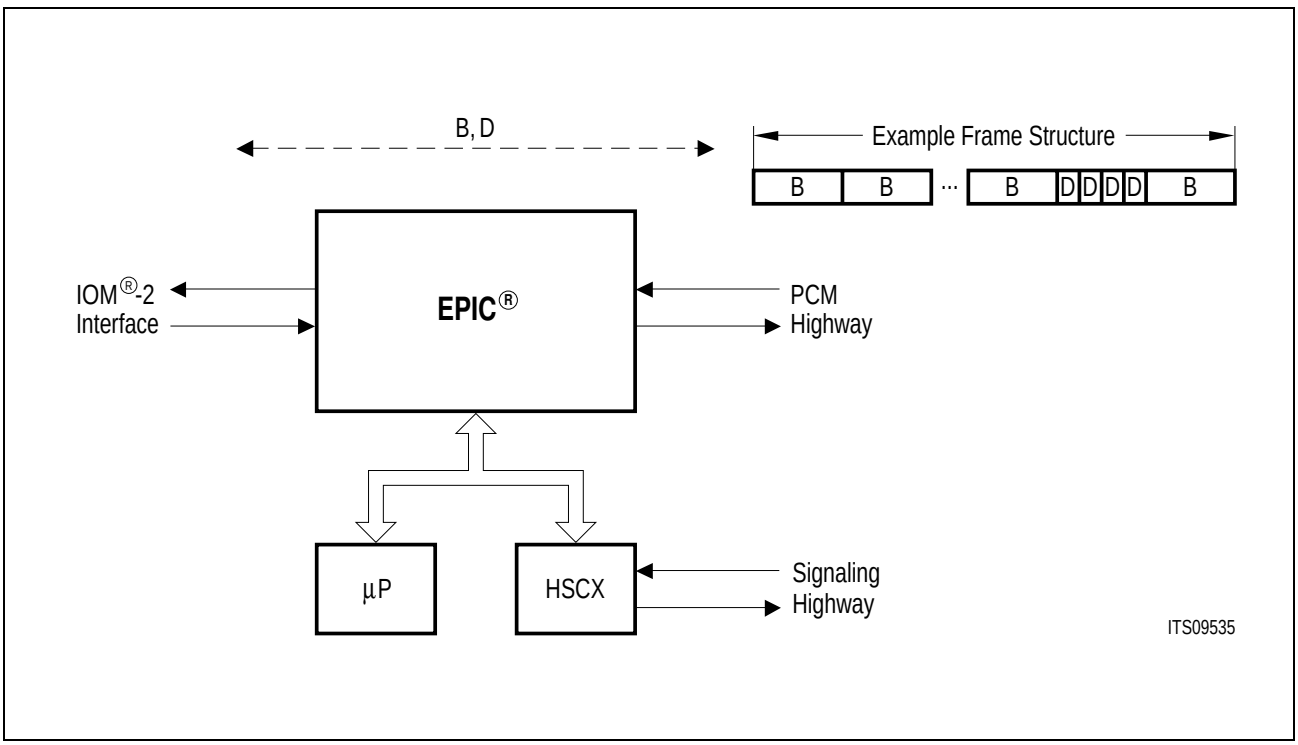


Figure 7
Digital Line Card Architecture with a Completely Central D-Channel Handling

1.7.1.4 Mixed D-Channel Processing, Signaling Decentralized, Packet Data Centralized

Another possibility is a mixed architecture with centralized packet data and decentralized signaling handling. This is a very flexible architecture which reduces the dynamic load of central processing units by evaluating the signaling information on the line card, but does not require resources for packet data handling. Any increase of packet data traffic does not necessitate a change in the line card architecture, the central packet handling unit can be expanded.

In this application IDECs are employed to handle the data on the D-channel. The IDECs separate signaling information from data packets. The signaling messages are transferred to the µP, which in turn hands them over to the group controller using the HSCX.

The packet data is processed differently. Together with the collision resolution information it is transferred to one IOM-2 port of the EPIC. The EPIC switches the channels to the PCM-highway, optionally combining four D-channels to one 64-kbit/s channel. In this configuration one IOM-2 interface is occupied by IDECs, reducing the total switching capability of the EPIC-1 to 24 ISDN-subscribers.

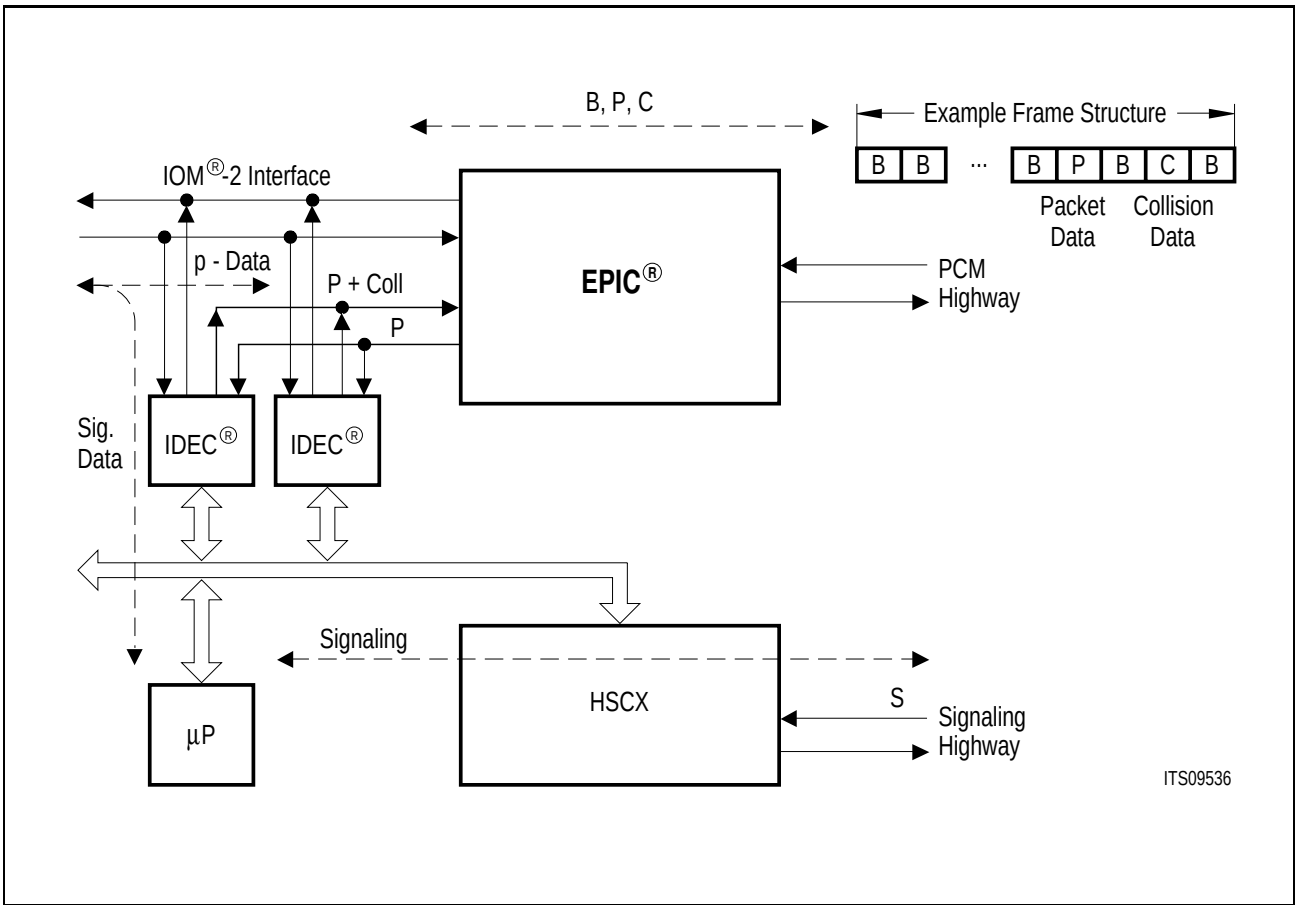


Figure 8
Line Card Architecture for Mixed D-Channel Processing

Alternatively, the packet and collision data can be directly exchanged between the IDECs and the PCM-highway. Thus, the full 32 subscriber switching capability of the EPIC is retained.

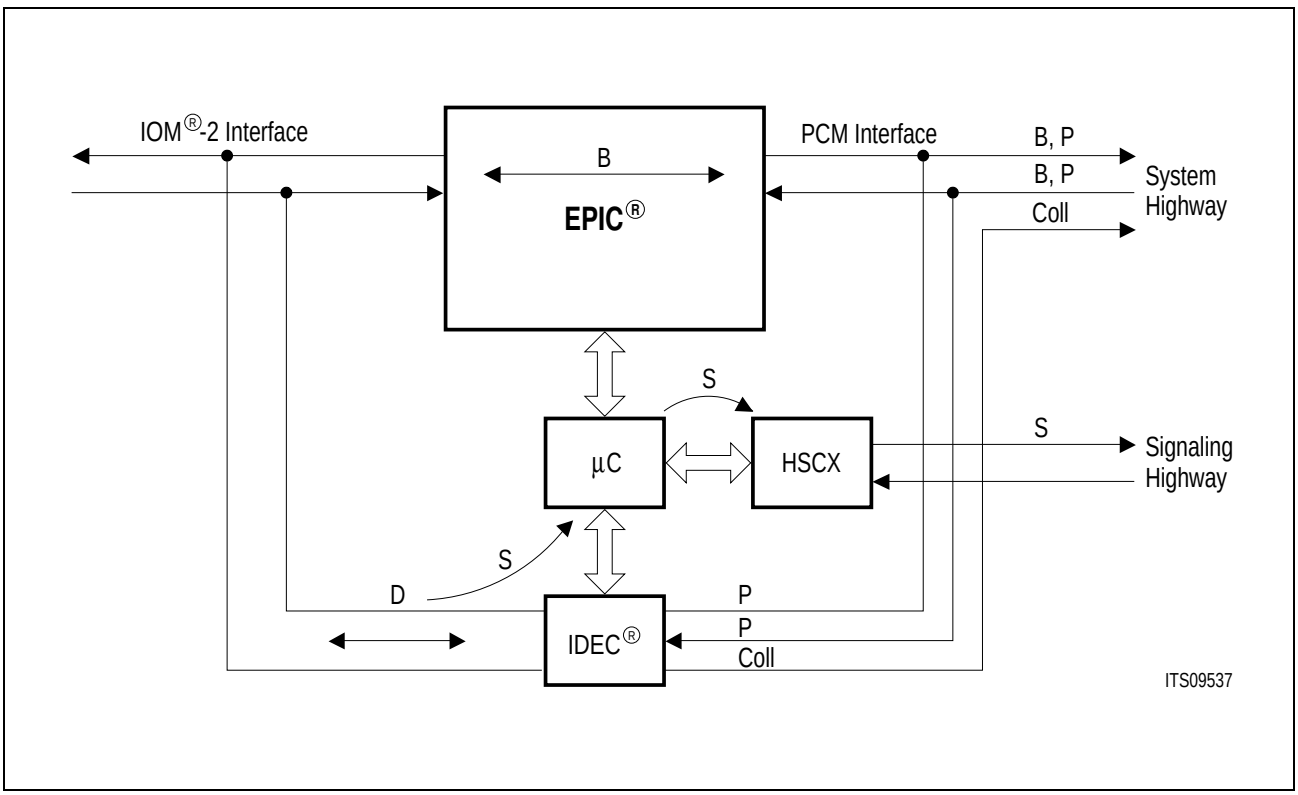


Figure 9
Line Card Architecture for Mixed D-Channel Processing

1.7.2 Analog Line Card

Together with the highly flexible Siemens codec filter circuits SLICOFI, SICOFI, SICOFI-2 or SICOFI-4 the EPIC constitutes an optimized analog subscriber board architecture.

The EPIC-1 handles the signalling and voice data for up to 64 subscriber channels with 64 kbit/s. The HSCX establishes the link to the group controller board.

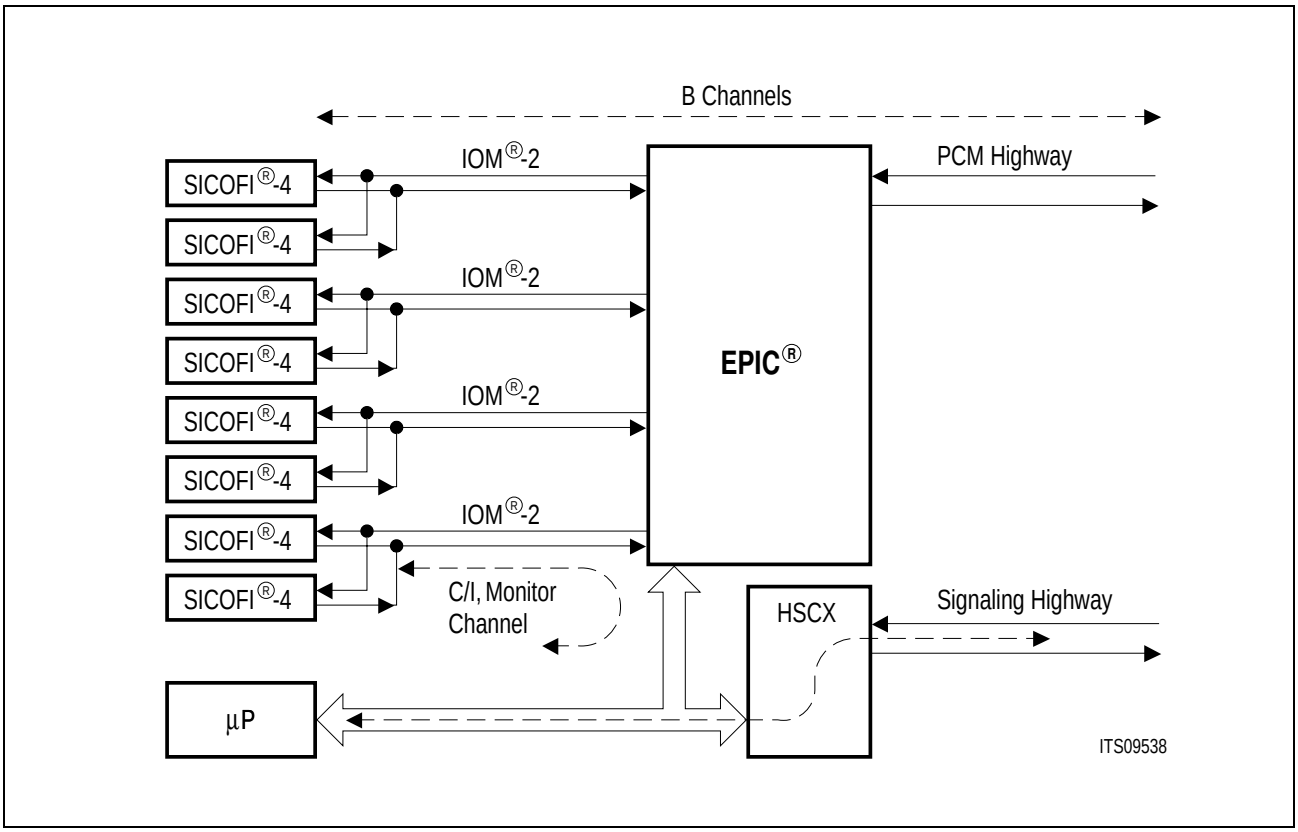


Figure 10
Line Card Architecture for Analog Subscribers

1.7.3 Packet Handlers

The EPIC is an important building block for networks based on either central, decentral or mixed signaling and packet data handling architectures. Its flexibility allows for the modification of the packet handling architecture according to the changing needs.

Thus it may be useful to add central packet handling groups to a network originally based on decentral signaling and packet handling. This may be the case if growing data packet traffic exceeds the initial capacity of the network. The result is a mixed architecture.

On the other hand, increasing packet handling demand on a few dedicated subscriber lines calls for solutions which back up the capacity at these few decentral line cards.

In both of these cases and several other applications, the EPIC is a powerful device for solving the problem of packet handling. In most applications it is used together with the IDEC (ISDN D channel Exchange Controller).

Decentralized and mixed packet handling has already been covered in the line card chapter. In the following, the centralized signaling/packet handlers built up with the EPIC will be described.

Central packet handling is used if many subscribers with a generally low demand for packet switching are to be connected to a system. Concentrating the packet servers for multiple users eliminates the need to provide a packet server channel for every user. The overall number of packet server channels can thus be reduced.

In such a central packet handling group, the EPIC performs the switching and concentrator function. It connects a variable number of PCM highways to the packet handler internal highway. HDLC controllers are also connected to this internal highway as illustrated in **figure 11**.

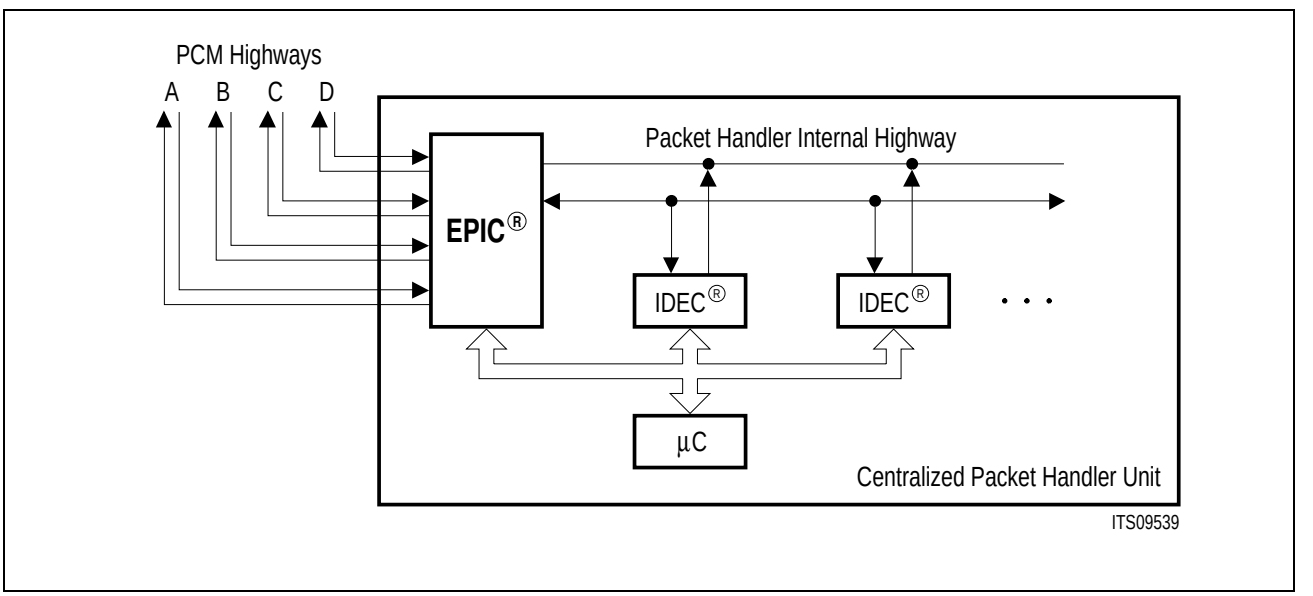


Figure 11
Centralized Packet Handler with a Single Internal Highway Connected to 4 PCM Highways

This figure shows one EPIC connecting four PCM highways to one packet handler internal highway. These highways are accessed by the IDECs, which are 4 channel HDLC controller and handle the packets. If more than four PCM highways shall be connected to the centralized packet handler, further EPICs are necessary. Such a configuration is shown in **figure 12**, where 8 highways are switched to one packet handler internal highway. In this case the two EPICs are connected in parallel at the packet handlers internal side.

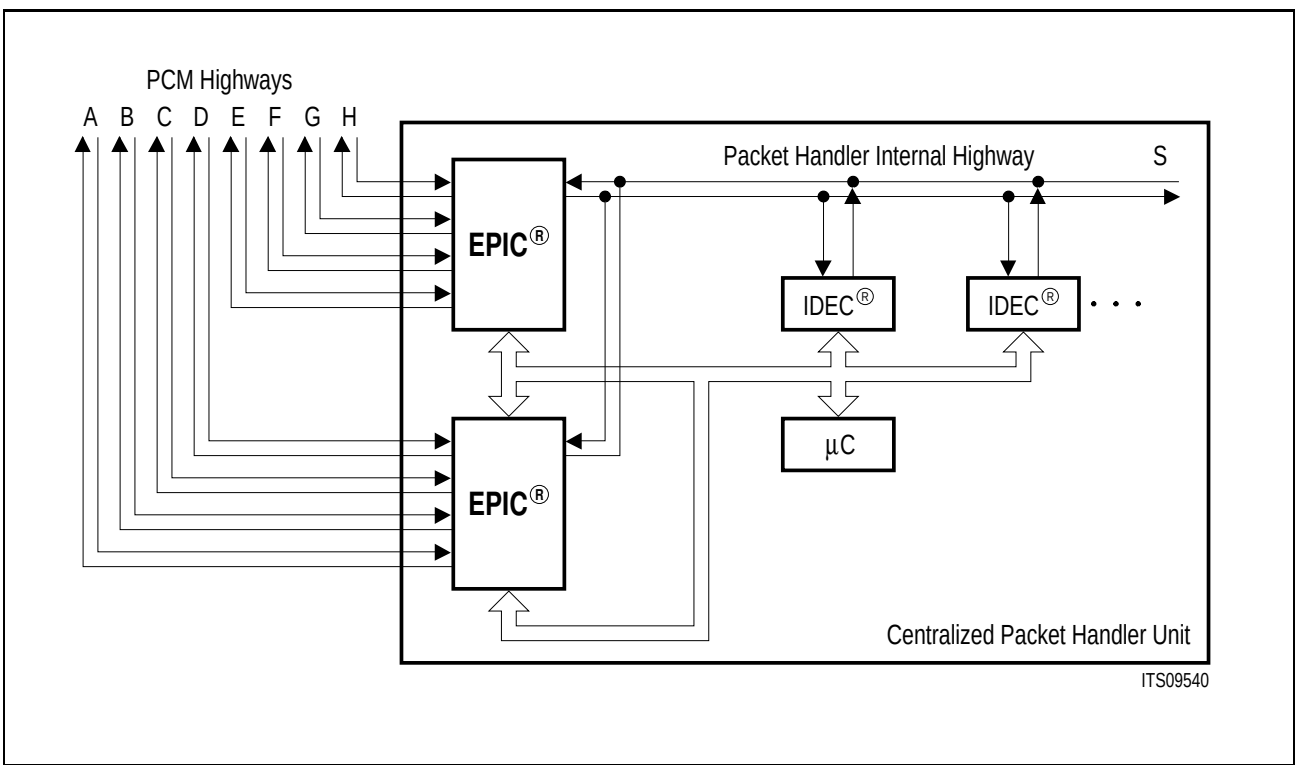


Figure 12
Centralized Packet Handler with One Internal Highway Connected to 8 PCM Highways

The data rate of the packet handler internal highway can be up to 4.096 Mbit/s. If this capacity is not sufficient, other packet handler internal highways may be added as depicted in **figure 13**.