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SIEMENS

ICs for Communications

Extended Line Card Interface Controller
ELIC®

PEB 20550
PEF 20550

Versions 1.3

User's Manual 01.96

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Edition 01.96

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PEB 20550 **PEF 20550** **Revision History:**		**User's Manual 01.96**
Previous Release:		Technical Manual 9.93
Page (in Previous Release)	Page (in User's Manual)	Subjects (major changes since last revision)
–	13	PEF 20550 (ext. temperature range; new)
–	38	System Integration and Application (DECT added)
29	46	Boundary scan number 22 = 110 (correction)
29	46	Boundary scan number 9: ID code for V1.3 added
31	49	Boundary scan ID code for V1.3 added
–	57	DMA-transfers, figure 31 (new)
–	60	Support of the HDLC protocol by SACCO, figure 35 (new)
51	76	SACCO clock mode 2 description (extended)
53	80	Extensions for V1.3
55	82	Arbiter state machine description (extended)
58	85	Table 14: Control channel delay examples (extended)
65	95	Internal reference clock RCL replaced by CFI reference clock CRCL
–	101	Interrupt driven transmission sequence example, figure 50 (new)
82	114	Internal reference clock RCL replaced by CFI reference clock CRCL
85	118	Register address arrangement (extended)
–	129	EMOD: ECMD2 restriction 5 (new)
93	130	PMOD: PMD1..0 description (data rate stepping corrected)
101	140	CMD2: CXF, CRR description (corrected)
104	144	MACR description (extended)
114	154	TIMR: SSR (correction)
121	162	VNSR: VN3..0 = V1.2 (correction)
124	167	EXIR: XMR description (extended)
128	172	CCR1: ODS description (extended for V1.3)
132	177	SACCO RSTA: C/R description (new)
140	185	VSTR: VN3..0 value for V1.3 added
142	187	SCV: SCV7...0 description (extended)
–	191	Application Hints (new)
148	380	$t_{ALS\ min}$ = 8 ns, $t_{DRH\ max}$ = 65 ns, $t_{AH\ min}$ = 0 ns (correction)
–	395	Package outlines (new)
–	396	Appendix (new)

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1 Overview

The PEB 20550 (**E**xtended **Li**ne Card **C**ontroller) is a highly integrated controller circuit optimized for line card and key system applications. It combines all functional blocks necessary to manage up to 32 digital (ISDN or proprietary) or 64 analog subscribers.

The switching and layer-1 control capability of the EPIC-1 (PEB 2055) constitutes a major functional block of the ELIC.

For layer-2 support, two independent Special Application Communication Controllers (SACCO) are available. One typically handles the communication with the group controller, the other is used to serve the subscriber terminals. A D-channel arbiter is employed to multiplex the HDLC controller between multiple subscribers while maintaining full duplex signaling protocols (e.g. LAPD).

Additionally, typical line card glue logic functions such as a power-up reset generator, a watchdog timer and two parallel ports are integrated.

The ELIC is implemented in a Siemens advanced 1.0-µm CMOS-technology and manufactured in a P-MQFP-80-1 package.

The ELIC is a member of a new chip family supporting D-channel multiplexing on the line card and in the subscriber terminal. This concept allows an highly economical implementation of digital subscriber lines.

Chip Family

Line Cards:

PEB 20550	Extended Line Card Controller	(ELIC)
PEB 2096	Octal U_{PN} Transceiver	(OCTAT-P)
PEB 2095	ISDN Burst Transceiver Circuit	(IBC)
PEB 2084	QUAD S_0 Transceiver	(QUAT-S)
PEB 2465	QUAD DSP based Codec Filter	(SICOFI-4)
PEB 2075	ISDN D-Channel Exchange Controller	(IDEC)

Terminals:

PSB 2196	Digital Subscriber Access Controller for U_{PN} Interface	(ISAC-P TE)
PEB 2081 (V3.2)	S/T-Bus Interface Circuit Extended	(SBCX)

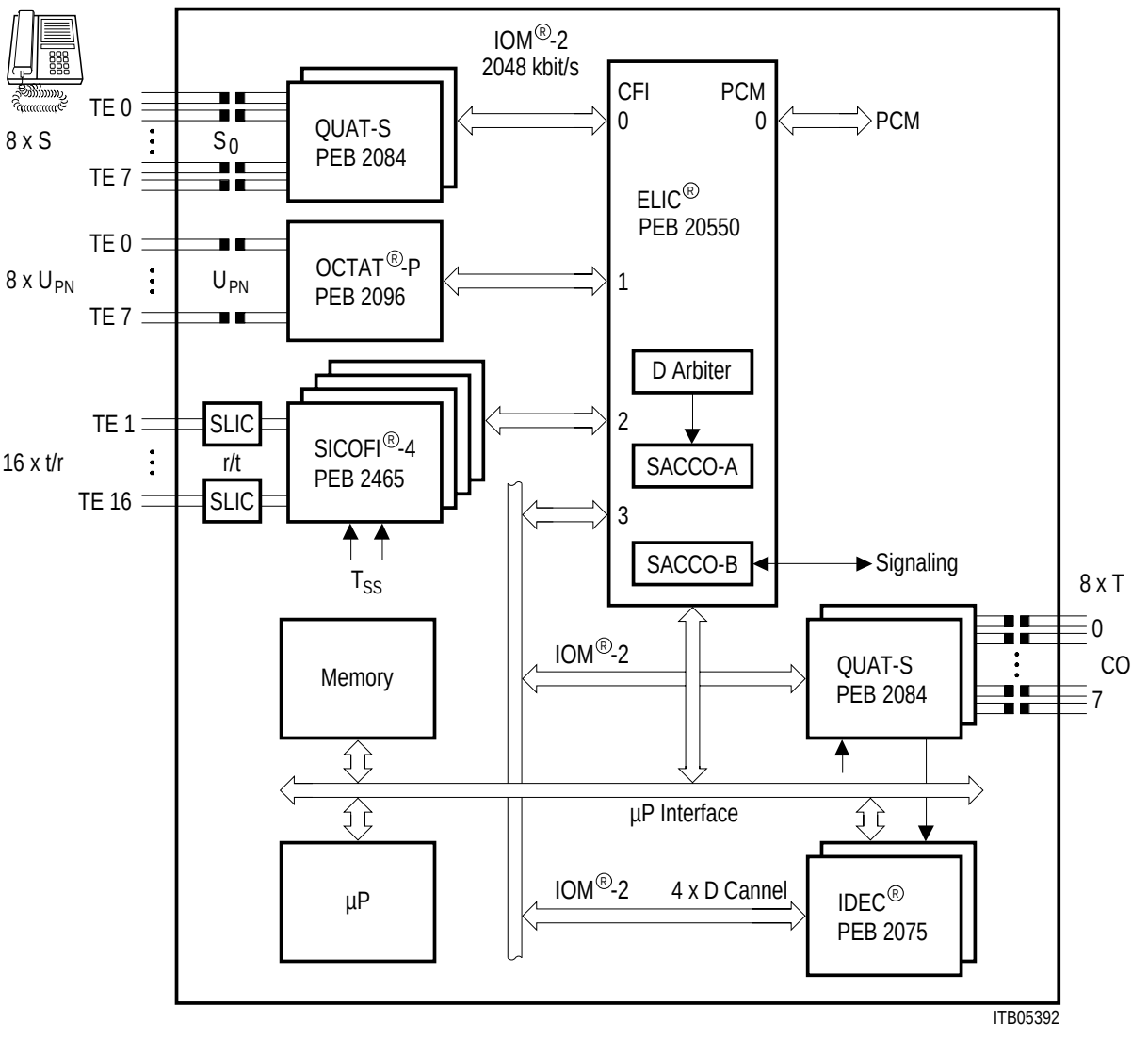

Figure 1
Example for an Integrated Analog / Digital PBX

SIEMENS

Extended Line Card Interface Controller ELIC®

PEB 20550
PEF 20550

Versions 1.3 **CMOS**

1.1 Features

P-MQFP-80-1

Switching (EPIC®-1)

- Non-blocking switch for 32 digital (e.g. ISDN) or 64 voice subscribers
  - Bandwidth 16, 32, or 64 kbit/s
  - Two consecutive 64-bit/s channels can be switched as a single 128-kbit/s channel
- Freely programmable time slot assignment for all subscribers
- Synchronous µP-access to two selected channels
- Two types of serial interfaces independently programmable over a wide data range (128 - 8192 kbit/s)
  - PCM-interface
    Tristate control signals for external drivers
    Programmable clock shift
    Single or double data clock
  - Configurable interface
    Configurable for IOM-, SLD- and PCM-applications
    High degree of flexibility for datastream adaption
    Programmable clockshift
    Single or double data clock

Type	Ordering Code	Package
PEB 20550	Q67101-H6484	P-MQFP-80-1 (SMD)
PEF 20550	Q67101-H6605	P-MQFP-80-1 (SMD)

Handling of Layer-1 Functions (EPIC®-1)

- Change detection for C/I-channel (IOM-configuration) or feature control (SLD-configuration)
- Additional last-look logic for feature control (SLD-configuration)
- Buffered monitor (IOM-configuration) or signaling channel (SLD-configuration)

Handling of Layer-2 Functions (SACCO)

- Two independent full duplex HDLC-channels
  - Serial interface
    Data rate up to 4 Mbit/s
    Independent time slot assignment for each channel with programmable time slot length (1-256 bits)
    Support of bus configuration with collision resolution
    Continuous transmission of 1 to 32 bytes possible
  - Protocol support
    Auto-mode, fully compatible to PEB 2050 (PBC) protocol
    Non-auto mode, address recognition capability
    Transparent mode, HDLC-framing only
    Extended transparent mode, fully transparent without HDLC-framing
  - 64-bytes FIFO’s per HDLC-channel and direction

D-channel Multiplexing (D-channel arbiter)

- Serving of multiple subscribers with one HDLC-controller
- Full duplex signaling protocols (e.g. LAPD or proprietary) supported
- Programmable priority scheme
- Broadcast transmission

Line Card Glue Logic

- Power-up reset generator
- Watchdog timer
- Parallel ports (8-bit input, 4-bit I/O)

Boundary Scan Support

- Fully IEEE 1149.1 compatible
- 32-bit device identification register

Bus Interface

- Siemens/Intel or Motorola type µP-interface
- 8-bit demultiplexed bus interface
- FIFO-access interrupt or DMA controlled

1.2 Pin Configuration

(top view)

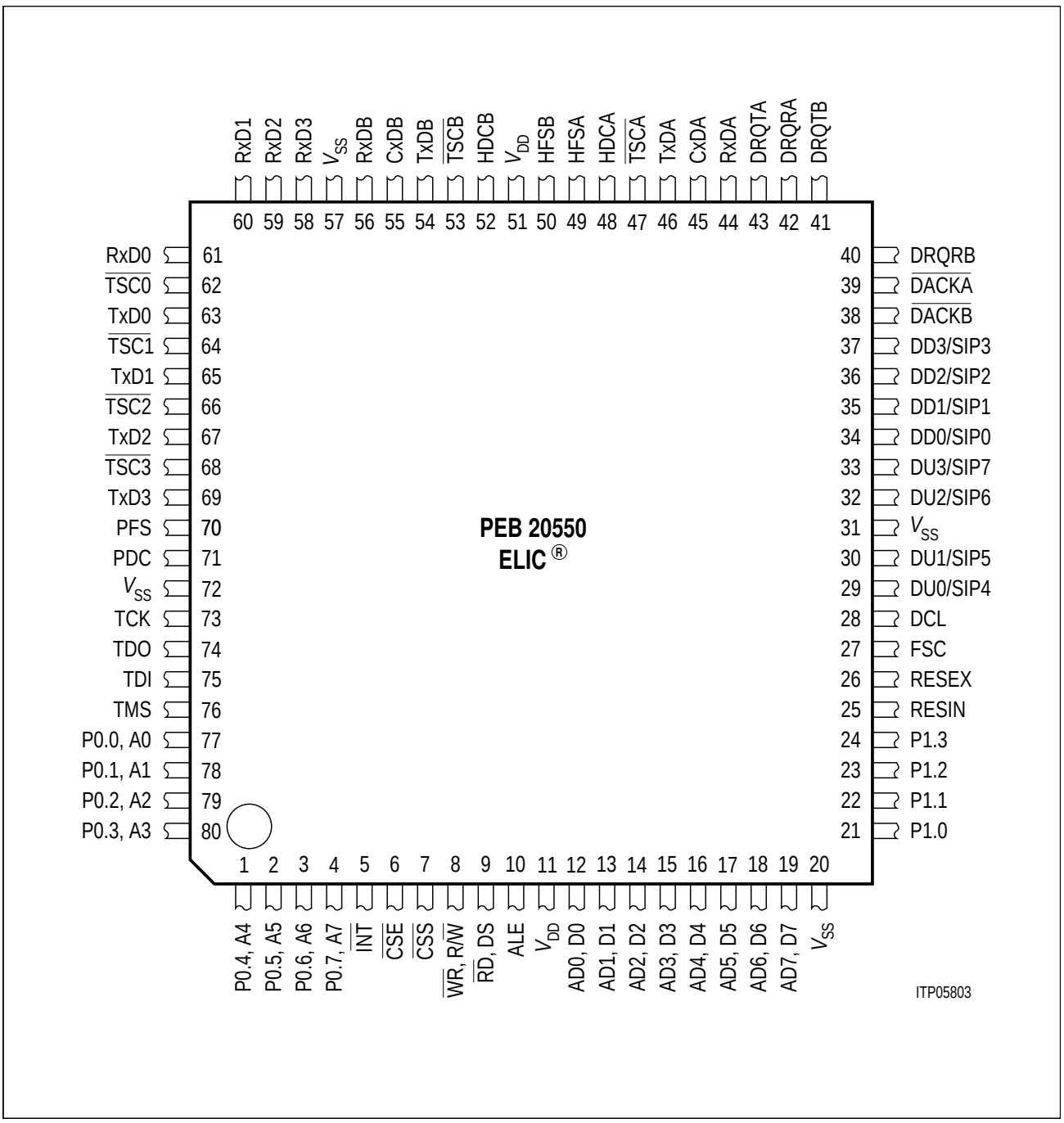

Figure 2

1.3 Pin Definitions and Functions

µ-Processor Interface

Pin No.	Symbol	Input (I) Output (O)	Function
6	$\overline{\text{CSE}}$	I	**C**hip **S**elect **EPIC-1**; active low. A "low" on this line selects all registers (excluding the SACCO-registers) for read/write operations.
7	$\overline{\text{CSS}}$	I	**C**hip **S**elect **SACCO**; active low. A "low" on this line selects the SACCO-registers for read/write operations.
8	$\overline{\text{WR}}$, R/$\overline{\text{W}}$	I	**W**rite, active low, Siemens/Intel bus mode. When "low", a write operation is indicated. **R**ead/**W**rite, Motorola bus mode. When "high" a valid µP-access identifies a read operation, when "low" it identifies a write access.
9	$\overline{\text{RD}}$, DS	I	**R**ead, active low, Siemens/Intel bus mode. When "low" a read operation is indicated. **D**ata **S**trobe, Motorola bus mode. A rising edge marks the end of a read or write operation.
12 13 14 15 16 17 18 19	AD0, D0 AD1, D1 AD2, D2 AD3, D3 AD4, D4 AD5, D5 AD6, D6 AD7, D7	I/O I/O I/O I/O I/O I/O I/O I/O	**A**ddress/**D**ata **B**us; multiplexed bus mode. Transfers addresses from the µP-system to the ELIC and data between the µP and the ELIC. **D**ata **B**us; demultiplexed bus mode. Transfers data between the µP and the ELIC. **When driving data the pins have push pull characteristic, otherwise they are in the state high impedance.**
10	ALE	I	**A**ddress **L**atch **E**nable ALE controls the on chip address latch in multiplexed bus mode. While ALE is "high", the latch is transparent. The falling edge latches the current address. During the first read/write access following reset ALE is evaluated to select the bus mode.

Pin Definitions and Functions (cont'd)

µ-Processor Interface

Pin No.	Symbol	Input (I) Output (O)	Function
77 78 79 80 1 2 3 4	P0.0,A0 P0.1,A1 P0.2,A2 P0.3,A3 P0.4,A4 P0.5,A5 P0.6,A6 P0.7,A7	I I I I I I I I	**A**ddress **B**us, demultiplexed bus mode. Transfers addresses from the µP-system to the ELIC. **P**ort **0**, multiplexed bus mode. Parallel input port. The current data is latched with the falling edge of $\overline{RD}$, DS.
21 22 23 24	P1.0 P1.1 P1.2 P1.3	I/O I/O I/O I/O	**P**ort **1** 4-bit I/O port. Every pin can be configured individually as input or output. For inputs the current data is latched with the falling edge of $\overline{RD}$, DS.
5	$\overline{INT}$	O (OD)	**I**nterrupt **R**equest, active low. This signal is activated when the ELIC requests an interrupt. Due to the open drain (OD) characteristic of $\overline{INT}$ multiple interrupt sources can be connected together.
25	RESIN	O	**R**eset **I**ndication This pin is set to "high", when the ELIC executes either a power-up reset, a watchdog timer reset, an external reset (RESEX) or a software system reset.
26	RESEX	I	**R**eset **E**xternal A "high" forces the ELIC into reset state.

Pin Definitions and Functions (cont'd)

EPIC®-1 Interface

Pin No.	Symbol	Input (I) Output (O)	Function
70	PFS	I	**PCM**-**I**nterface **F**rames **S**ynchronization
71	PDC	I	**PCM**-**I**nterface **D**ata **C**lock Single or double data rate.
61 60 59 58	RxD0 RxD1 RxD2 RxD3	I I I I	**R**eceive **PCM**-**I**nterface **D**ata Time-slot oriented data is received on this pins and forwarded into the downstream data memory of the EPIC-1.
63 65 67 69	TxD0 TxD1 TxD2 TxD3	O O O O	**T**ransmit **PCM**-**I**nterface **D**ata Time-slot oriented data is shifted out of the EPIC-1s upstream data memory on this lines. **For time-slots which are flagged in the tristate data memory or when bit OMDR:PSB is reset the pins are set in the state high impedance.**
62 64 66 68	$\overline{\text{TSC0}}$ $\overline{\text{TSC1}}$ $\overline{\text{TSC2}}$ $\overline{\text{TSC3}}$	O O O O	**T**ristate **C**ontrol Supplies a control signal for an external driver. These lines are "low" when the corresponding TxD-outputs are valid. During reset these lines are "high".
27	FSC	I/O	**F**rame **S**ynchronization Input or output in IOM-configuration. Direction indication signal in SLD-mode.
28	DCL	I/O	**D**ata **C**lock Input or output in IOM, slave clock in SLD configuration. In IOM-configuration single or double data rate, single data rate in SLD-mode.

Pin Definitions and Functions (cont'd)

EPIC®-1 Interface

Pin No.	Symbol	Input (I) Output (O)	Function
29 30 32 33	DU0/SIP4 DU1/SIP5 DU2/SIP6 DU3/SIP7	I/IO (OD) I/IO (OD) I/IO (OD) I/IO (OD)	**D**ata **U**pstream Input; IOM- or PCM-configuration. **S**erial **I**nterface **P**ort, SLD-configuration. **Depending on the bit OMDR:COS these lines have push pull or open drain characteristic. For unassigned channels or when bit OMDR:CSB is reset the pins are in the state high impedance.**
34 35 36 37	DD0/SIP0 DD1/SIP1 DD2/SIP2 DD3/SIP3	O/IO (OD) O/IO (OD) O/IO (OD) O/IO (OD)	**D**ata **D**ownstream Output, IOM- or PCM-configuration. **S**erial **I**nterface **P**ort, SLD-configuration. **Depending on the bit OMDR:COS these lines have push pull or open drain characteristic. For unassigned channels or when bit OMDR:CSB is reset the pins are in the state high impedance.**

Pin Definitions and Functions (cont'd)

SACCO-Interface

Pin No.	Symbol	Input (I) Output (O)	Function
49 50	HFSA HFSB	I I	**H**DLC-Interface **F**rame **S**ynchronization Channel **A**/**B** Frame synchronization pulse in clock mode 2, data strobe in clock mode 1.
48 52	HDCA HDCB	I I	**H**DLC-Interface **D**ata **C**lock **C**hannel **A**/**B**. Single or double data rate.
44 56	RxDA RxDB	I I	**R**eceive **S**erial **D**ata **HDLC**-**C**hannel **A**/**B** The serial data received on this lines is forwarded into the corresponding HDLC-receive channel. Data is sampled on the – falling edge of HDC (CCR2:RDS = 0) or – rising edge of HDC (CCR2:RDS = 1).
46 54	TxDA TxDB	O (OD) O (OD)	**T**ransmit **S**erial **D**ata **HDLC**-**C**hannel **A**/**B**. Data output lines of the corresponding HDLC-transmit channel. **Depending on the bit CCR1:ODS the pins have push pull or open drain characteristic. When transmission is disabled ($\overline{\text{TSCA}}$ or B = 1) or when bit CCR2:TXDE is reset the pins are in the state high impedance.**
47 53	$\overline{\text{TSCA}}$ $\overline{\text{TSCB}}$	O O	**T**ristate **C**ontrol **HDLC**-**C**hannel **A**/**B**, active low. Supplies a control signal for an external driver. When low the corresponding TxD-outputs are valid. The detailed functionality is defined programming the SACCO-registers CCR2:SOC1,SOC0. During reset these lines are high.
45 55	CxDA CxDB	I I	**C**ollision **D**ata **HDLC**-**C**hannel **A**/**B** In a bus configuration, the external serial bus must be connected to the respective CxD-pin for collision detection. In point-to-point configurations the pin provides a "clear to send" function. When '0'/'1' the transmit channel is enabled/disabled. **If this function is not needed CxDA/B has to be tied to V_{SS}.**

Pin Definitions and Functions (cont'd)

SACCO-Interface

Pin No.	Symbol	Input (I) Output (O)	Function
42 40	DRQRA DRQRB	O O	**DMA**-**R**equest **R**eceiver **C**hannel **A**/**B** The receiver of HDLC-channel **A**/**B** requests a DMA-data transfer by activating this lines. The DRQR-pin remains "high" as long as the receiver FIFO requires data transfers. Only blocks of 32, 16, 8 or 4 bytes are transferred.
43 41	DRQTA DRQTB	O O	**DMA**-**R**equest **T**ransmitter **C**hannel **A**/**B** The transmitter of HDLC-channel **A**/**B** requests a DMA-data transfer by activating this lines. The DRQT-pin remains "high" as long as the transmit FIFO requires data transfers. The number of data bytes to be transferred from system memory to the FIFO must be written first into the XBCH, XBCL registers (byte count registers).
39 38	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I I	**DMA**-**A**cknowledge **HDLC**-Channel **A**/**B**, active low. When "low", this lines notifies the HDLC-channel, that the requested DMA-cycle is in progress. Together with $\overline{\text{RD}}$ (DRQR) or $\overline{\text{WR}}$(DRQT) $\overline{\text{DACK}}$ works like $\overline{\text{CS}}$ to enable a read or write operation to the top of the receive or the transmit FIFO. When $\overline{\text{DACK}}$ is active, the address lines are ignored and the FIFOs are implicitly selected. When $\overline{\text{DACK}}$ is not used it has to be connected to V_{DD}.

Pin Definitions and Functions (cont'd)

Boundary Scan Interface, according to IEEE Std. 1149.1

Pin No.	Symbol	Input (I) Output (O)	Function
76	TMS	I (internal pull-up)	**T**est **M**ode **S**elect A 0 -> 1 transition on this pin is required to step through the TAP-controller state machine.
75	TDI	I (internal pull-up)	**T**est **D**ata **I**nput In the appropriate TAP-controller state test data or a instruction is shifted in via this line
74	TDO	O	**T**est **D**ata **O**utput In the appropriate TAP-controller state test data or a instruction is shifted out via this line.
73	TCK	I	**T**est **C**lock Single rate test data clock.

Note: Pin 75 (TDI) and pin 76 (TMS) are internally connected to V_{DD} via pull-up resistors.

1.4 Logic Symbol

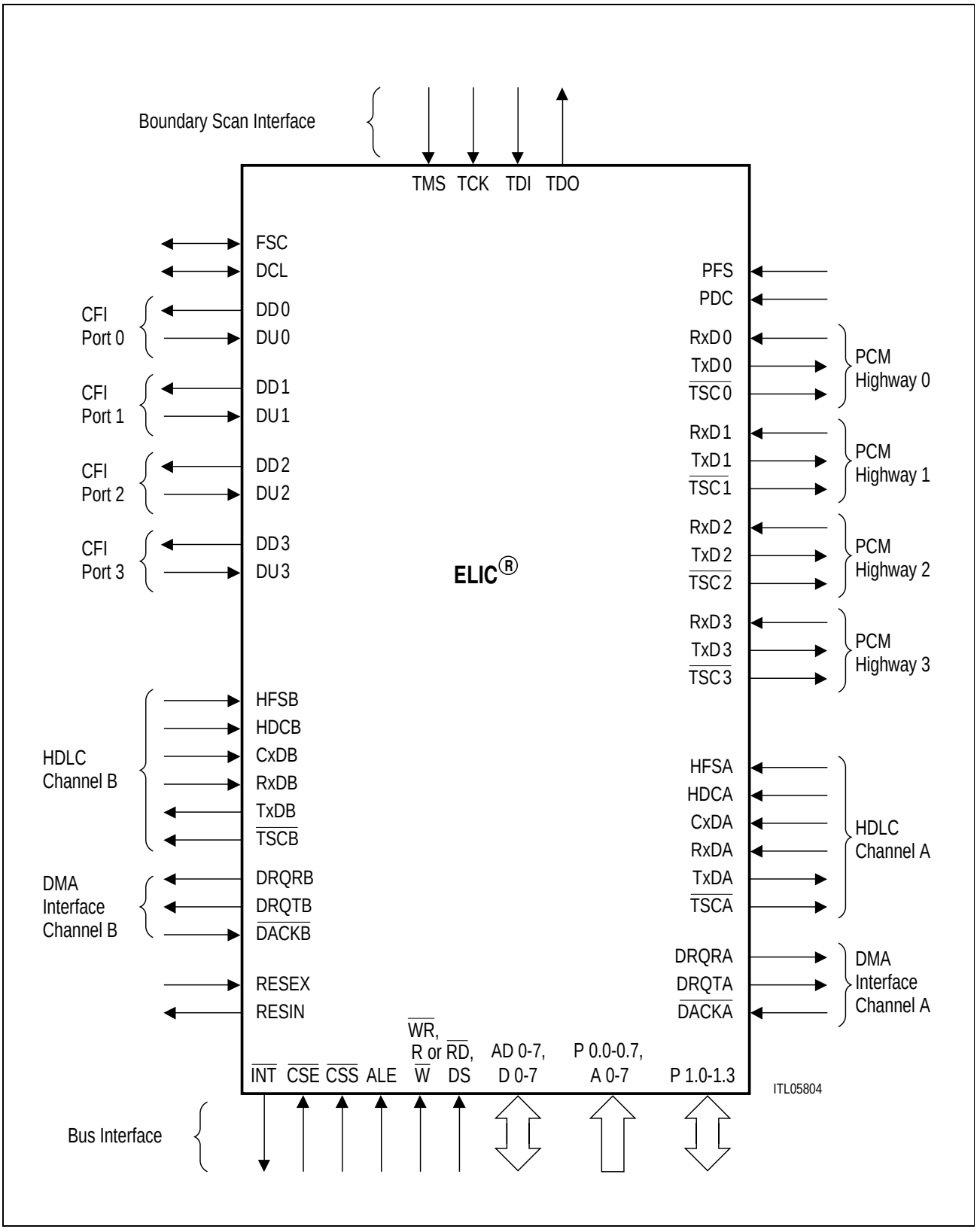

Figure 3

1.5 Functional Block Diagram

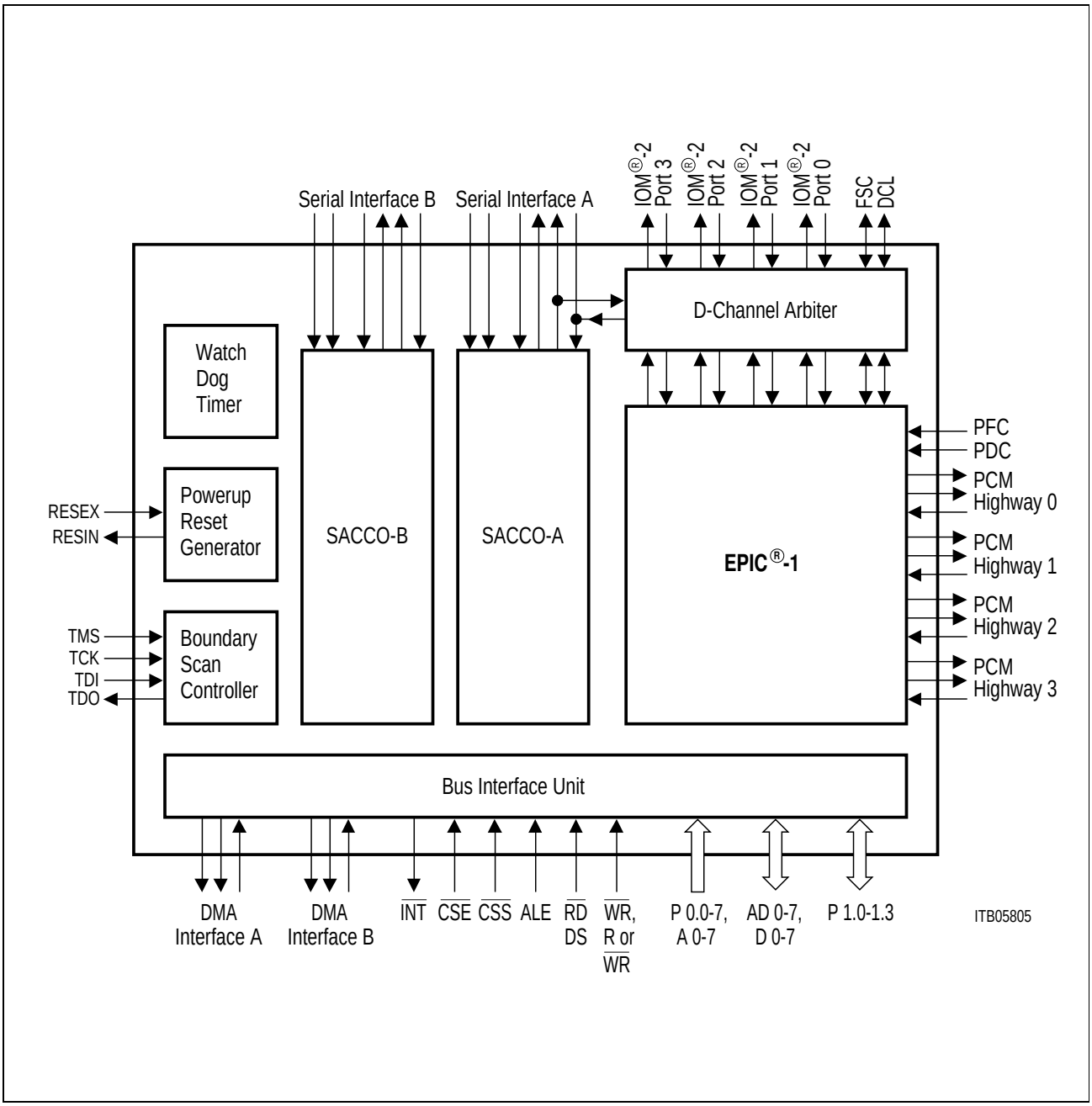

Figure 4

1.6 System Integration and Application

The main application fields of the ELIC are:

- Digital line cards, different architectures are supported,
- Central control units of key systems,
- Analog line cards,
- DECT line cards.

1.6.1 Digital Line Card

1.6.1.1 Switching, Layer-1 Control, Group Controller Signaling

The ELIC performs a switching capability for up to 32 digital subscribers between the PCM- system highway and the IOM-2 interface (64 B-channels). Typically it switches 64-kbit/s channels between the PCM and the IOM-interfaces. Moreover it is able to handle also 16-, 32- and 128-kbit/s channels.

The signaling handler supports the command/indication (C/I) channel which is used to exchange predefined layer-1 information with the transceiver device.

A monitor handler supports the handshake protocol defined on the IOM-monitor channel. It allows programming of layer-1 devices which do not have a dedicated µP interface.

The communication between the line card and the group controller is performed by one of the SACCO-channels. Its auto-mode is optimized for this application and implements a slave station behaviour in normal response mode. The auto-mode is compatible with the PBC (PEB 2050) but due to the large FIFO-size the response time requirements compared to the PBC are reduced drastically.

The data exchange between the line card and the group controller board can take place on a separate signalling highway or on the PCM-highway (due to the time slot capability of the SACCO) (see **figure 5**).