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Data Sheet, Rev. 2, July 2004

SIDEC

Smart Integrated Digital Echo Canceller

PEF/PEB 20954 HT, Version 1.1

PEF/PEB 20954 E, Version 1.1

Wireline Communications

Infineon technologies

Never stop thinking.

Edition 2004-07-28

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Revision History:	**2004-07-28**	Rev. 2
Previous Version:	**Data Sheet, DS1, 1999-04**	

Page	Subjects (major changes since last revision)
Changes from previous version DS3, 2003-06-01 to DS4, 2003-09-01	
Page 141	timing t_smon_delay
	document rearranged
	Additional configuration hints in the **“Operational Description” on Page 51** and following pages

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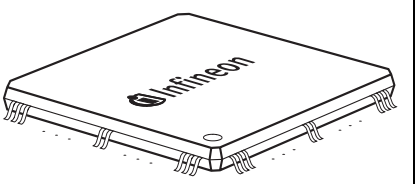
1 Introduction

The **S**mart **I**ntegrated **D**igital **E**cho **C**anceller (SIDEC) suppresses echoes in telecommunication networks which might disturb any kind of terrestrial or wireless communication. It incorporates leading edge CMOS technology as well as INFINEON's' many years' experience in Telecommunication ICs.

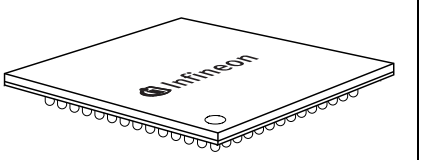
In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscribe loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone system. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T (International Telecommunications Union, Telecommunication Standardization Sector) suggests in the recommendation G.131 the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

Version 1.1

1.1 Key Features



P-TQFP-144-6, -8, -14



P-LFBGA-160-2

- 2.048 MHz PCM input and output interfaces with selectable µ- and A-Law coding according to ITU G.711
- Rapid convergence of patented algorithm at the beginning or during a connection even in the presence of background noise at the near end subscriber
- Echo return loss enhancement of > 30 dB (ERLE)
- Detection of double talk for adaptive convergence control
- Independently controlled voiceband echo cancelling according to ITU G.165 and G.168 for
  - 32 channels with end echo path delay of less than 63.75 ms
  - 16 channels with end echo path delay of less than 127.75 ms (usage of two SIDEC in parallel for simultaneous processing of 32 channels is easily possible)
- Smart Non Linear Processor controlled by echoloss, echo path delay and background noise
- Various options for comfort noise injection
- Maskable disabling functions
  - 2100 Hz tone with phase reversal detection
  - 2100 Hz tone without phase reversal detection
  - 2010 Hz continuity check (SS7)
  - via PCM timeslot 16 Bit a, b, c or d according to ITU G.704
  - individual channels maskable via Microprocessor Interface, UCC Interface and Serial Interface

Type	Package
PEF/PEB 20954 HT	P-TQFP-144-8
PEF/PEB 20954 E	P-LFBGA-160-2

- Integrated Universal Control and Communication Interface (UCCI) for signaling highways with direct hardware control for:
  - disable cancelling
  - configurable disabling functions
  - communication between board controllers
- Support of Channel Associated Signaling (CAS) BR transparency (robbed bits) in send path
- Selectable µ- to A-Law or A- to µ-Law Conversion on a global or per channel basis
- Configurable idle channel supervision
- Clear channel capability (64 clear) on a per channel basis
- Special evaluation of bit 8 in T1 Modem calls possible (56 clear)
- Serial 256 kbit/s interface to control the functions disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control or combinations of above
- Monitor pins for several internal states
- Switchable global loop from receive output to send input and send output to receive input
- Switchable global attenuation (2.5 dB or 6 dB) at the receive and send output
- Flexible Microprocessor Interface (Intel or Motorola type, Mux and Demux mode) usable for:
  - configuration of parameters such as thresholds and functions on a global basis
  - Disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control (all functions individually for each channel)
  - support of background tests for disabled or idle timeslots (feeding and reading of test levels)
  - possibility to read levels, attenuations, internal states, signal values or all coefficients of a selected timeslot
  - control of the RAM Built In Self Test
- Advanced Integrated Watchdog Timer
- Supervision of the input clocks
- Various clock modes possible for 32.768 MHz and 8.192 MHz
- Boundary Scan according to IEEE 1149.1 Standard
- Power supply: 3.3 V, 5V tolerant inputs
- Typical power dissipation: 900 mW
- Plastic package P-TQFP 144-8, P-LFBGA 160-2
- Temperature range: -40°C - 85°C and 0°C - 70°C

Ordering Information

Table 1 Ordering Information

Product	Package	Q-Number
PEB 20954 HT	**P-TQFP 144-8** (0°C - 70°C)	Q67003 H9363
PEF 20954 HT	**P-TQFP 144-8** (-40°C - 85°C)	Q67003 H9364
PEB 20954 E	P-LFBGA-160-2 (0°C - 70°C)	Q67003 H9422
PEF 20954E	P-LFBGA-160-2 (-40°C - 85°C)	Q67003 H9423

1.2 Logic Symbol

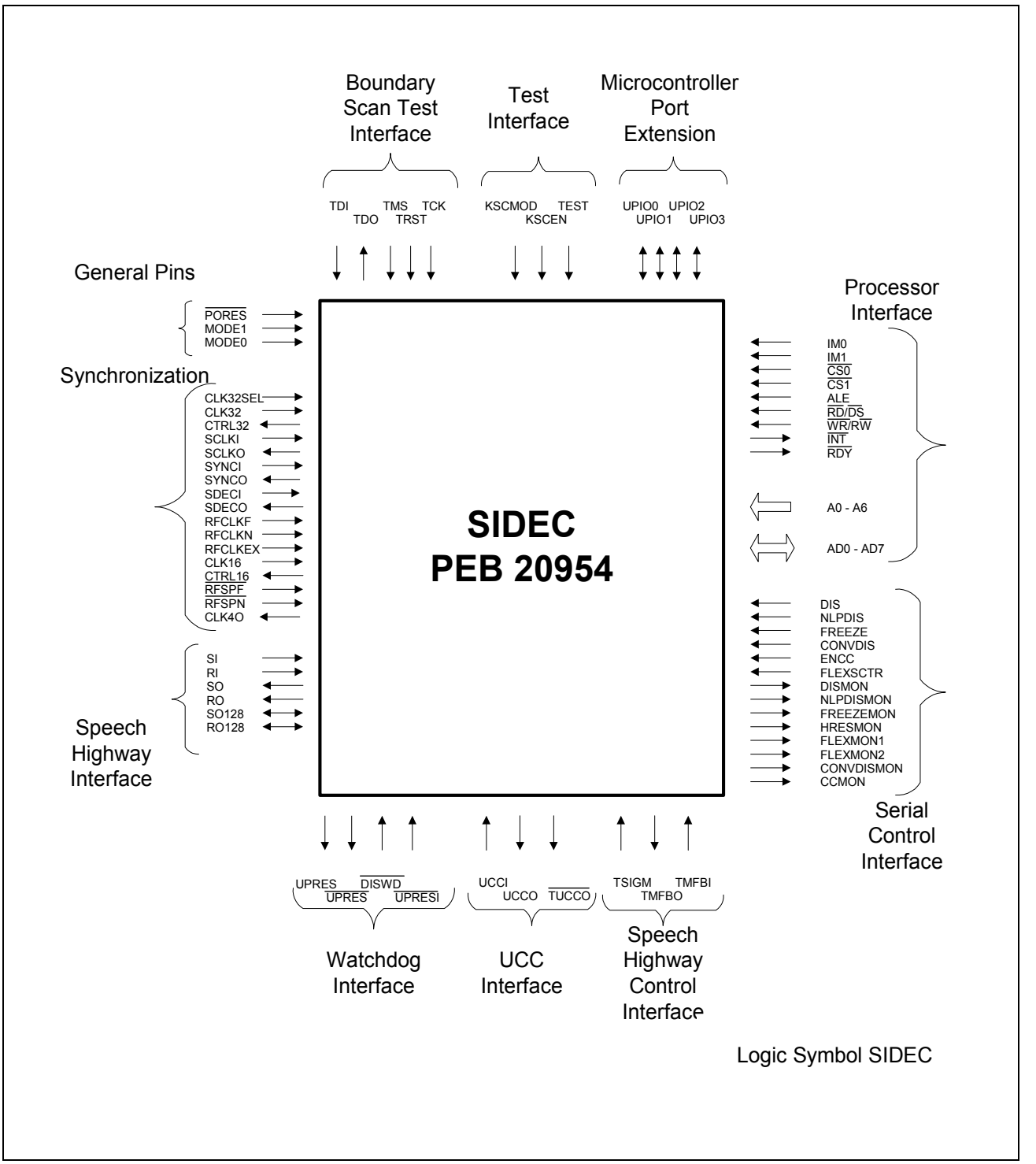


Figure 1 Logic Symbol of the SIDEC

1.3 Typical Applications

The SIDEC can be used for various applications.

Figure 2 to **Figure 5** display typical examples.

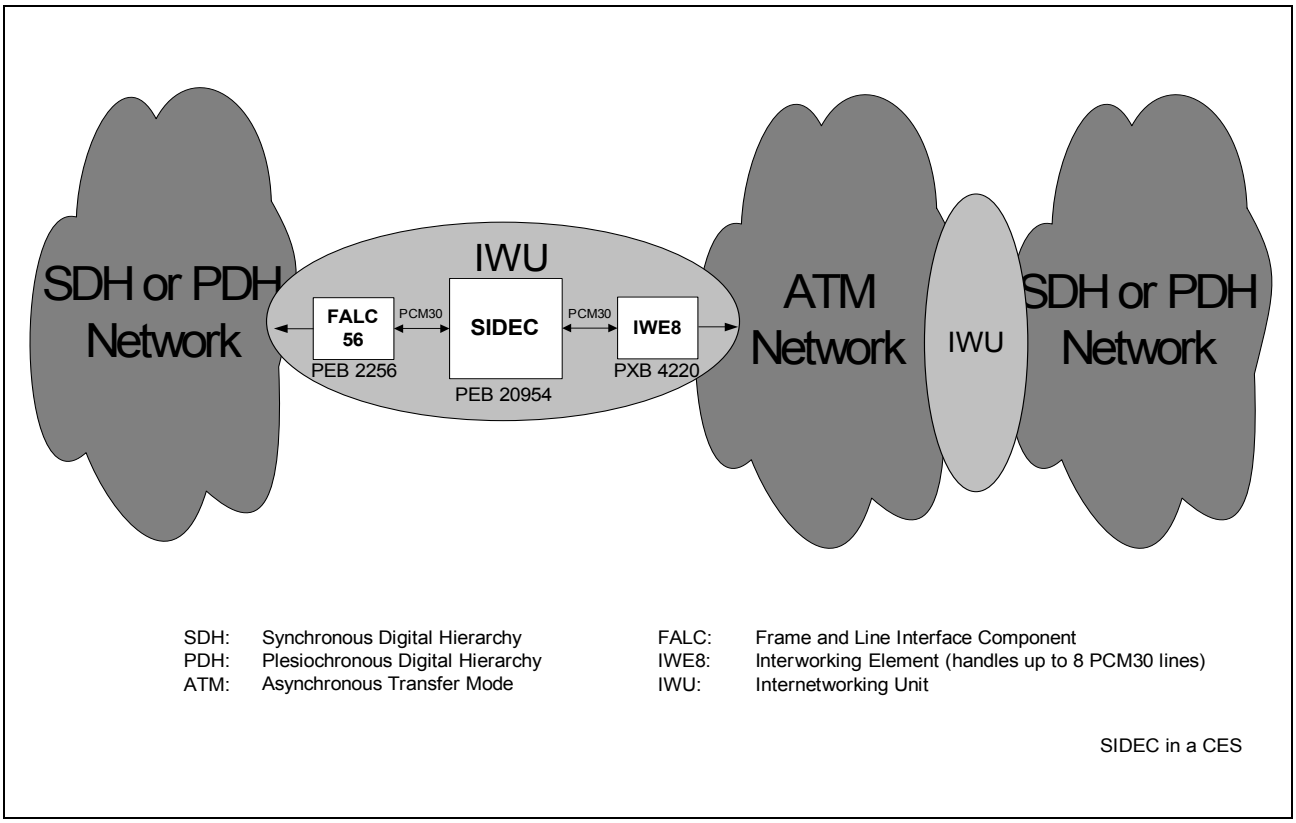


Figure 2 SIDEC in a Circuit Emulation Service Carried over ATM

In this interworking unit there are two INFINEON products connected to the SIDEC. The FALC 56 serves as a frame and line interface component whereas the IWE8 PXB 4220 operates as an interworking element.

The delays of networks and the inter working units are usually long. In the application above the SIDEC cancels the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEC can cancel end echo paths (SDH or PDH Network on near end side) up to 128 ms. For details see **Figure 17**.

For the set up illustrated in **Figure 2** a application note "Using SIDEC in a Voice over ATM Application" is available.

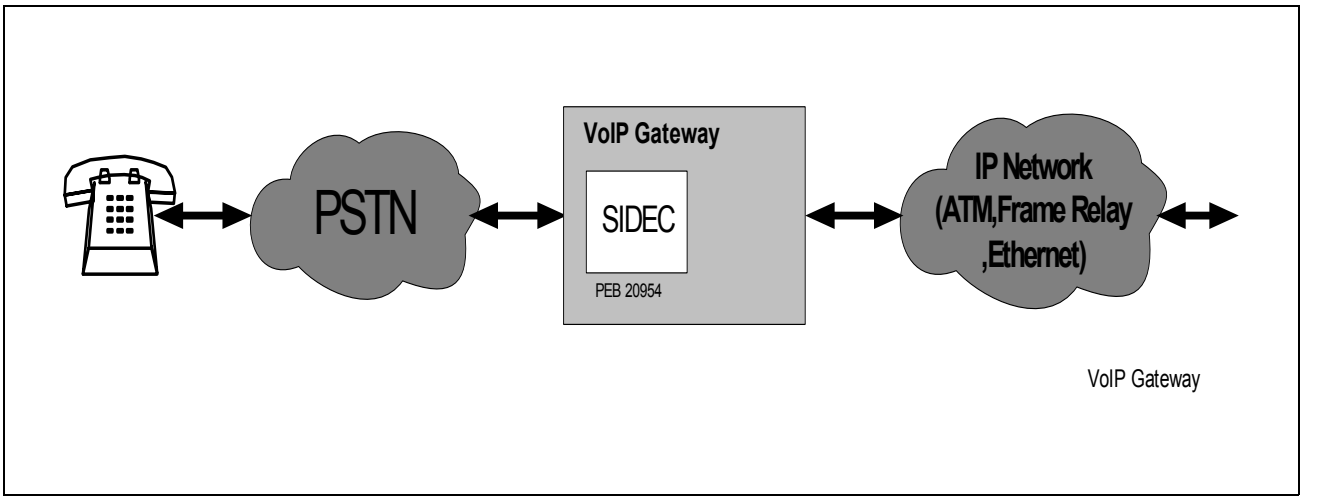


Figure 3 SIDEC in a Voice over IP Gateway

An emerging market in the telecom industry is “Voice Over IP”. Due to the long delay echo cancellation is required. The delay is introduced through packetizing and voice compression. The SIDEC handles different functions in a Voice over IP gateway, such as Voice Detection, Voice Activity Detection, Comfort Noise and A-law u-law conversion regarding G.711.

In a gateway the SIDEC points into the PSTN network as shown in **Figure 3**. The echo itself is generated by the hybrid in the PSTN cloud. Before the voice signal from the POTS gets packetized into ATM, FR or Ethernet cells the echo is being cancelled by the SIDEC.

For a high voice quality in “Voice Over IP” environment echo cancellation is a major requirement.

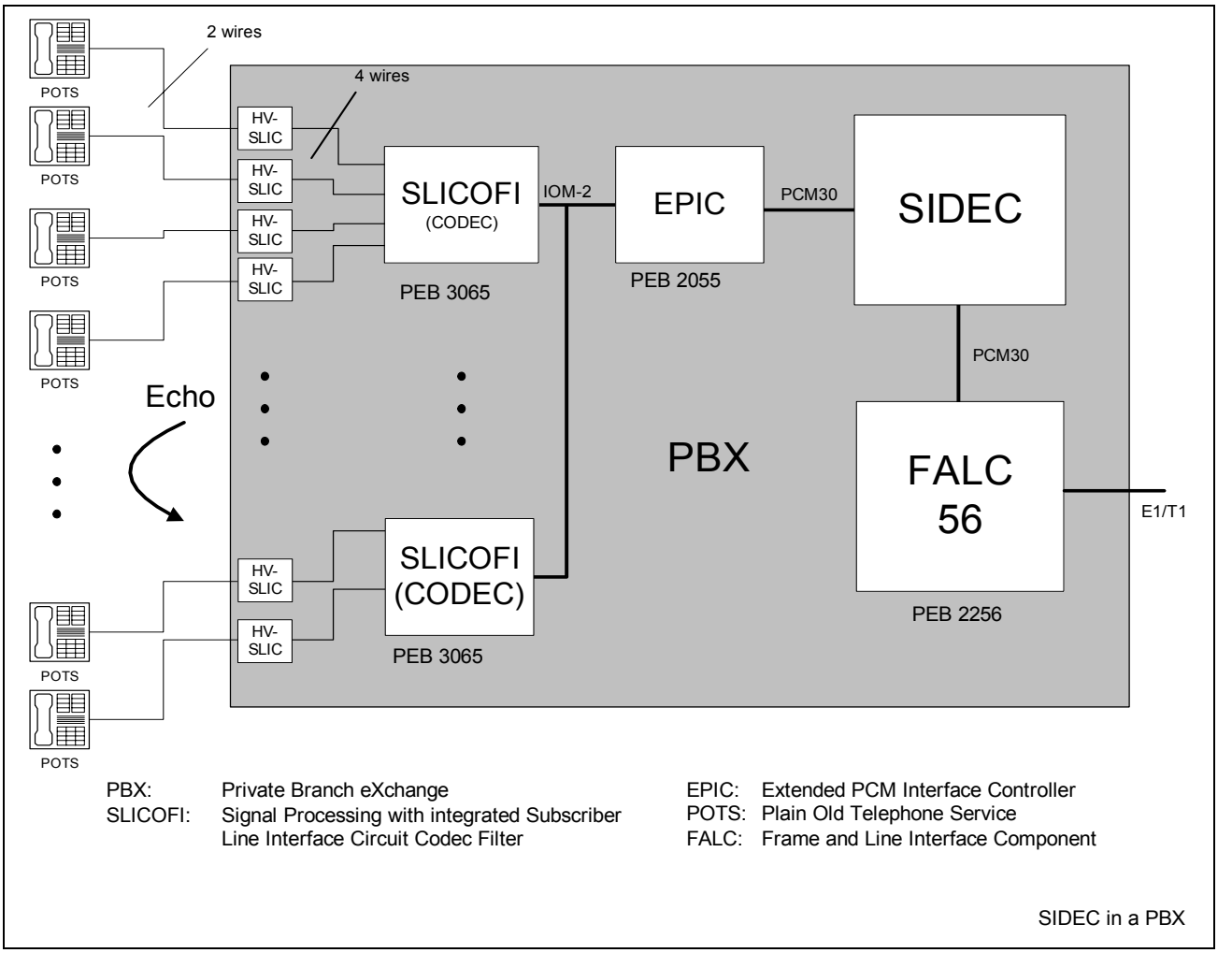


Figure 4 SIDEC in a Private Branch Exchange (PBX)

SIDEC can be used in a PBX or Central Office (CO) to cancel the echo next to the customer side (near end echo). The echo delay is kept short. The delay for this application is usually less than 64ms and the SIDEC can cancel up to 32 channels.

Figure 4 shows a PBX with a T1/E1 interface FALC LH to the CO on the one side. On the other side analog phones are connected.

A possible INFINEON solution with the SICOFI (includes D/A and A/D conversion) and the SLIC (hybrid) to connect the analog phone is shown above.

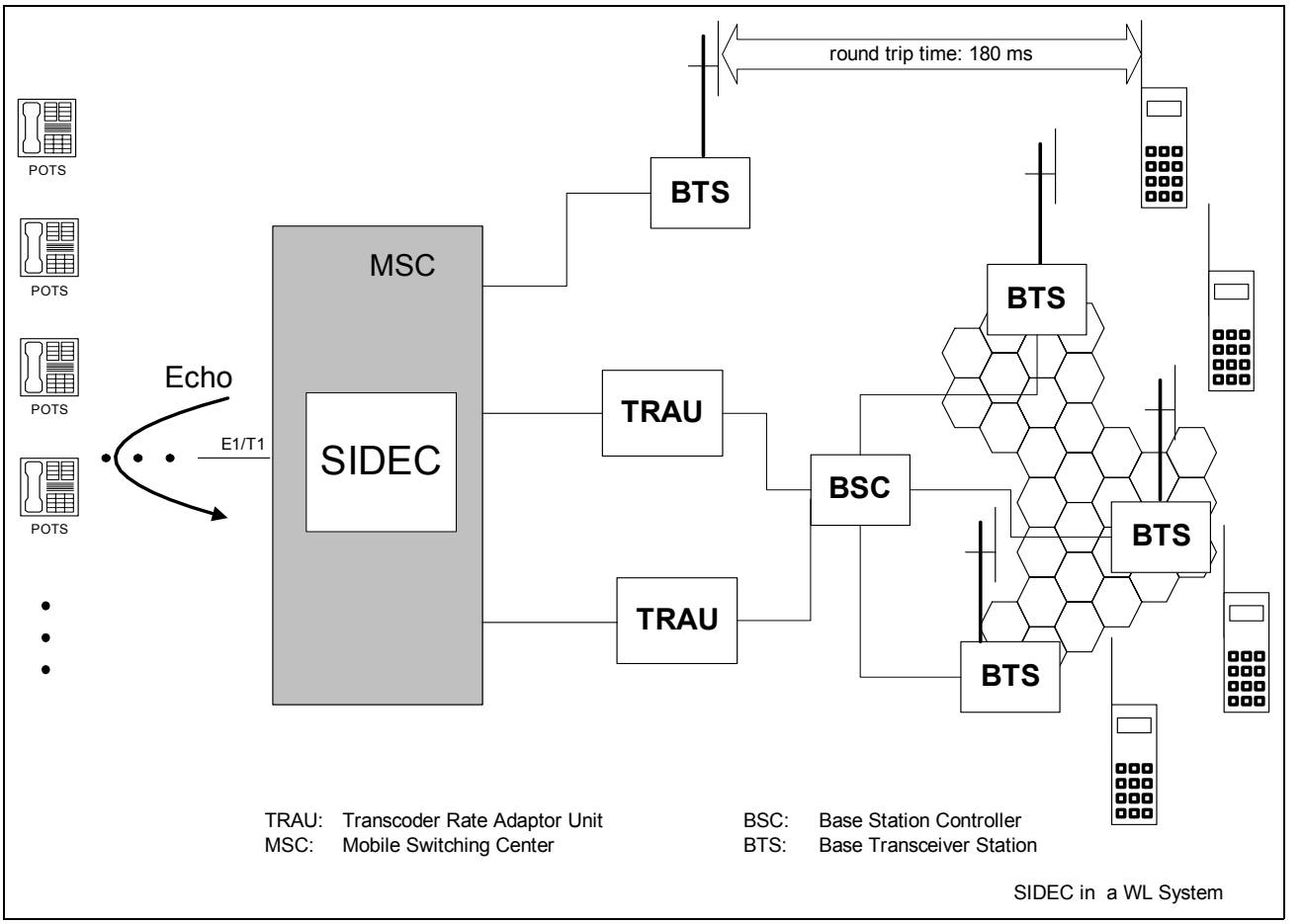


Figure 5 SIDEC in a Wireless System

Due to voice compression and error correction the one way transmission time for wireless voice signals is typically 90 ms. With 180 ms roundtrip time the 50 ms roundtrip time for echo free transmission is exceeded by at least 130 ms. Hence, the speaker on the mobile phone will hear any kind of echo generated in the hybrid next to the POTS or the acoustical echo of the POTS. The SIDEC suppresses those two kinds of echoes if it is incorporated in the MSC. Depending on the individual call the end echo path can differ dramatically. In Europe the end echo path could even go to different countries causing strong dispersion of the echo. Only a high quality echo canceller with long end path delay options guarantees compensation of the strongly varying echoes.

2 Pin Description

2.1 Pin Diagram

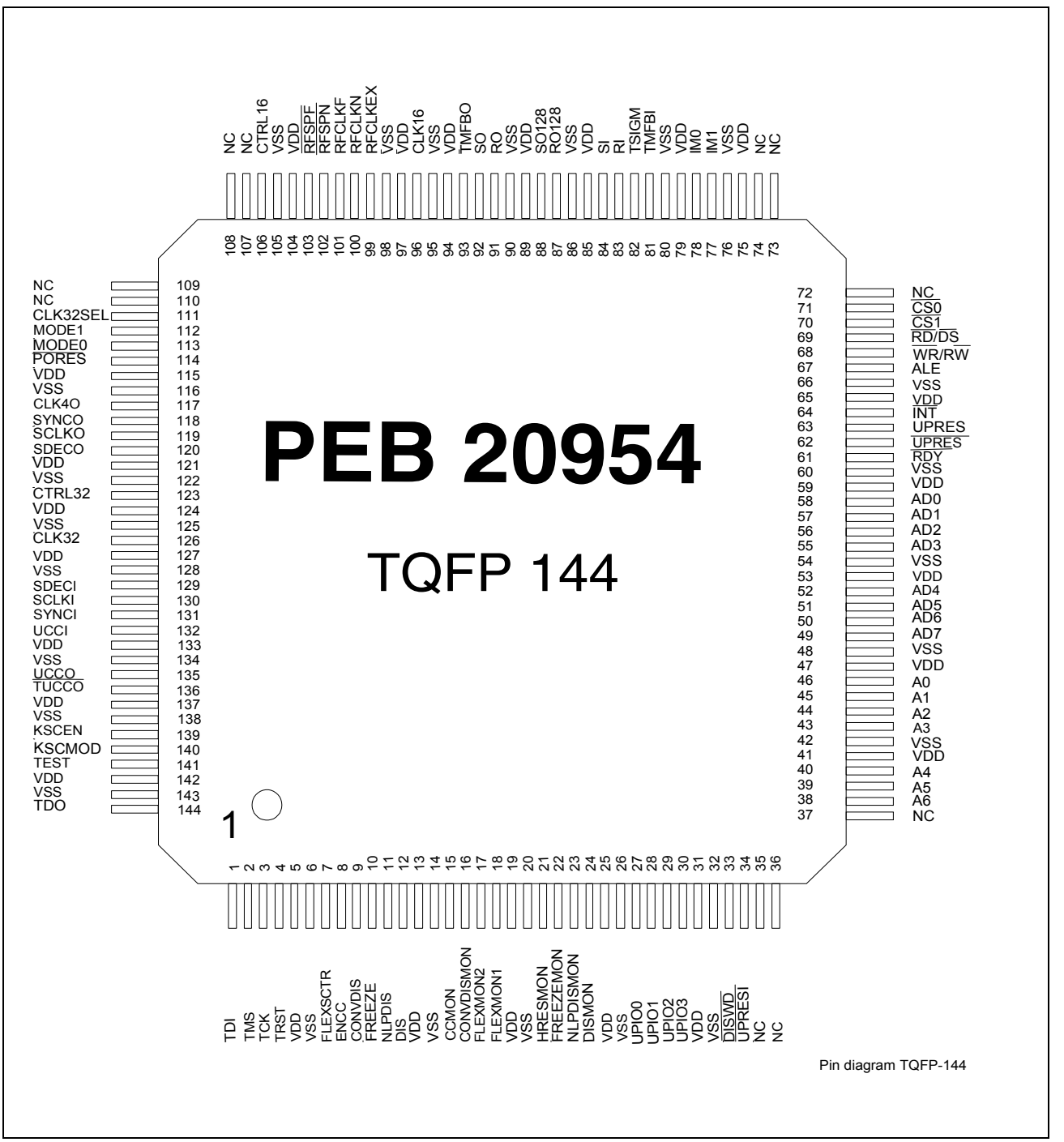
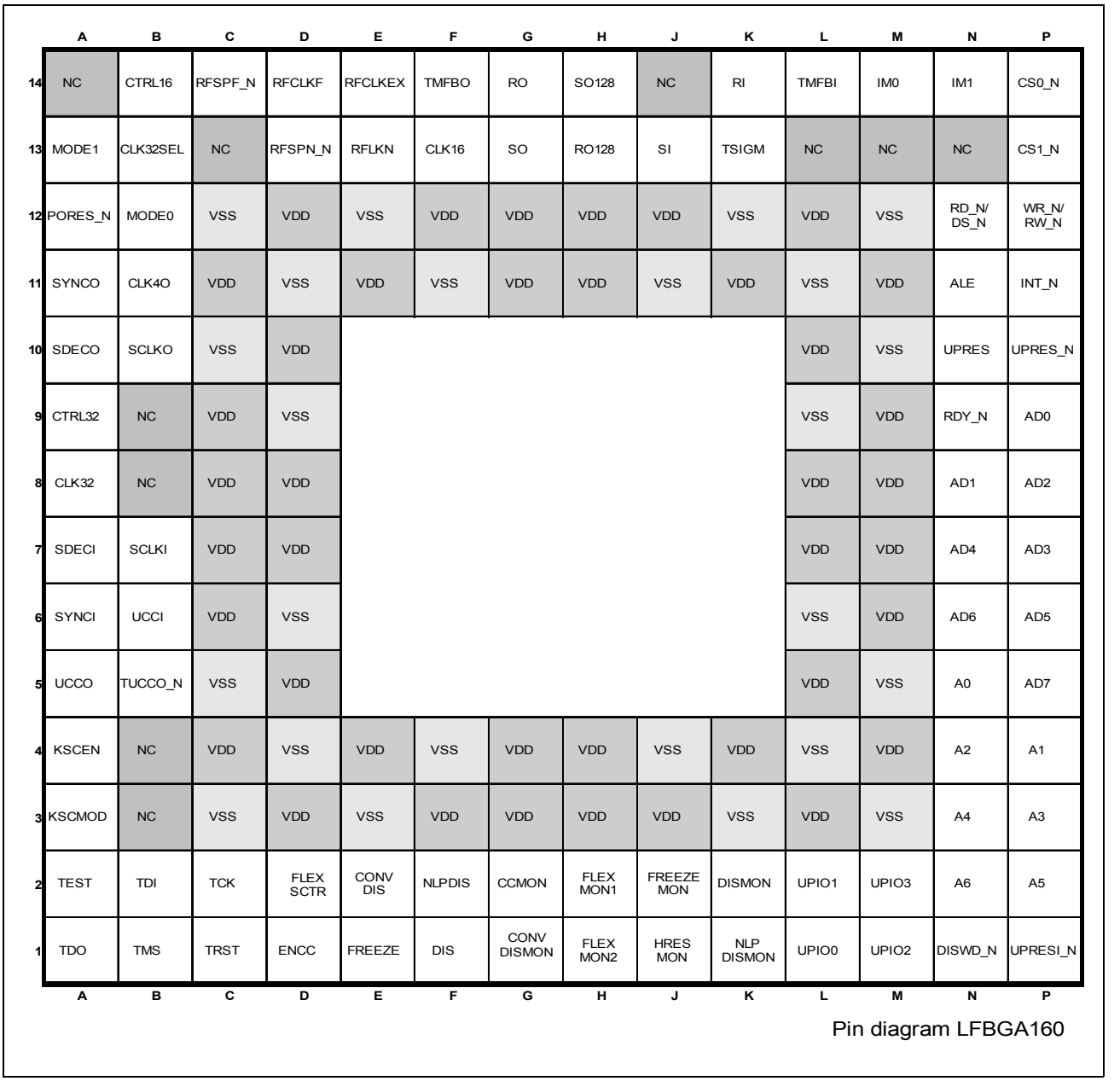


Figure 6 Pin Configuration P-TQFP-144-8



	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	NC	CTRL16	RFSPF_N	RFCLKF	RFCLKEX	TMFBO	RO	SO128	NC	RI	TMFBI	IM0	IM1	CS0_N
13	MODE1	CLK32SEL	NC	RFSPN_N	RFLKN	CLK16	SO	RO128	SI	TSIGM	NC	NC	NC	CS1_N
12	PORES_N	MODE0	VSS	VDD	VSS	VDD	VDD	VDD	VDD	VSS	VDD	VSS	RD_N/ DS_N	WR_N/ RW_N
11	SYNCO	CLK4O	VDD	VSS	VDD	VSS	VDD	VDD	VSS	VDD	VSS	VDD	ALE	INT_N
10	SDECO	SCLKO	VSS	VDD							VDD	VSS	UPRES	UPRES_N
9	CTRL32	NC	VDD	VSS							VSS	VDD	RDY_N	AD0
8	CLK32	NC	VDD	VDD							VDD	VDD	AD1	AD2
7	SDECI	SCLKI	VDD	VDD							VDD	VDD	AD4	AD3
6	SYNCI	UCCI	VDD	VSS							VSS	VDD	AD6	AD5
5	UCCO	TUCCO_N	VSS	VDD							VDD	VSS	A0	AD7
4	KSCEN	NC	VDD	VSS	VDD	VSS	VDD	VDD	VSS	VDD	VSS	VDD	A2	A1
3	KSCMOD	NC	VSS	VDD	VSS	VDD	VDD	VDD	VDD	VSS	VDD	VSS	A4	A3
2	TEST	TDI	TCK	FLEX SCTR	CONV DIS	NLPDIS	CCMON	FLEX MON1	FREEZE MON	DISMON	UPIO1	UPIO3	A6	A5
1	TDO	TMS	TRST	ENCC	FREEZE	DIS	CONV DISMON	FLEX MON2	HRES MON	NLP DISMON	UPIO0	UPIO2	DISWD_N	UPRESI_N
	A	B	C	D	E	F	G	H	J	K	L	M	N	P

Pin diagram LFBGA160

Figure 7 Pin Configuration P-LFBGA-160-2(top view)

2.2 Pin Definitions and Functions for the P-TQFP-144-8 package

Table 2 General Pins

Pin No.	Symbol	Input (I) Output (O) Pull Up / Pull Down	Function			
114	$\overline{\text{PORES}}$	I, PU	Power On Reset. A low on this pin forces all registers and counters to predefined values			
112 113	MODE1 MODE0	I, PU I, PU	1 1	End delay < 64ms	1 0	For future use
112 113	MODE1 MODE0	I, PU I, PU	0 1	End delay < 128 ms Master Mode	0 0	End delay < 128 ms Slave Mode

Table 3 Synchronization

Pin No.	Symbol	I/O, PU/PD	Function
111	CLK32SEL	I, PU	Selects from which source SCLKO will be derived: '1': SCLKO will be derived from CLK32 by dividing by 4 '0': SCLKO will be derived from CLK16 by dividing by 2
126	CLK32	I, PU	32.768 MHz Operating Clock for the SIDEC
123	CTRL32	O	Control voltage for the 32.768 MHz operating Clock VCO, maskable for reduced power consumption
130	SCLKI	I, PU	System clock input (8.192 MHz) for PCM- and UCCI
119	SCLKO	O	8.192 MHz system clock output, source CLK32 or CLK16 is selectable via pin CLK32SEL, maskable for reduced power consumption
117	CLK4O	O	4.096 MHz system clock output for subsequent circuits, derived from SCLKI, maskable for reduced power consumption

Table 3 Synchronization (cont'd)

Pin No.	Symbol	I/O, PU/PD	Function
131	SYNCI	I, PU	System Synchronization input pulse. Defines the frame alignment of PCM and UCCI signals in conjunction with the values in registers RIALIGN, SIALIGN, SOALIGN, UCCALIGN, PHALIGN and also the multiframe alignment of the UCCI. Must be integer multiple of 125 µs if UCC Interface is not used. Must be multiple integer of 4 ms if UCC interface is used. Leave open if not used or connect to V_{DD}
118	SYNCO	O	System Synchronization output pulse (see SYNCI), duration configurable one or two SCLKO periods, period 125 µs. If the UCC interface is not used and no SYNCI is applied, SYNCO can take over the part and role of SYNCI.
120	SDECO	O	Synchronization output pulse for other SIDECs if this SIDEC uses its own 32.768 MHz VCO. Can also be used for synchronization of external devices to the serial control input and monitor output signals of the SIDEC.The pulse width is 488 ns with a period of 125 µs.
129	SDECI	I, PU	Synchronization input pulse if the SIDEC uses the 32.768 MHz VCO of another SIDEC. The same SCLKI signal can be applied to SDECI and SCLKI pin if the SCLKI is supplied by a source with correct phase condition to the CLK32 (see **Figure 15**). If the pin is not used leave it open or connect it to V_{DD}.
101	RFCLKF	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6:5]="00"
100	RFCLKN	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6:5]="01"

Table 3 Synchronization (cont'd)

Pin No.	Symbol	I/O, PU/PD	Function
99	RFCLKEX	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6]='1'
96	CLK16	I, PU	Clock from 16.384 MHz VCXO
106	CTRL16	O	Control voltage for the 16.384 MHz VCXO
103	$\overline{\text{RFSPF}}$	I, PU	Receive Frame Sync Pulse from the far end side (F1). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '0'.
102	$\overline{\text{RFSPN}}$	I, PU	Receive Frame Sync Pulse from the near end side (F2). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '1'.

Table 4 Microprocessor Interface

Pin No.	Symbol	I/O, PU/PD	Function
78	IM0	I, PU	Interface Mode Intel = low, Motorola = high
77	IM1	I, PU	Interface Mode MUXED = low, DEMUXED = high
71	$\overline{\text{CS0}}$	I, PU	Chip Select. A low signal selects the SIDEC (internally "anded" with $\overline{\text{CS1}}$).
70	$\overline{\text{CS1}}$	I, PU	Chip Select. A low signal selects the SIDEC (internally "anded" with $\overline{\text{CS0}}$).
46-43 40-38	A0..A6	I, PU	Address Bus. Only used in demuxed mode, can be left open in muxed mode.
58-55 52-49	AD0..AD7	I/O, -	Multiplexed Address/Data Bus in multiplexed mode, Data Bus in demultiplexed mode

Table 4 Microprocessor Interface (cont'd)

Pin No.	Symbol	I/O, PU/PD	Function
67	ALE	I, PU	Address Latch Enable in multiplexed mode. Address on AD bus is internally latched with the falling edge of ALE.This signal is also used for the internal clock supervision. In Demuxed mode there must be provided an external independent clock signal (i.e. processor clock) in order to enable proper clock supervision.
69	$\overline{RD}/\overline{DS}$	I, PU	Intel mode. A low indicates a read operation. Motorola mode. Data Strobe, active low to control read/write
68	$\overline{WR}/R\overline{W}$	I, PU	Intel mode. A low indicates a write operation. Motorola mode. High = read cycle, low = write cycle
64	$\overline{INT}$	O, (od)	Interrupt request from the SIDEC, active low
61	$\overline{RDY}$	O, (od)	Ready signal for µC devices that support this feature. For read cycles the signal is asserted after the data on the AD bus is valid. For writing cycles the signal is asserted when a write access is ready to be concluded.

Table 5 Microcontroller Port Extension

Pin No.	Symbol	I/O, PU/PD	Function
27	UPIO0	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
28	UPIO1	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
29	UPIO2	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
30	UPIO3	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO