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QuadLIU™

Quad E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications

PEF 22504 E, PEF 22504 HT, Version 2.1

Communications

Never stop thinking

Edition 2006-01-25

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PEF 22504 E, Quad E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications

Revision History: 2006-01-25, Rev. 1.3

Previous Version: Preliminary Data Sheet 2005-11-07	
Chapter, Table	**Subjects (major changes since last revision)**
Chapter 2.3, Chapter 5	The QuadLIU™ is now available in PG-TQFP-144-17 package also

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Preface

The QuadLIU™ is four channel E1/T1/J1 Line interface Component, it is designed to fulfill all required interfacing between four analog E1/T1/J1 lines and four digital framers.

The digital functions as well as the analog characteristics can be configured either via a flexible microprocessor interface, SPI interface or via a SCI interface.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1**, “Introduction”: Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- **Chapter 2**, “Pin Descriptions”: Lists pin locations with associated signals, categorizes signals according to function, and describe signals.
- **Chapter 3**, “Functional Description”: Describes the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation
- **Chapter 4**, “Registers”: Gives a detailed description of all implemented registers and how to use them in different applications/configurations.
- **Chapter 5**, “Package Outlines”: Shows the mechanical characteristics of the device packages.
- **Chapter 6**, “Electrical Characteristics”: Specifies maximum ratings, DC and AC characteristics.
- **Chapter 7**, “Operational Description”: Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).
- **Chapter 8**, “Appendix”: Gives an example for over voltage protection and information about application notes and tool support.

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.231
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETSI ETS 300 233
ETSI TBR12
ETSI TBR13
FCC Part68
H.100
H-MVIP
IEEE 1149.1
TR-TSY-000009
TR-TSY-000253
TR-TSY-000499
ITU-T G.703
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU.T G.733
ITU-T G.775
ITU-T G.823
ITU-T G.824
ITU-T I.431
JT-G703
JT-G704
JT-G706
JT-G33
JT-I431
MIL-Std. 883D
UL 1459

1 Introduction

The QuadLIU™ is the latest addition to Infineon's family of sophisticated E1/T1/J1 Line interface Components. This monolithic four channel device is designed to fulfill all required interfacing between four analog E1/T1/J1 lines and four digital framer interfaces for world market telecommunication systems.

The device is supplied in P/PG-LBGA-160-1 package (P/PG-LBGA-160-1 is RoHS compliant) and in a PG-TQFP-144-17 package, and is designed to minimize the number of external components required, so reducing system costs and board space.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards.

Crystal-less jitter attenuation with only one master clock source reduces the amount of required external components.

Equipped with a flexible microprocessor interface, a SCI and a SPI interface, it connects to various control processor environment. A standard boundary scan interface is provided to support board level testing. LBGA device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

The QuadLIU™ is not hardware and software compatibel to older versions!

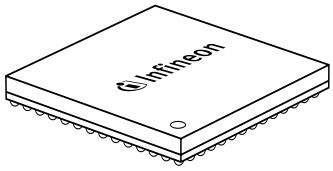
Other members of the FALC® family are the OctalLIU™ supporting eight line interface components on a single chip, the OctalFALC™ and the QuadFALC® E1/T1/J1 Framer And Line interface Components for long-haul and short-haul applications, supporting 8 or 4 channels on a single chip respectively.

Quad E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications QuadLIU™

PEF 22504 E

Version 2.1

1.1 Features



P/PG-LBGA-160-1

P-TQFP-144-6, -8, -14

Line Interface

- High-density, generic interface for all E1/T1/J1 applications
- Four Analog receive and transmit circuits for long-haul and short-haul applications
- E1 or T1/J1 mode selectable
- Data and clock recovery using an integrated digital phase-locked loop
- Clock generator for jitter-free transmit clocks per channel
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) and PUB 62411 are met
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Flexible programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1. 403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22.5 dB (T1/J1)
- Programmable low transmitter output impedances for high transmit return loss and generic E1/T1/J1 applications
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Flexible tristate functions of the digital receive outputs
- Receive line monitor mode
- Integrated switchtable 300 Ω receive resistors for generic E1/T1/J1 applications to meet termination resistance 75/120 Ω for E1, 100 Ω for T1 and 110 Ω for J1
- Integrated multi purpose analog switch at line receive interface to support generic redundancy applications (only supported in P/PG-LBGA-160-1 package)
- Crystal-less wander and jitter attenuation/compensation according to TR 62411, ETS-TBR 12/13, PUB 62411
- Common master clock reference for E1 and T1/J1 with any frequency within 1.02 and 20 MHz
- Power-down function
- Support of automatic protection switching
- Dual-rail or single-rail digital inputs and outputs
- Unipolar CMI for interfacing fiber-optical transmission routes
- Selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold

Type	Package
PEF 22504 HT	PG-TQFP-144-17
PEF 22504 E	P/PG-LBGA-160-1

- Local loop, digital loop and remote loop for diagnostic purposes. Automatic remote loop switching is possible with In-Band and Out-Band loop codes
- Low power device, two power supply voltages 1.8 V and 3.3 V or a single supply of 3.3 V
- Alarm and performance monitoring per second 16-bit counter for code violations, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS)
- Single-bit defect insertion
- Flexible clock frequency for receiver and transmitter
- Dual elastic stores for both, receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Programmable In-band loop code detection and generation (TR62411)
- Local loop back, payload loop back land remote loop back capabilities (TR54016)
- Flexible pseudo-random binary sequence generator and monitor

Microprocessor Interfaces

- Asynchronous 8/16-bit microprocessor bus interface (Intel or Motorola type selectable)
- SPI bus interface
- SCI bus interface
- All registers directly accessible
- Multiplexed and non-multiplexed address bus operations on asynchronous 8/16-bit microprocessor bus interface
- Hard/software reset options
- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

General

- Boundary scan standard IEEE 1149.1
- PG-TQFP-144-17P-BGA-160-1 package
- Temperature range from -40 to +85 °C
- 1.8 V and 3.3 V power supply or single 3.3 V power supply
- Typical power consumption 140 mW per channel

Applications

- Wireless base stations
- E1/T1/J1 ATM gateways, multiplexer
- E1/T1/J1 **C**hannel & **D**ata **S**ervice **U**nits (CSU, DSU)
- E1/T1/J1 Internet access equipment
- LAN/WAN router
- ISDN PRI, PABX
- **D**igital **A**ccess **C**rossconnect **S**ystems (DACS)
- SONET/SDH add/drop multiplexer

1.2 Logic Symbol

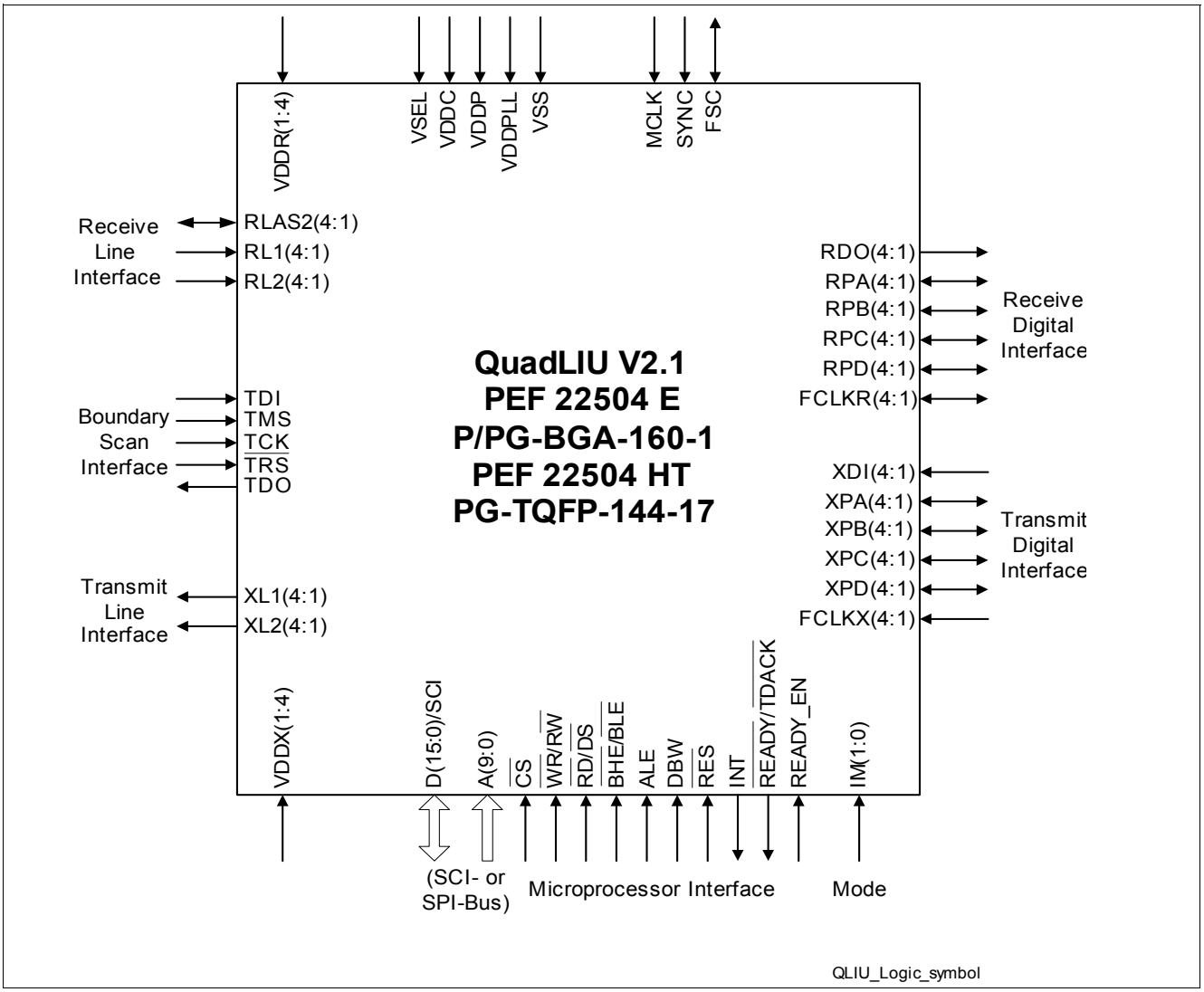


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 shows a multiple link application, **Figure 3** a repeater application using the QuadLIU™.

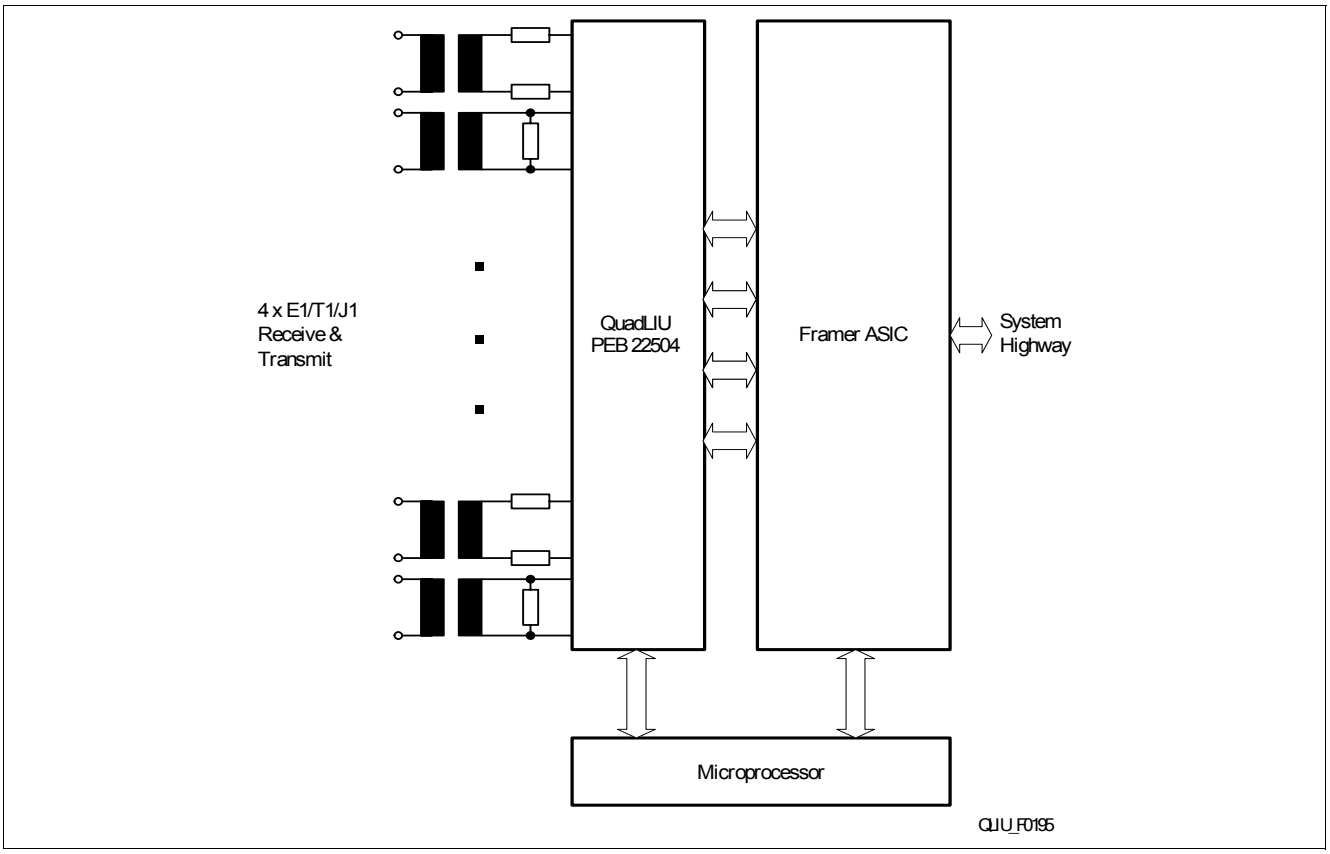


Figure 2 Typical Multiple Link Application

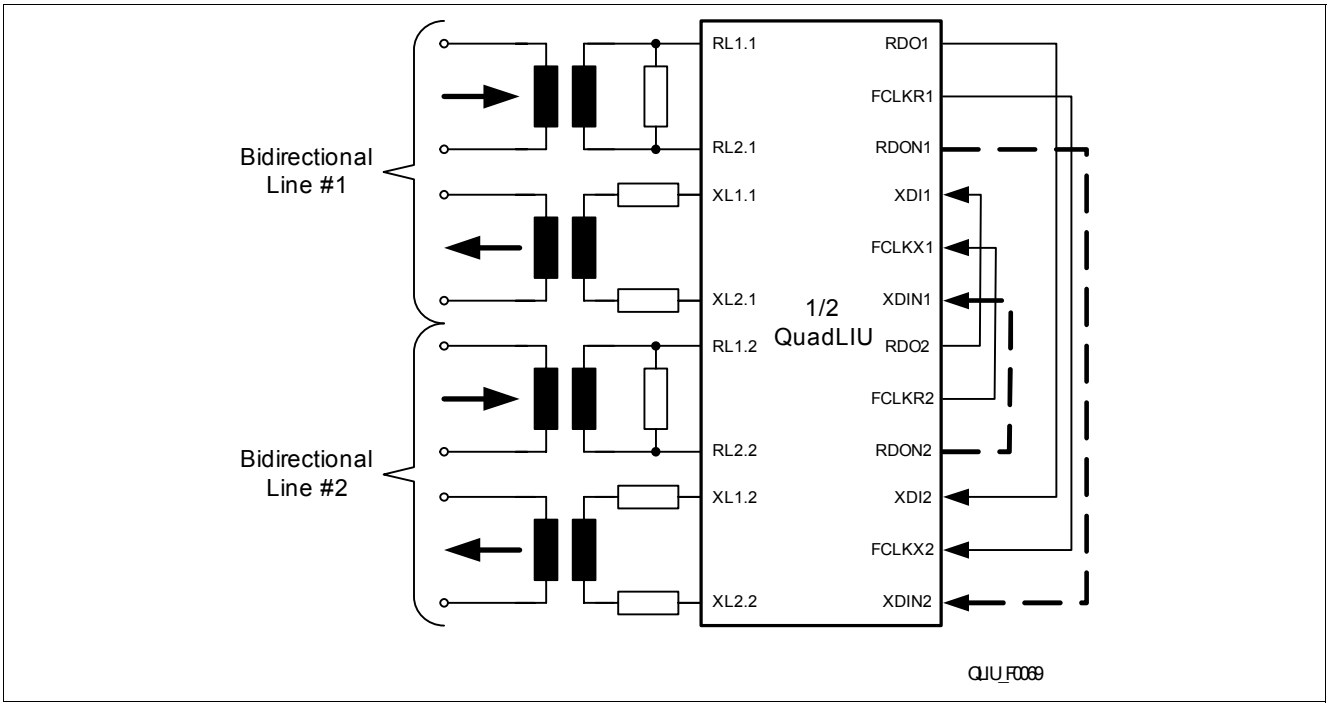


Figure 3 Typical Multiple Repeater Application between line #1 and Line #2

2 Pin Descriptions

In this chapter the function and placement of all pins are described.

2.1 Ball Diagram P/PG-LBGA-160-1 (top view)

Figure 4 shows the ball layout of the QuadLIU™ in a P/PG-LBGA-160-1 package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	●	XL1_2	XL2_2	VDDR	VSSR	RL1_2	RL2_2	RL2_1	RL1_1	VSSR	VDDR	XL2_1	XL1_1	
B	VSSX (RLAS22	VSSX	XDI1	MCLK	XPC2	$\overline{TRS}$	XPD2	VDD	XPA1	VDDP	XPB1	D15	VSSX	VSSX (RLAS21)
C	VDDX	VDDX	FCLKX 1	TCK	VSSP	VDDP	XPA2	XPB2	XPC1	VDDC	TDO	D14	VDDX	VDDX
D	RPC1	RPA1	RPB1	RPD1	TMS	VSEL	RCLK2	VSS	XPD1	RCLK1	TDI	D12	D13	D11
E	RDO1	FCLKR 1	VDD	VDD							VSS	VDD	VDD	D10
F	RDO2	VSS	FCLKR 2	RPA2							D9	D7	D8	D6
G	RPC2	RPB2	FCLKX 2	RPD2			VSS	VSS			D5	READY /DTACK (VDD)	D4	D3
H	XDI3	FCLKX 3	XDI2	RPA3			VSS	VSS			D2	READY EN (VSS)	D0	D1
J	RPB3	RPD3	RPC3	FCLKR 3							$\overline{BHE}$/ $\overline{BLE}$	$\overline{CS}$	$\overline{WR}$/ $\overline{RW}$	$\overline{RD}$/$\overline{DS}$
K	RDO3	IM1 (VSS)	VDD	RDO4							A9	A8	A6	A7
L	FCLKR 4	RPB4	RPA4	DBW	RCLK3	XPA3	XPD3	XPB4	ALE	SEC/ FSC	A5	A3	A2	A4
M	VDDX	VDDX	RPC4	INT	$\overline{RES}$	FCLKX 4	VDD	VDD	XPD4	VDDC	IM	A1	VDDX	VDDX
N	VSSX (RLAS23	VSSX	RPD4	XDI4	XPC3	SYNC	XPB3	XPA4	RCLK4	VSS	XPC4	A0	VSSX	VSSX (RLAS24)
P		XL1_3	XL2_3	VDDR	VSSR	RL1_3	RL2_3	RL2_4	RL1_4	VSSR	VDDR	XL2_4	XL1_4	

QUIU_F0213_2

Figure 4 Top View of the Pin Configuration (Ball Layout) P/PG-LBGA-160-1

2.2 Ball Diagram P/PG-LBGA-160-1 (bottom view)

Figure 4 shows the ball layout of the QuadLIU™ in a P/PG-LBGA-160-1 package.

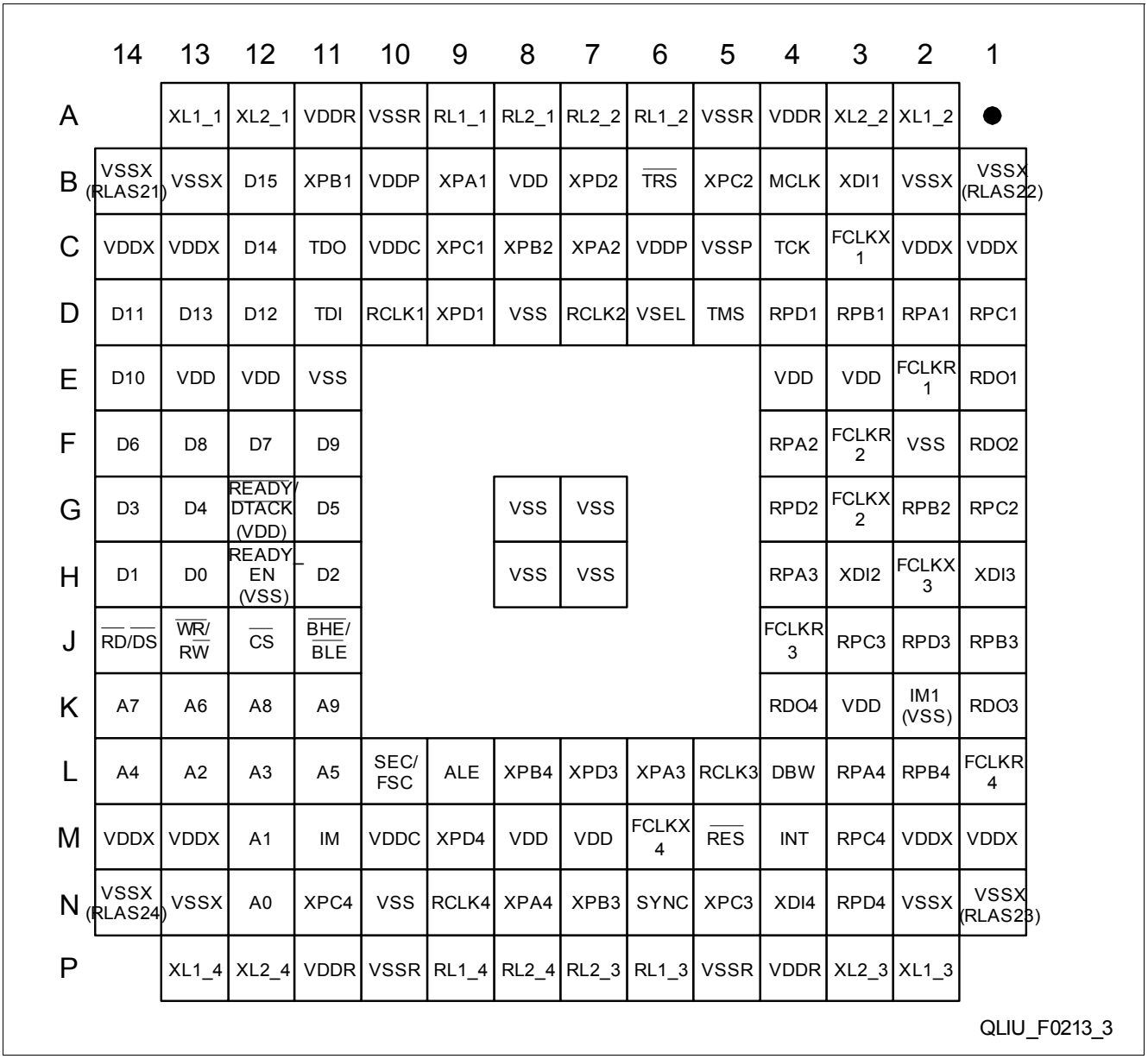


Figure 5 Bottom View of the Pin Configuration (Ball Layout) P/PG-LBGA-160-1

2.3 Pin Diagram P-TQFP-144

Figure 6 shows the pin diagram of the QuadLIU™.

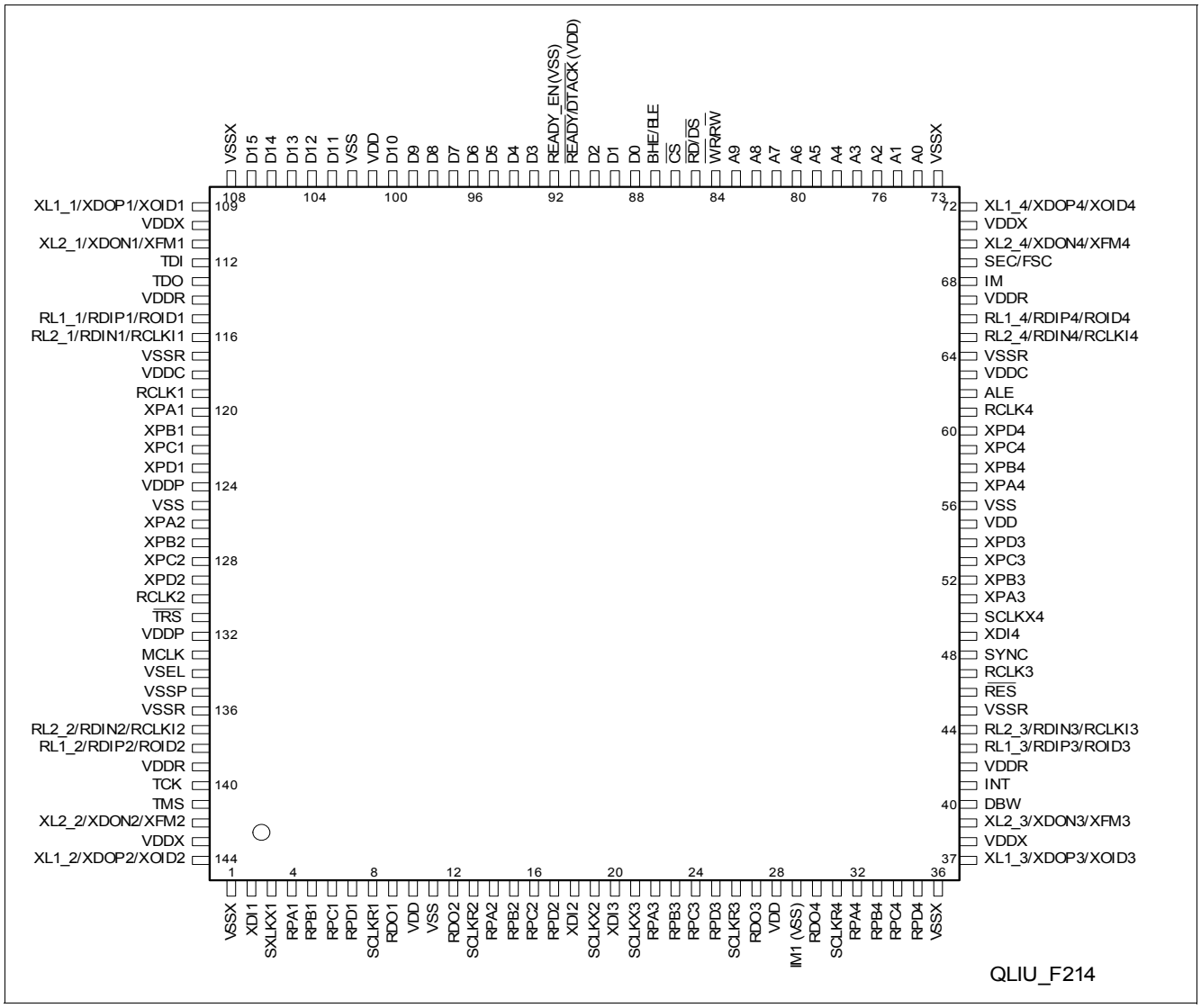


Figure 6 Pin Configuration P-TQFP-144-8

2.4 Pin Definitions and Functions

The following table describes all pins and their functions:

Table 1 I/O Signals for P/PG-LBGA-160-1

Pin No.	Name	Pin Type	Buffer Type	Function
Operation Mode Selection and Device Initialization				
M5	$\overline{\text{RES}}$	I	PU	**Hardware Reset** Active low
K2	IM1	I	PD	**Interface Mode Selection** $'00_B'$: Asynchronous Intel Bus Mode. $'01_B'$: Asynchronous Motorola Bus Mode $'10_B'$: SPI Bus Slave Mode. $'11_B'$: SCI Bus Slave Mode
M11	IM0	I	PU	
Asynchronous and Serial Micro Controller Interfaces				
K11	A9	I	PU	**Address Bus Line 9 (MSB)**
K12	A8	I	PU	**Address Bus Line 8**
K14	A7	I	PU	**Address Bus Line 7**
K13	A6	I	PU	**Address Bus Line 6**
L11	A5	I	PU	**Address Bus Line 5**
	A5	I	PU	**SCI source address bit 5 (MSB)** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
L14	A4	I	PU	**Address Bus Line 4**
	A4	I	PU	**SCI source address bit 4** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
L12	A3	I	PU	**Address Bus Line 3**
	A3	I	PU	**SCI source address bit 3** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
L13	A2	I	PU	**Address Bus Line 2**
	A2	I	PU	**SCI source address bit 2** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
M12	A1	I	PU	**Address Bus Line 1**
	A1	I	PU	**SCI source address bit 1** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
N12	A0	I	PU	**Address Bus Line 0**
	A0	I	PU	**SCI source address bit 0 (LSB)** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
B12	D15	IO	PU	**Data Bus Line 15**
	PLL10	I	PU	**PLL programming bit 10** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.

Table 1 I/O Signals (cont'd)**for P/PG-LBGA-160-1**

Pin No.	Name	Pin Type	Buffer Type	Function
C12	D14	IO	PU	**Data Bus Line 14**
	PLL9	I	PU	**PLL programming bit 9** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
D13	D13	IO	PU	**Data Bus Line 13**
	PLL8	I	PU	**PLL programming bit 8** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
D12	D12	IO	PU	**Data Bus Line 12**
	PLL7	I	PU	**PLL programming bit 7** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
D14	D11	IO	PU	**Data Bus Line 11**
	PLL6	I	PU	**PLL programming bit 6** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
E14	D10	IO	PU	**Data Bus Line 10**
	PLL5	I	PU	**PLL programming bit 5** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
F11	D9	IO	PU	**Data Bus Line 9**
	PLL4	I	PU	**PLL programming bit 4** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
F13	D8	IO	PU	**Data Bus Line 8**
	PLL3	I	PU	**PLL programming bit 3** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
F12	D7	IO	PU	**Data Bus Line 7**
	PLL2	I	PU	**PLL programming bit 2** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
F14	D6	IO	PU	**Data Bus Line 6**
	PLL1	I	PU	**PLL programming bit 1** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
G11	D5	IO	PU	**Data Bus Line 5**
	PLL0	I	PU	**PLL programming bit 0** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
G13	D4	IO	PU	**Data Bus Line 4**
G14	D3	IO	PU	**Data Bus Line 3**

Table 1 I/O Signals (cont'd)**for P/PG-LBGA-160-1**

Pin No.	Name	Pin Type	Buffer Type	Function
H11	D2	IO	PU	**Data Bus Line 2**
	SCI_CLK	I	–	**SCI Bus Clock** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	SCLK	I	–	**SPI Bus Clock** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
H14	D1	IO	PU	**Data Bus Line 1**
	SCI_RXD	I	PU	**SCI Bus Serial Data In** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	SDI	I	PU	**SPI Serial Data In** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
H13	D0	IO	PU	**Data Bus Line 0**
	SCI_TXD	I	PP or oD	**SCI Bus Serial Data Out** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	SDO	I	PU	**SPI Bus Serial Data Out** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
L9	ALE	I	PU	**Address Latch Enable** A high on this line indicates an address on an external multiplexed address/data bus. The address information provided on lines A(10:0) is internally latched with the falling edge of ALE. This function allows the QuadLIU™ to be connected to a multiplexed address/data bus without the need for external latches. In this case, pins A(7:0) must be connected to the data bus pins externally. In case of demultiplexed mode this pin can be connected directly to VDD or can be left open.
J14	$\overline{RD}$	I	PU	**Read Enable** Intel bus mode. This signal indicates a read operation. When the QuadLIU™ is selected via CS, the RD signal enables the bus drivers to output data from an internal register addressed by A(10:0) to the Data Bus.
	$\overline{DS}$	I	PU	**Data Strobe** Motorola bus mode. This pin serves as input to control read/write operations.

Table 1 I/O Signals (cont'd)**for P/PG-LBGA-160-1**

Pin No.	Name	Pin Type	Buffer Type	Function
J13	$\overline{WR}$	I	PU	**Write Enable** Intel bus mode. This signal indicates a write operation. When CS is active the QuadLIU™ loads an internal register with data provided on the data bus.
	$\overline{RW}$	I	PU	**Read/Write Select** Motorola bus mode. This signal distinguishes between read and write operation.
L4	DBW	I	PU	**Data Bus Width select** Bus interface mode A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{BHE}$/$\overline{BLE}$.
J11	$\overline{BHE}$	I	PU	**Bus High Enable** Intel bus mode. If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus D(15:8). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open.
	$\overline{BLE}$	I	PU	**Bus Low Enable** Motorola bus mode. If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus D(7:0). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open.
J12	$\overline{CS}$	I	PU	**Chip Select** Low active chip select.
M4	INT	O	–	**Interrupt Request** Interrupt request. INT serves as general interrupt request for all interrupt sources. These interrupt sources can be masked via registers IMR(7:0). Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR(7:0). Output characteristics (push-pull active low/high, open drain) are determined by programming register IPC.

Table 1 I/O Signals (cont'd)**for P/PG-LBGA-160-1**

Pin No.	Name	Pin Type	Buffer Type	Function
G12	$\overline{\text{READY}}$	O	oD (PU)	**Data Ready** oD output only if activated by READY_EN = 1_B and if Intel bus mode is selected. If not activated (READY_EN = 0_B) the pull-up resistor is active. Asynchronous handshake signal to indicate successful read or write cycle.
	$\overline{\text{DTACK}}$	O	oD (PU)	**Data Acknowledge** oD output only if activated by READY_EN = 1_B and if motorola bus mode is selected. If not activated (READY_EN = 0_B) the pull-up resistor is active. Asynchronous handshake signal to indicate successful read or write cycle.
H12	READY_EN	I	PD	**Ready Enable** Activates the oD functionality of $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$. 0_B: $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is not activated (only pull-up resistor is active). Pin $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ can be connected to VDD. 1_B: $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is an active oD output
Separate Analog Switches (only supported in BGA package)				
B14	RLAS21	IO (analog)	–	**Analog Switch Connector port 1** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1)
B1	RLAS22	IO (analog)	–	**Analog Switch Connector port 2** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1)
N1	RLAS23	IO (analog)	–	**Analog Switch Connector port 3** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1)
N14	RLAS24	IO (analog)	–	**Analog Switch Connector port 4** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1)
Line Interface Receiver				
A9	RL1.1	I (analog)	–	**Line Receiver input 1, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	ROID1	I	–	**Receive Optical Interface Data, port 1** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
A8	RL2.1	I (analog)	–	**Line Receiver input 2, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.

Table 1 I/O Signals (cont'd)**for P/PG-LBGA-160-1**

Pin No.	Name	Pin Type	Buffer Type	Function
A6	RL1.2	I (analog)	–	**Line Receiver input 1, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	ROID2	I	–	**Receive Optical Interface Data, port 2** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
A7	RL2.2	I (analog)	–	**Line Receiver input 2, port 2** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
P6	RL1.3	I (analog)	–	**Line Receiver input 1, port 3** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	ROID3	I	–	**Receive Optical Interface Data, port 3** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
P7	RL2.3	I (analog)	–	**Line Receiver input 2, port 3** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
P9	RL1.4	I (analog)	–	**Line Receiver input 1, port 4** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	ROID4	I	–	**Receive Optical Interface Data, port 4** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
P8	RL2.4	I (analog)	–	**Line Receiver input 2, port 4** Analog input from the external transformer. Selected if LIM1.DRS is cleared.