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Preliminary Data Sheet, DS 1, Nov. 2001

SWITI
Switching IC

PEF 20450 MTSI
PEF 20470 MTSI-L
PEF 24470 MTSI-XL
Version 1.3

Wired
Communications

Infineon
technologies

Never stop thinking.

Edition 2001-11-20

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SWITI
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PEF 20450 / 20470 / 24470
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Table of Contents **Page**

1 Overview . . . 3
1.1 Overview of Features . . . 5
1.2 Features in Detail . . . 6
1.3 Logic Symbol . . . 8
1.4 Standard PBX or CO Application . . . 10

2 Pin Description . . . 11
2.1 Pin Diagrams . . . 11
2.2 Pin Definitions and Functions . . . 12
2.2.1 Local Bus Interface (PCM) . . . 12
2.2.2 General Purpose Port . . . 12
2.2.3 Clock Signals . . . 12
2.2.4 JTAG Interface . . . 13
2.2.5 Microprocessor Interface . . . 13
2.2.6 Power Supply . . . 14

3 Architectural Description . . . 15
3.1 Functional Block Diagram . . . 15
3.2 Overview of Functional Blocks . . . 16
3.3 Switching Factory . . . 17
3.3.1 Switching Modes . . . 17
3.3.1.1 Minimum and Constant Delay . . . 17
3.3.1.2 Subchannel Switching . . . 17
3.3.1.3 Multipoint Switching . . . 17
3.3.1.4 Broadcast Switching . . . 18
3.3.1.5 Bidirectional Switching . . . 18
3.3.1.6 Message Mode . . . 19
3.3.2 Parallel Mode for Local Bus . . . 19
3.3.3 Switching Block Error Handling . . . 20
3.3.4 Analyze Connection and Data Memory . . . 20
3.4 Clock Generator and PLL . . . 21
3.4.1 General Overview . . . 21
3.4.2 Analog PLL (APLL) . . . 22
3.4.2.1 Functional Description . . . 23
3.4.2.2 Jitter Transfer Function . . . 25
3.4.3 Phase Alignment . . . 26
3.4.4 PLL Synchronization . . . 27
3.5 Loops . . . 27
3.6 Read SWITI Configuration with Indirect Register Addressing . . . 27
3.7 Power-On and Reset Behavior . . . 28
3.7.1 Hardware Reset . . . 28
3.7.2 Software Reset . . . 28

4 Description of Interfaces . . . 29

Table of Contents **Page**

4.1 Local Bus Interface (PCM) . . . 29
4.2 Data Rate . . . 30
4.3 Microprocessor Interface . . . 31
4.3.1 Intel/Siemens or Motorola Mode . . . 31
4.3.2 De-multiplexed or Multiplexed Mode . . . 31
4.4 General Purpose Port (GPIO) . . . 33
4.5 General Purpose Clocks . . . 33
4.5.1 Frame Group Outputs . . . 34
4.5.2 GPCLK as Clock Outputs . . . 34
4.6 JTAG (Boundary Scan) . . . 35
4.6.1 Boundary Scan . . . 35
4.6.2 Test-Access-Port (TAP) . . . 35
4.6.3 TAP Controller . . . 36
4.7 Identification Code via µP Read Access . . . 38

5 Register Description . . . 39
5.1 Register Overview For 8-Bit Interface . . . 40
5.2 Detailed Register Description For 8-bit Interface . . . 42
5.3 Register Overview For 16-Bit Interface . . . 67
5.4 Detailed Register Description For 16-Bit Interface . . . 68

6 Programming the Device . . . 72
6.1 Read and Write Access . . . 73
6.2 Interrupt Handling . . . 74
6.3 Command and Register Overview . . . 76
6.4 Indirect Configuration Register Access . . . 81
6.5 Initialization Procedure . . . 82
6.6 Clocking Unit . . . 83
6.7 Local Bus (PCM) Line Interface . . . 84
6.7.1 Standby Command . . . 84
6.7.2 Determining Clock Rates . . . 84
6.7.3 Performing Bit Shifting . . . 85
6.7.3.1 Input Bit Shifting . . . 85
6.7.3.2 Output Bit Shifting . . . 86
6.8 Global Clock Signals . . . 87
6.8.1 Framing Groups . . . 87
6.9 Read Time-Slot Value . . . 88
6.10 Establish Connections . . . 89
6.10.1 Establish 8-bit Connections . . . 89
6.10.2 Subchannel Switching . . . 90
6.10.2.1 Establish 4-bit Connections . . . 90
6.10.2.2 Establish 2-bit Connections . . . 91
6.10.2.3 Establish 1-bit Connections . . . 92
6.10.3 Establish Broadcast Connections . . . 93

Table of Contents **Page**

6.10.4 Establish Subchannel Broadcast Connection 94
6.10.5 Establish Multipoint Connection 95
6.11 Send Messages 96
6.12 Release Connections 97
6.12.1 Release 8-bit Connections 97
6.12.2 Release 4-bit Connections 97
6.12.3 Release 2-bit Connections 97
6.12.4 Release 1-bit Connections 98
6.12.5 Release Broadcast Connection 99
6.12.6 Release Subchannel Broadcast Connection 99
6.12.7 Release Multipoint Connection 100
6.13 Stop Sending Messages 100

7 Timing Diagrams 101
7.1 PCM Interface Timing 101
7.2 PCM Parallel Mode Timing 104
7.3 Microprocessor Interface Timing 105
7.3.1 Infineon/Intel Timing in De-Multiplexed Mode 105
7.3.2 Infineon/Intel Timing in Multiplexed Mode 106
7.3.3 Motorola Microprocessor Timing 108
7.4 JTAG Interface Timing 110
7.5 Hardware Reset Timing 112

8 Electrical Characteristics 113
8.1 Absolute Maximum Ratings 113
8.2 Operating Range 113
8.3 Crystal Oscillator 114
8.4 DC Characteristics 115
8.5 Capacitances 115
8.6 AC Characteristics 116

9 Package Outlines 117

List of Figures

		Page
Figure 1	Logic Symbol	9
Figure 2	Standard PBX or CO Application	10
Figure 3	Pin Configuration	11
Figure 4	Block Diagram	15
Figure 5	Bidirectional Mode	19
Figure 6	SWITI Clock Generator	21
Figure 7	Block Diagram of APLL	23
Figure 8	APLL - Jitter Transfer Function	25
Figure 9	Example of Phase Alignment	26
Figure 10	PCM Interface Configurations	29
Figure 11	PCM Bit Shifting	30
Figure 12	Multiplexed and in De-multiplexed Bus Mode	32
Figure 13	GPIO Port Configuration Example	33
Figure 14	Frame Signal Example	34
Figure 15	Order of Register Access	72
Figure 16	8-bit µP Access Interrupt Structure	74
Figure 17	16-bit µP Access Interrupt Structure	75
Figure 18	Initialization Procedure after Reset	82
Figure 19	Example: Input Bit Shifting	85
Figure 20	Example: Output Bit Shifting	86
Figure 21	Example Framing Groups	87
Figure 22	Example: 8-bit Connection	89
Figure 23	Subchannel Address in Time-Slot	90
Figure 24	Example: 4-bit Connection	90
Figure 25	Example: 2-bit Connection	91
Figure 26	Example: 1-bit Connection	92
Figure 27	Example: Broadcast Connection	93
Figure 28	Example: Subchannel Broadcast Connection	94
Figure 29	Example: Multipoint Connection	95
Figure 30	Example: Send Message	96
Figure 31	PCM Timing	101
Figure 32	Parallel Mode Timing	104
Figure 33	Infineon/Intel Read Cycle in De-Multiplexed Mode	106
Figure 34	Infineon/Intel Write Cycle in De-Multiplexed Mode	106
Figure 35	Infineon/Intel Read Cycle in Multiplexed Mode	107
Figure 36	Infineon/Intel Write Cycle in Multiplexed Mode	108
Figure 37	Motorola Read Cycle	109
Figure 38	Motorola Write Cycle	109
Figure 39	Boundary Scan Timing	111
Figure 40	Hardware Reset Timing	112
Figure 41	External Crystal	114
Figure 42	I/O Wave Form for AC-Test	116
Figure 43	Outlines of P-MQFP-100-2	117

List of Table

		Page
Table 1	Who should read what?	2
Table 2	SWITI Family Tree	3
Table 3	Local Bus Interface	12
Table 4	GPIO	12
Table 5	Clock Pins	12
Table 6	JTAG Interface	13
Table 7	Microprocessor Interface	13
Table 8	Power Supply Pins	14
Table 9	TAP Controller Instructions	36
Table 10	Boundary Scan IDCODE	37
Table 11	IDCODE via µP Read Access	38
Table 12	Register Overview For 8-Bit Interface	40
Table 13	Value Range for SPA/DPA	41
Table 14	Value Range for ITSA/OTSA	41
Table 15	Value Range for SCA	41
Table 16	Register Overview For 16-Bit Interface	67
Table 17	Affected Registers for Connection Commands	76
Table 18	Affected Registers for Configuration Commands	77
Table 19	Connection Command and Parameter Codes	78
Table 20	Configuration Command 1 and Parameter Codes	79
Table 21	Configuration Command 2 and Parameter Code	79
Table 22	PCM Timing	102
Table 23	PCM Parallel Mode Timing	104
Table 24	Infineon/Intel Timing in De-Multiplexed Mode	105
Table 25	Infineon/Intel Timing in Multiplexed Mode	107
Table 26	Motorola Timing	108
Table 27	JTAG Interface Timing	110
Table 28	Hardware Reset Timing	112
Table 29	Absolute Maximum Ratings	113
Table 30	Operating Range	113
Table 31	External Capacitances for Crystal (Recommendation)	114
Table 32	DC Characteristics	115
Table 33	Input/Output Capacitances	115

PRELIMINARY

Preface

The Switching IC (SWITI) is a family of switching devices for a wide area of telecommunication and data communication applications. This document provides complete reference information according to chip interfaces, programming, internal architecture and applications.

Organization of this Document

This Preliminary Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Description**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Description of Interfaces**
  Rough overview of the internal architecture.

- **Chapter 4, Description of Interfaces**
  Short introduction of used interfaces.

- **Chapter 5, Register Description**
  Gives information about all registers accessible via the microprocessor interface according to address, short name, access, reset value and value range.

- **Chapter 6, Programming the Device**
  Gives a variety of examples how to programm the device, lists all available command and parameter values.

- **Chapter 7, Timing Diagrams**
  Contains timing diagrams.

- **Chapter 8, Electrical Characteristics**
  Specification of the electrical parameters.

- **Chapter 9, Package Outlines**
  Outlines of the available packages (P-MQFP-100-2).

PRELIMINARY

Table 1 Who should read what?

Addressed Person	Relevant Chapters
Programmer	3, 5, 6
Board Designer	2, 3, 4, 7, 8, 9

1 Overview

The new switching family, called SWITI, provides a complete and cost-effective solution for all switching systems. The family is divided in two sub-families, the MTSI family and the HTSI family. The Preliminary Data Sheet describes the functionality and characteristic of the MTSI devices.

The devices can be used in today's switching applications, e.g. conventional PBXs and central offices, as well as in H.100/H.110 applications (only the HTSI family), which are the key to high performing CTI- and Voice-over-IP-applications, one of the most important future technologies in telecommunications.

The main requirements of today's switching applications are met by the following features:

- Constant delay e.g. to support wide band data switching, or channel bundling
- Bit switching/subchannel switching to support applications such as mobile base stations, DECT, computer telephony

In addition, the SWITI family provides new features to ensure a broad range of configurations to make it possible to adapt the device to all switching applications:

- A compliant H.100/H.110 interface (HTSI)
- 8-channel stream-to-stream switching capability (HTSI)
- Message mode, which allows to assign a preset value to any output time-slot
- GPIO (General Purpose I/O) port, which is controlled from the external µP

SWITI family. The SWITI family consists of 6 ICs with different switching capacities. The possible configurations are shown in **Table 2**. The HTSI versions provide an additional H.100 / H.110 interface, while the MTSIs are standard switching devices. All devices can be programmed easily, thus helping the designer/programmer to integrate the device into his application comfortably.

Table 2 SWITI Family Tree

Name	Package	Sales code	Connec-tions	Local bus IN/OUT	H-Bus IO
HTSI-XL (H-Mode)	P-BGA-217-1	PEF24471 HTSI-XL	2048	16/16	32
HTSI-XL (M-Mode)		PEF24471 HTSI-XL		32/32	-
HTSI-L (H-Mode)	P-BGA-217-1	PEF20471 HTSI-L	1024	16/16	32
HTSI-L (M-Mode)		PEF20471 HTSI-L		32/32	-

Table 2 SWITI Family Tree (cont'd)

Name	Package	Sales code	Connec-tions	Local bus IN/OUT	H-Bus IO
HTSI (H-Mode)	P-BGA-217-1	PEF20451 HTSI	512	16/16	32
HTSI (M-Mode)		PEF20451 HTSI		32/32	-
MTSI-XL	P-MQFP-100-2	PEF24470 MTSI-XL	2048	16/16	-
MTSI-L	P-MQFP-100-2	PEF20470 MTSI-L	1024	16/16	-
MTSI	P-MQFP-100-2	PEF20450 MTSI	512	16/16	-

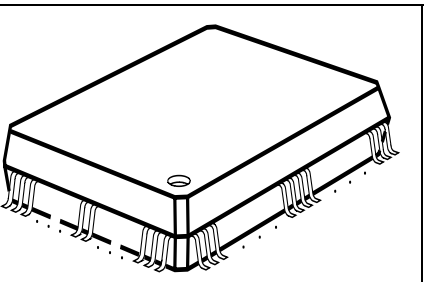
PRELIMINARY

Switching IC SWITI

PEF 20450 / 20470 / 24470

Version 1.3 **CMOS**

1.1 Overview of Features



P-MQFP-100-2

General

- Switching capacity of 512, 1024, or up to 2048 connections of different types between different buses
- Programmable data rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s on per stream basis
- 16 PCM Highways (IN/OUT)
- Constant delay or minimum delay programmable on per connection basis
- Subchannel switching ability of 1-bit, 2-bit, 4-bit wide time-slots
- Programmable clock shift for local bus
- Automatic data rate adaption
- Optional 8-bit parallel input and/or 8-bit parallel output for first 8 lines of local bus
- Broadcast capabilities
- Multipoint switching ability
- Read and write access to all time-slots
- Message mode (time-slot write access)
- Programmable framing group
- GPIO port
- 8-bit µP-interface supports both Intel and Motorola mode
- Optional 16-bit µP interface mode (instead of GPIO port)
- On chip PLL for PCM bus clock operation (master/slave)
- JTAG interface
  - Boundary scan according to IEEE 1149.1
- 3.3 V power supply
- 5 V tolerant inputs/outputs

Type	Package
PEF 20450 / 20470 / 24470	P-MQFP-100-2

1.2 Features in Detail

Flexible Data Rates

Each input and each output line of the local bus is programmable to operate at different data rates. The possible data rates are 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s.

Constant and Minimum Delay

Each connection independent of the addressed buses can be determined to be a constant delay or minimum delay connection. Constant delay means that any input time-slot or subchannel is available on the programmed output after 2 frames. Minimum delay means that the time-slot or subchannel appears at the output as soon as possible. The minimum delay depends on the chosen connections and the possible range is between 0 and 2 frames.

Subchannel Switching

Each connection can be a 1-bit, 2-bit, 4-bit, or 8-bit connection. Subchannel switching has a constant delay of 2 frames. Subchannel switching is supported only for data rate of 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Programmable Clock Shift

The position of time-slot 0 of each local bus input line can be programmed within the time-slot before and after the PFS rising edge in half bit steps. Also the position of time-slot 0 of all local bus output lines can be programmed within the first time-slot after the PFS rising edge.

Automatic Data Rate Adaption

Connections are also possible between lines operating at different data rates. The programmer just specifies input and output line, time-slot, and if necessary, the subchannel.

Parallel Mode

The first 8 local bus input and output lines can be configured to one parallel input or output port respectively. In serial mode a time-slot is determined by 8 consecutive data clock cycles according to each line. In parallel mode a time-slot is determined by 1 data clock cycle according to the first 8 lines.

Broadcast

With this feature it is possible to distribute one incoming time-slot to different output time-slots.

Multipoint

Multipoint connections can be seen as the opposite of broadcast connections. Here it is possible to generate one output time-slot consisting of several input time-slots. The specified input time-slots are logically AND or OR connected (selectable) and have a constant delay of 2 frames.

Read Access

The programmer has access to any input time-slot. After issuing an appropriate command the arrival of the time-slot will be reported by interrupt. The value can be read from a dedicated register. For every read request the command has to be issued again.

Message Mode (Write Access)

This feature allows a constant value to be sent to any given output time-slot.

Framing Group

It is possible to specify up to 8 different framing signals of 8 kHz. The position of the rising edge and the pulse width can be programmed for each signal. The reference frame is determined by the PFS signal. The pulse parameters are programmed in half step resolution according to a 16.384 MHz clock.

General Purpose Clocks

All 8 GPCLK lines can be configured as individual clock outputs with 8 kHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz and for test purposes with the internal frequency or the input frequency of the analog PLL (APLL).

GPIO Port

Each line of the general purpose input/output port can be configured to be either input or output. According to an input an edge causes an interrupt. The outputs can be influenced by write access via the microprocessor interface. Thus the user has the possibility to observe and influence additional signals for his application.

Microprocessor Interface

All devices provide a standard 8-bit microprocessor interface operating in either Intel or Motorola mode. Optionally it is possible to configure the GPIO port as additional data lines to provide a 16-bit microprocessor interface. The use of the 16-bit µP interface

reduces the number of write cycles required to configure a connection from 7 (in case of 8-bit µP interface) to 3 write cycles.

Input/Output Tolerance

The MTSI can be used in a 5 V environment. Inputs and outputs are 3.3 V and 5 V tolerant. The outputs have TTL level driving capability.

1.3 Logic Symbol

The MTSI is a pure PCM switch and provides 16 PCM input lines and 16 PCM output lines.

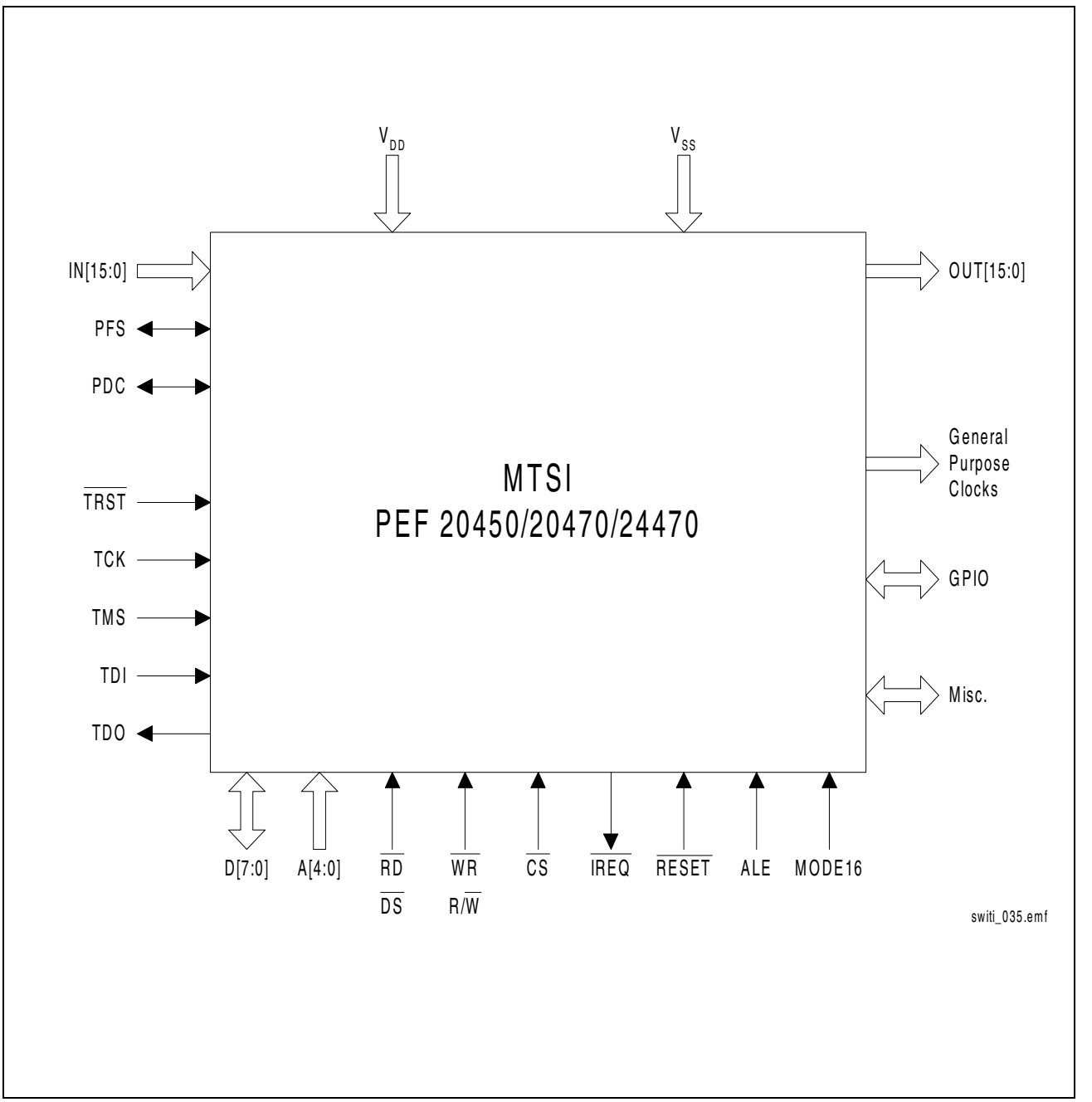


Figure 1 Logic Symbol

1.4 Standard PBX or CO Application

The MTSI or the HTSI in M-Mode can be used, just as the MTSC or MTSL, in standard private branch exchange or central office applications (**Figure 2**), e.g. in the switching network.

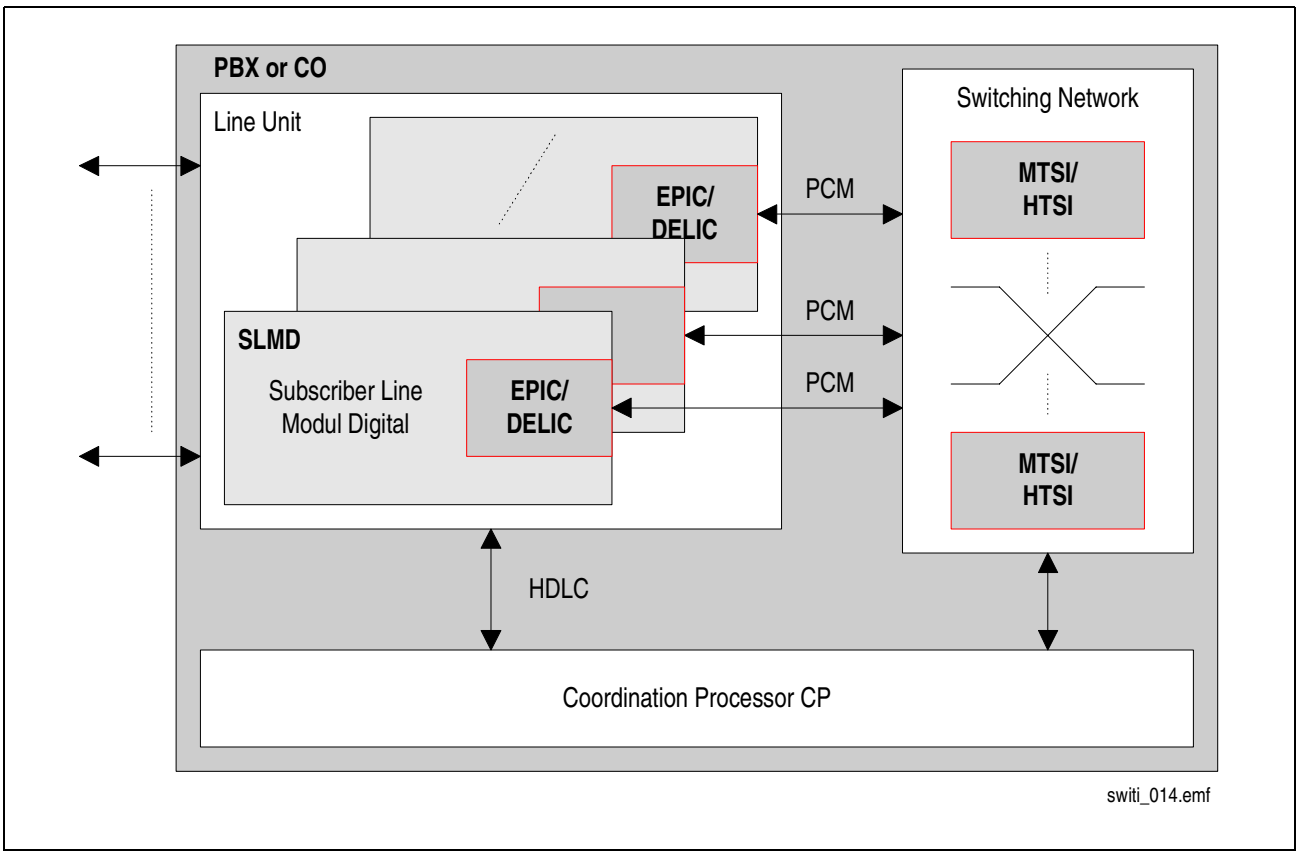


Figure 2 Standard PBX or CO Application

2 Pin Description

The pin description gives an overview of the pin numbers, names, direction, position and function ordered by the different interfaces.

Note: All unused input or I/O pins should be connected to V_{SS} to avoid leakage current.

2.1 Pin Diagrams

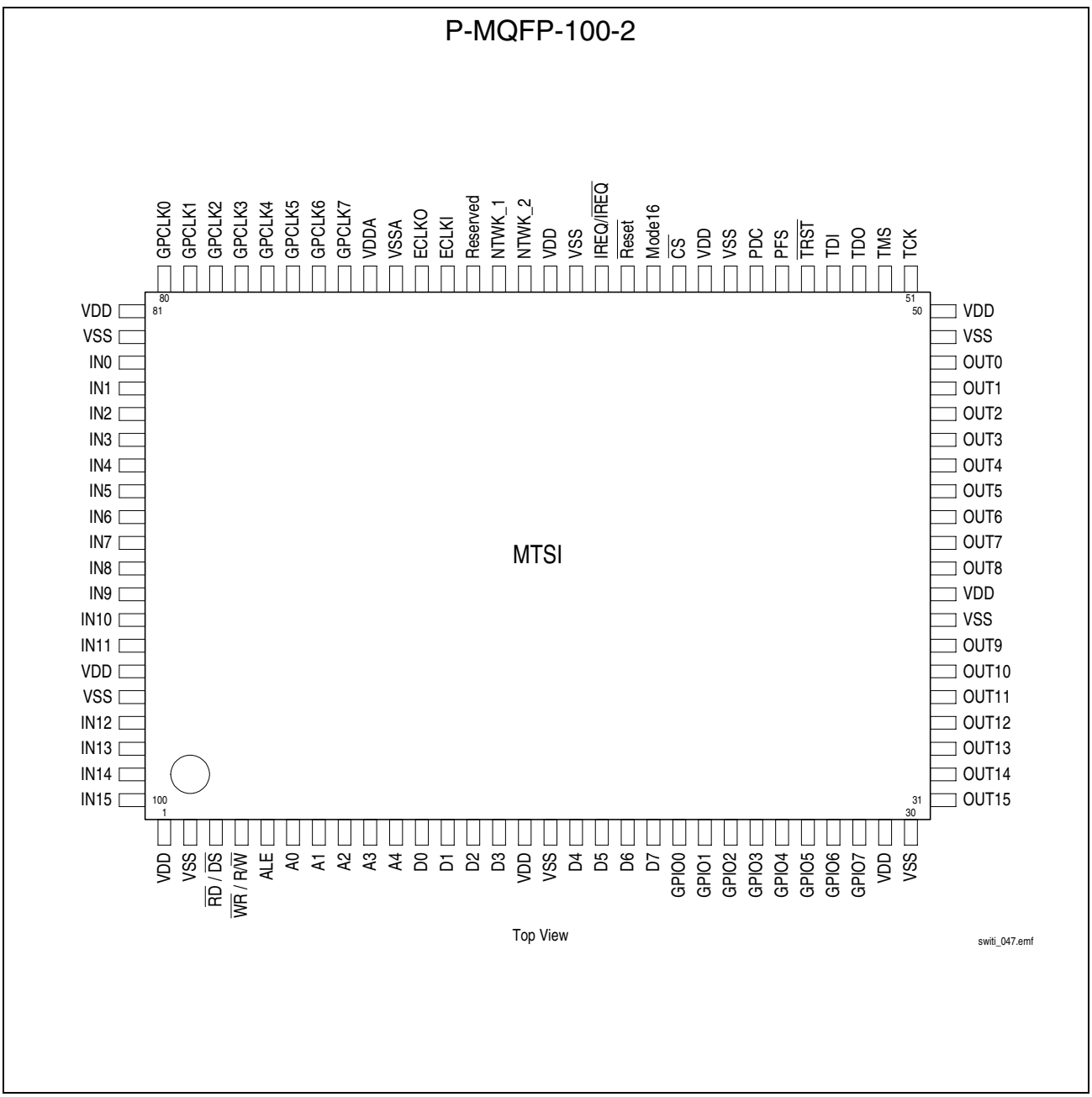


Figure 3 Pin Configuration

2.2 Pin Definitions and Functions

2.2.1 Local Bus Interface (PCM)

Table 3 Local Bus Interface

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
56	PFS	I/O	PCM Frame Synchronization Clock of 8 kHz	High Z
57	PDC	I/O	PCM Data Clock of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, 16.384 Mbit/s	High Z
100-97, 94-83	IN[15:0][1)]	I	PCM Receive Data Port 15 to 0	
31-37, 40-48	OUT[15:0][2)]	O	PCM Transmit Data Port 15 to 0	High Z

1) 100 is IN15, 99 is IN14, 98 is IN13..

2) 31 is OUT15, 32 is OUT14, 33 is OUT13..

2.2.2 General Purpose Port

Table 4 GPIO

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
28-21	GPIO[7:0][1)] D[15:8]	I/O	General Purpose I/O port (only if 8-bit µP interface used) Upper 8 bit of 16-bit µP interface	Input

1) 28 is GPIO7, 27 is GPIO6, 26 is GPIO5..

2.2.3 Clock Signals

Table 5 Clock Pins

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
69	ECLKI	I	External Crystal Input of 16.384 MHz, or 32.768 MHz External Oscillator Input of 16.384 MHz, or 32.768 MHz	
70	ECLKO	O	External Crystal Output of 16.384 MHz, or 32.768 MHz	
73-80	GPCLK[7:0] 1)	O	General Purpose Clock Output (Framing Signals)	High Z

Table 5 Clock Pins (cont'd)

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
67	NTWK_1	I	Primary Network Timing Reference Input Optionally the PLL can be synchronized to this input which can be 8 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz	
66	NTWK_2	I	Secondary Network Timing Reference Input Optionally the PLL can be synchronized to this input which can be 8 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz	

1) 73 is GPCLK7, 74 is GPCLK6, 75 is GPCLK5..

2.2.4 JTAG Interface

Table 6 JTAG Interface

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
51	TCK	I	Test Clock Single rate test data clock.	
52	TMS	I	Test Mode Select A '0' to '1' transition on this pin is required to step through the TAP controller state machine.	
55	$\overline{\text{TRST}}$	I	Test Reset Resets the TAP controller state machine (asynchronous reset).	
53	TDO	O	Test Data Out In the appropriate TAP controller state test data or a instruction is shifted out via this line.	High Z
54	TDI	I	Test Data Input In the appropriate TAP controller state test data or a instruction is shifted in via this line.	

2.2.5 Microprocessor Interface

Table 7 Microprocessor Interface

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
60	$\overline{\text{CS}}$	I	Chip Select Active low. A "low" on this line selects all registers for read/ write operations.	
3	$\overline{\text{RD}}$ $\overline{\text{DS}}$	I	Read (Intel/Infineon Mode) Indicates a read access. Data Strobe (Motorola Mode) During a read cycle, DS indicates that the device should place valid data on the bus. During a write access, DS indicates that valid data is on the bus.	

Table 7 Microprocessor Interface (cont'd)

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
4	$\overline{WR}$ R/$\overline{W}$	I	Write (Intel/Infineon Mode) Indicates a write access. Read/Write (Motorola Mode) Indicates the direction of the data transfer on the bus.	
5	ALE	I	Address Latch Enable Controls the on-chip address latch in multiplexed bus mode. While ALE is 'high', the latch is transparent. The falling edge latches the current address. ALE is also evaluated to determine the bus mode (ALE fix 'low' = Motorola, fix 'high' = Intel/Infineon)	
61	MODE16	I	Microprocessor Bus 8/16-Bit Interface Selection ('low' = 8 bit, 'high' = 16 bit)	
63	IREQ/ $\overline{IREQ}$	O OD	Interrupt Request This pin is programmable to push/pull (active high or low) or open-drain. This signal is activated when SWITI requests an µP interrupt. When operated in open drain mode, multiple interrupt sources may be connected.	High Z
10-6	A[4:0][1)]	I	Address Bus When operated in address/data multiplex mode, the address pins are externally connected to the D bus.	
20-17, 14-11	D[7:0][2)]	I/O	Data bus	Input
62	$\overline{RESET}$	I	System Reset SWITI is forced to go into reset state.	

1) 10 is A4, 9 is A3, 8 is A2..

2) 20 is D7, 19 is D6, 18 is D5..

2.2.6 Power Supply

Table 8 Power Supply Pins

Pin No.	Symbol	In (I) Out (O)	Function
1,15, 29,39, 50,59, 65,81, 95	V_{DD}	I	Power Supply 3.3 V
2,16, 30,38, 49,58, 64,82, 96	V_{SS}	I	Digital Ground (0 V)
72	V_{DDA}	I	Power Supply Analog Logic 3.3 V Used for PLL
71	V_{SSA}	I	Analog Ground (0 V)
68	R		Reserved. Must be connected to ground

3 Architectural Description

The following sections give a short overview of the functionality of the SWITI.

3.1 Functional Block Diagram

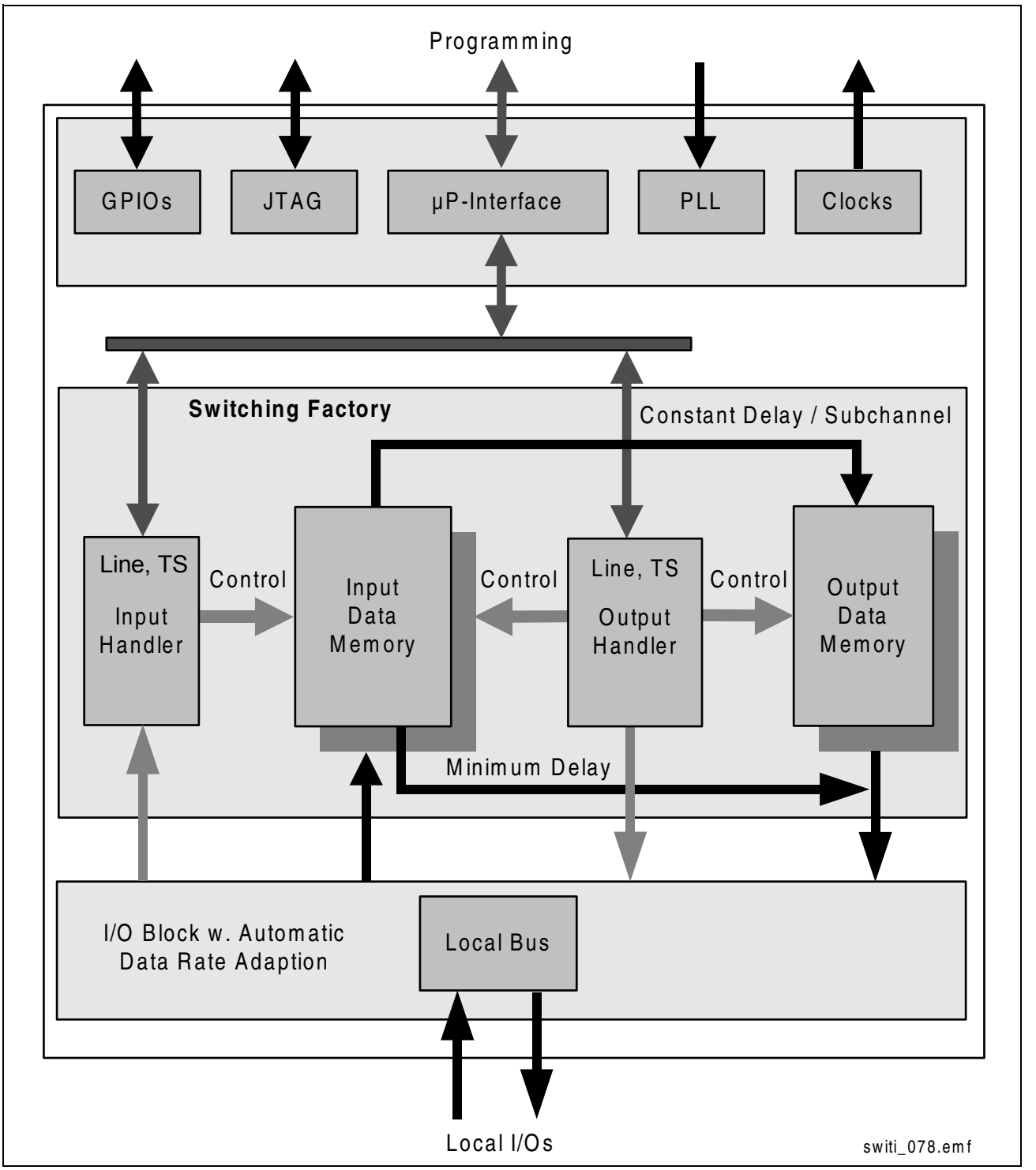


Figure 4 Block Diagram

3.2 Overview of Functional Blocks

Switching Factory

The switching factory is responsible for transferring and handling the incoming data streams to the assigned output channels and time-slots. The block includes a 512, 1024, or 2048 byte input and output data memory as well as an input and output connection memory.

Local bus I/O Block

The block is designed to handle the conversion of the data provided via the switching block and the external local bus (PCM) interface. It performs the PCM timing, the data rate selection and the tristate control.

Microprocessor Interface Block

A standard 8-bit multiplexed or de-multiplexed µP interface is provided, compatible to Intel/Infineon Tech. (e.g. 80386EX, C166) and Motorola (e.g. 68040, 68340, 68360, 801) bus systems. If the GPIO port is not needed it can be used to provide a 16-bit µP interface.

GPIO Block

This block supports up to 8 external port lines each one configurable as input or output. A change on an input line may cause an interrupt (if not masked). The user has access to the port configuration and information via the appropriate registers of the µP interface.

PLL and Clock Block

The PLL generates all frequencies supporting the local bus (PCM). The internal phase-locked loop (PLL) generates all bus frequencies synchronized to a selected reference signal. The output frequency tolerance is equal to the input frequency tolerance. The PLL operates from a 16.384 MHz, or 32.768 MHz external crystal, oscillator.