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Data Sheet, DS1, Sep. 2002

DFE-T V2.2

Quad ISDN 4B3T Echocanceller Digital Front End

PEF 24901, Version 2.2

Wired Communications

Infineon technologies

Never stop thinking.

Edition 2002-09-30

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Data Sheet

Revision History:	**2002-09-30**	DS1
Previous Version:	Preliminary Data Sheet, DS1, 6.99	

Page	**Subjects (major changes since last revision)**
	update related documents
Chapter 1	conforms to ITU-T G.961 (not ITU-T I.430) removed transparent channel
Chapter 1.1	Removed: Sophisticated power management for restricted power mode Removed: Monitor Time-Out (MTO) procedure 'LTD' supported Coefficients are no more retrievable by MON-8 commands
Figure 2, **Figure 6**, **Table 1**	logic symbol, pin conf., pin definitions: removed TP1, MTO 49, 53: no function, may be clamped to GND or VDD, respectively, for compatibility to former versions
Chapter 1.3	added DELIC-PB, restriction on DELIC-PB, added Vbat, removed solution with ELIC/IDEC (IDEC is discontinued)
Page 19	added note on CLOCK and FSC from same source
Figure 4	added connection between pin CLOCK and FSC
Table 1, **Table 2**	changed: pins CLS 0..3 indicate 1 ms clock of the received frame.
Table 1	added footnote to PU/PD to TCK in case that JTAG is reset: e.g. pull-down 47 kΩ
Table 1	removed from all PD/PU-pins: internal pullup (160 kΩ), added footnote to PU/PD: e.g. 10 to 20 kΩ
Table 1	removed from PUP: (as soon as 1.FSC was received after reset)
Chapter 2.3	updated pinning changes
Table 3	added new table 'pin controlled test modes'
Chapter 3.1	removed dedicated block diagram
Chapter 3.2.2	replaced double last look criterion by real reaction times
Chapter 3.2.3	removed MON0 commands
Chapter 3.2.3	removed MTO function
Chapter 3.3	$\overline{\text{NOP}}$ is always set to one added note: activation of the interface to the analog front end

Data Sheet

Revision History: 2002-09-30 DS1

Chapter 3.5	removed from 1 kHz Frame: '..40 kHz block clock'
Chapter 3.5.1	removed 'After successful synchronization, resynchronization will occur if the syncword is not detected at the expected position in 64 consecutive frames. The U-transceiver is synchronized, if it detects the syncword four times consecutively within a period of 1 ms.'
Chapter 3.5.8, **Chapter 3.5.11.2**	removed U2A (not supported)
Page 15, **Page 45**	removed statement on performance on 0.6mm FTZ loops
Page 47	removed transparent messages
Table 12	refined description of signal detection, removed transparent channel from table 4B3T signal elements
Chapter 3.5.9	refined description C/I-codes, changed validation times of C/I-commands, introduced LTD
Figure 17	updated state machine
Table 14	updated differences to the former state machine
Chapter 3.5.11.1	changes to state machine inputs: C/I=AR1: no reset of receiver C/I DC: state Deactivted is entered
Chapter 3.5.11.2	C/I-indication 'AI' is also issued if test loop #1 has been activated
Page 64	Transparent state may also be entered by loopback 1 (not loopback 2)
Chapter 3.5.5	reworked chapter block error counter
Chapter 3.5.11.1	AR1, AR2, and AR4: added description of resolving loopback requests
Chapter 3.6	changed chapter 'clock generation',
Chapter 4.1	added to HW reset: '...the 15.36 MHz ...', ' ...Note that FSC and DCL...'
Chapter 4.2	the DFE-T goes in power down, if the U-transceiver is in state 'Deactivated' and no MONITOR message is pending
Figure 26	testloops repeater: #4
Chapter 4.4.1.2	removed fig: 'Loopback #2'

Data Sheet

Revision History: 2002-09-30 DS1

Figure 27	reworked
Chapter 4.4.1.3	DLB is always transparent
Chapter 4.4.2	reworked chapter RDS, added note with active states
Chapter 4.4.3	reworked operation
Chapter 4.4.4.2	added note: Data Through is pure test mode
Chapter 4.4.5	removed chapter: DSP access - not supported
Chapter 4.4.5	added note on pin 16 and 49
Table 18	changed coding of instruction BYPASS: ’1111’ (instead of ’11XX’)
Table 19 **Table 20**	restricted tables to commands and indications for DFE-T V2.2
Table 19	added note on response to 87xxh
Table 20	coding of MON-8 command AST = ’810X’ (not ’880X’); AST is sent in upstream direction
Page 89	removed MON-0: not supported
Chapter 6	reworked fig. DFE-T V2.2 Register Map
Chapter 6.1	reworked register summary
Chapter 6.1.1 **Chapter 6.1.2**	new chapters added: registers TEST and LOOP are evaluated and executed immediately
Chapter 6.2	reworked detailed register description
Chapter 7.1	updated
Chapter 7.2	updated
Chapter 7.3	updated
Figure 29	removed 100 pF load capacitance
Chapter 7.4	updated
Table 23 **Table 25**	updated
Chapter 7.5	removed clock input capacitance
Chapter 7.6	updated

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Preface

This document describes the interfaces, functions and behavior of the QUAD ISDN 4B3T Echocanceller Digital Front End (DFE-T V2.2). The PEF 24901 is the digital part of a two-chip solution featuring four times ISDN basic rate access at 144 kbit/s. DFE-T V2.2 supersedes the existing versions, DFE-T V1.1 and DFE-T V1.2.

The corresponding Analog Front End, the AFE V2.1 (PEF 24902) is described in detail in the Data Sheet V1.1, the Delta Sheet V1.2 and the Data Sheet V2.1.

Organization of this Document

This Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1**, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2**, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3**, Functional Description
  Gives a functional overview of the device, shows a block diagram, specifies the various interfaces and describes the provided U-transceiver functions.

- **Chapter 4**, Operational Description
  Describes the reset and power-down behavior, illustrates the activation and deactivation procedures, shows how the device is tested and how maintenance data can be retrieved.

- **Chapter 5**, Monitor Commands
  Lists all available Monitor Commands that can be applied.

- **Chapter 6**, Register Description
  Lists all register functions that are addressable by the new MON-12 protocol.

- **Chapter 7**, Electrical Characteristics
  Denotes the operating conditions and gives the exact interface timing.

- **Chapter 8**, Package Outlines

- **Chapter 9**, Appendix A: Standards and Specifications

- **Chapter 10**, Terminology
- **Chapter 11**, Index

Related Documentation

- DFE-T V2.2 Product Brief 03.01
- DFE-T V2.2 Delta Sheet 11.01
- AFE V1.1 Data Sheet 05.96
- AFE V1.2 Delta Sheet 06.97
- AFE V2.1 Data Sheet 01.01

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1 Introduction

The Quad ISDN 4B3T Echocanceller Digital Front End (DFE-T) is the digital part of an optimized two-chip solution featuring 4x ISDN basic rate access at 144 kbit/s. The PEF 24901 is designed to provide in conjunction with the Quad ISDN Echocanceller Analog Front End (PEF 24902 V2.1) full duplex data transmission at the U-reference point according to FTZ Guideline 1TR 220, ETSI TS 102 080 and ITU-T G.961 standards.

The DFE-T 2nd generation has been completely reengineered to guarantee the availability of the well proved DFE-T/AFE solution over the year 2000. PEF 24901 V2.2 is downwards pin compatible and functionally equivalent to the DFE-T V1.x. Thus, line card manufacturers can make use of the most advanced process technology without the need to change their current design (besides the changeover to 3.3 V power supply).

No software changes are required if the DFE-T V2.2 is deployed in existing DFE-T V1.x solutions. Some new features are provided such as enhanced monitoring and test functions. The data rate is programmable from 1 Mbit/s to 4 Mbit/s.

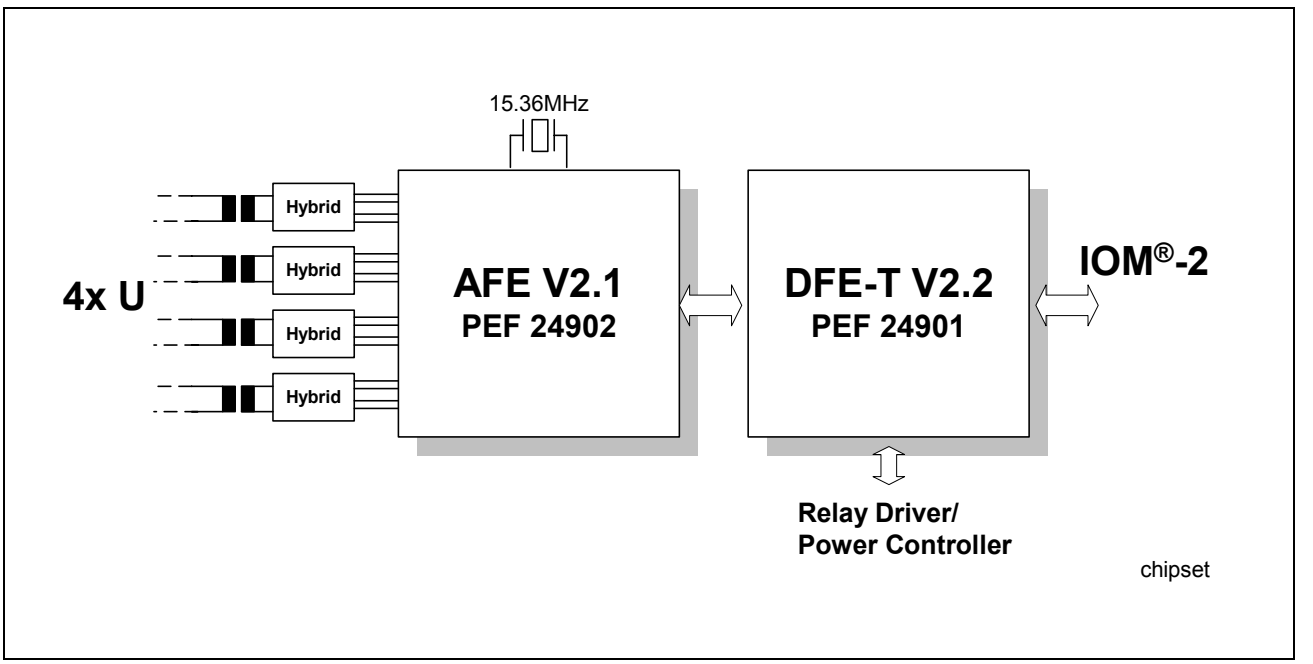


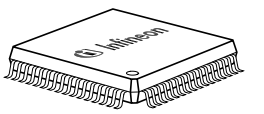
Figure 1 DFE-T/ AFE 2nd Generation Chip Set

The output and input pins are throughout 5 V TTL compatible although the PEF 24901 is processed in advanced 3.3 V CMOS technology. A power down state with very low power consumption is featured.

The PEF 24901 comes in a P-MQFP-64 package.

Version 2.2

1.1 Features



P-MQFP-64-1, -2, -3, -8

U-Interface

- Digital part of a two-chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access at 144 kbit/s
- Conforms to:
  - FTZ 1TR 220 (1991)
  - ETSI TS 102 080 V1.3.1 (1998)
  - ITU-T G.961 (1995)
- 4B3T-block code at 120-kHz symbol rate
- Subscriber loop length without repeater:
  - up to 4.2 km on 0.4 mm wire
- LT mode
- 1 kbit/s maintenance channel for transmission of data loopback commands and detected transmission errors
- Activation/ deactivation controller
- Adaptive echo cancellation and equalization
- Automatic gain control and polarity adaption
- Clock recovery (frame and bit synchronization)
- Transmission error counters for line monitoring
- Remote and local control of test loops

System Interface

- IOM®-2 interface with programmable data rates (1 Mbit/s to 4 Mbit/s)
- 4 relay driver pins per port addressable by Monitor command
- 2 status pins per port accessible via Monitor channel

Type	Package
PEF 24901	P-MQFP-64

Other Features

- Software compatible to the PEF 24901 V1.2
- Inputs and outputs 5 V TTL compatible
- DOUT (open drain) accepts pull-up to 3.3 V or 5 V
- Advanced low power CMOS technology
- +3.3 V ±0.3 V Power Supply
- Extended temperature range (– 40 ... to 85 °C) available
- Boundary-Scan, JTAG IEEE 1149.1

Add-On Features and Differences with Respect to DFE-T V1.2

- +3.3 V instead of +5 V power supply
- LT-RP mode is not supported
- DOUT configurable either as open drain or push-pull (tristate) output
- Bit Error Rate measurement per port
- Additional digital local loops
- C/I code ’HI’ are no more supported
- C/I code mnemonics adapted to 2B1Q notation for consistency reasons - coding has been retained unchanged
- State machine notation is aligned to that of 2B1Q for consistency reasons
- New MON-12 class features internal register access
- Coefficients are no more retrievable by MON-8 commands
- The Boundary-Scan instructions ’CLAMP’ and HIGHZ are supported in version 2.2 (’SSP’ is omitted since for this function a dedicated pin is reserved)
- JTAG Boundary-Scan with dedicated reset line $\overline{\text{TRST}}$ (replaces power-on reset functionality)

1.2 Logic Symbol

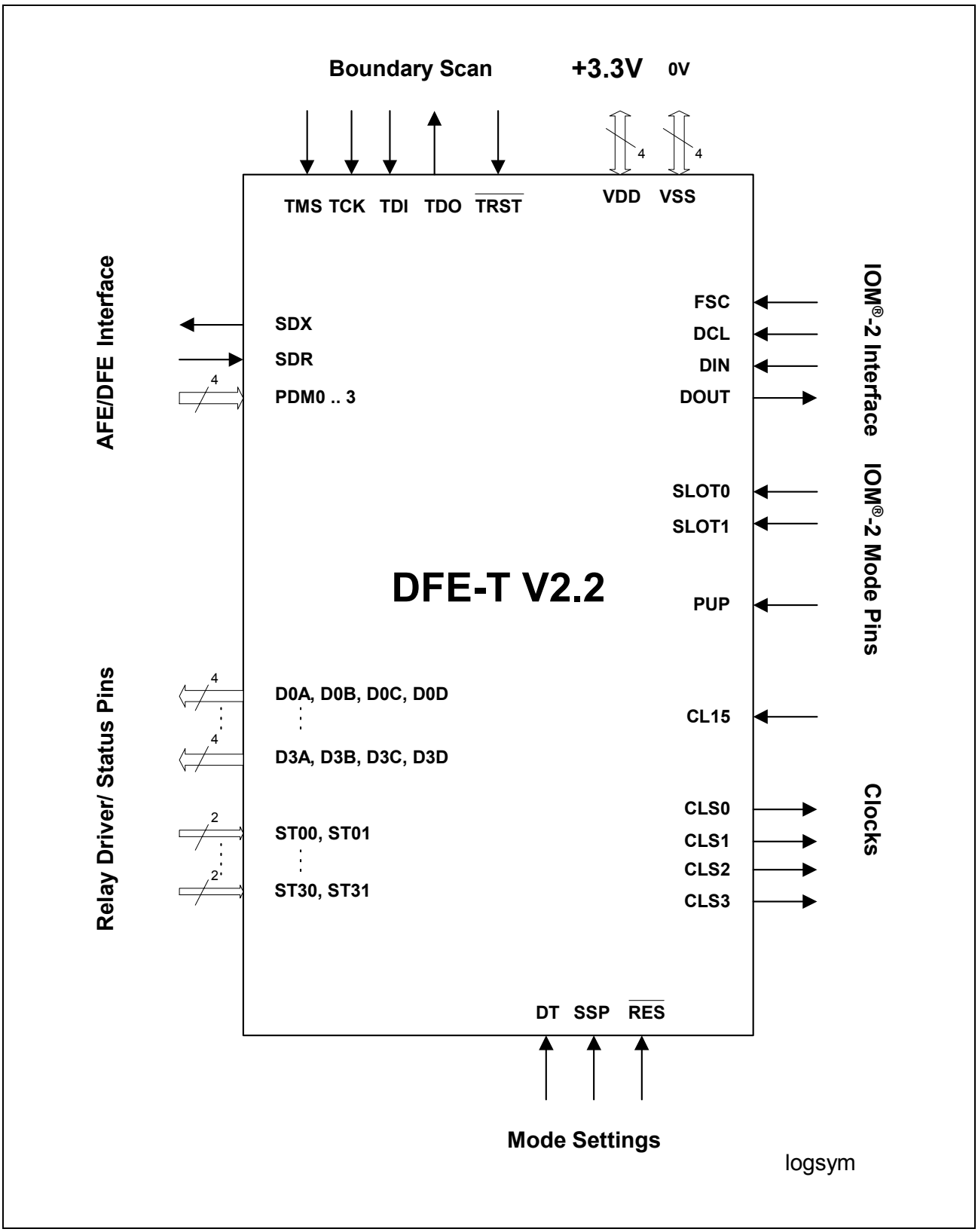


Figure 2 Logic Symbol

1.3 System Integration

This paragraph shows how the DFE-T V2.2 may be integrated in systems using other Infineon ISDN devices. The PEF 24901 V2.2 is optimized for use in the following applications:

- Digital Line Cards for Central Office
- Digital Line Cards for Access Networks (LT mode only)
- PBX applications (LT mode only)

Figure 3 illustrates a line card solution. The DELIC-PB (PEB 20571) supersedes the ELIC® (PEB 20550) and features up to 32 HDLC controllers on-chip. The DELIC controls up to 4 devices of DFE-T V2.2 on a single IOM®-2 interface. In this application an additional clock doubler is necessary to generate the 8.192 MHz DCL clock for the DFE-T derived from the 4.096 MHz BCL clock of the DELIC.

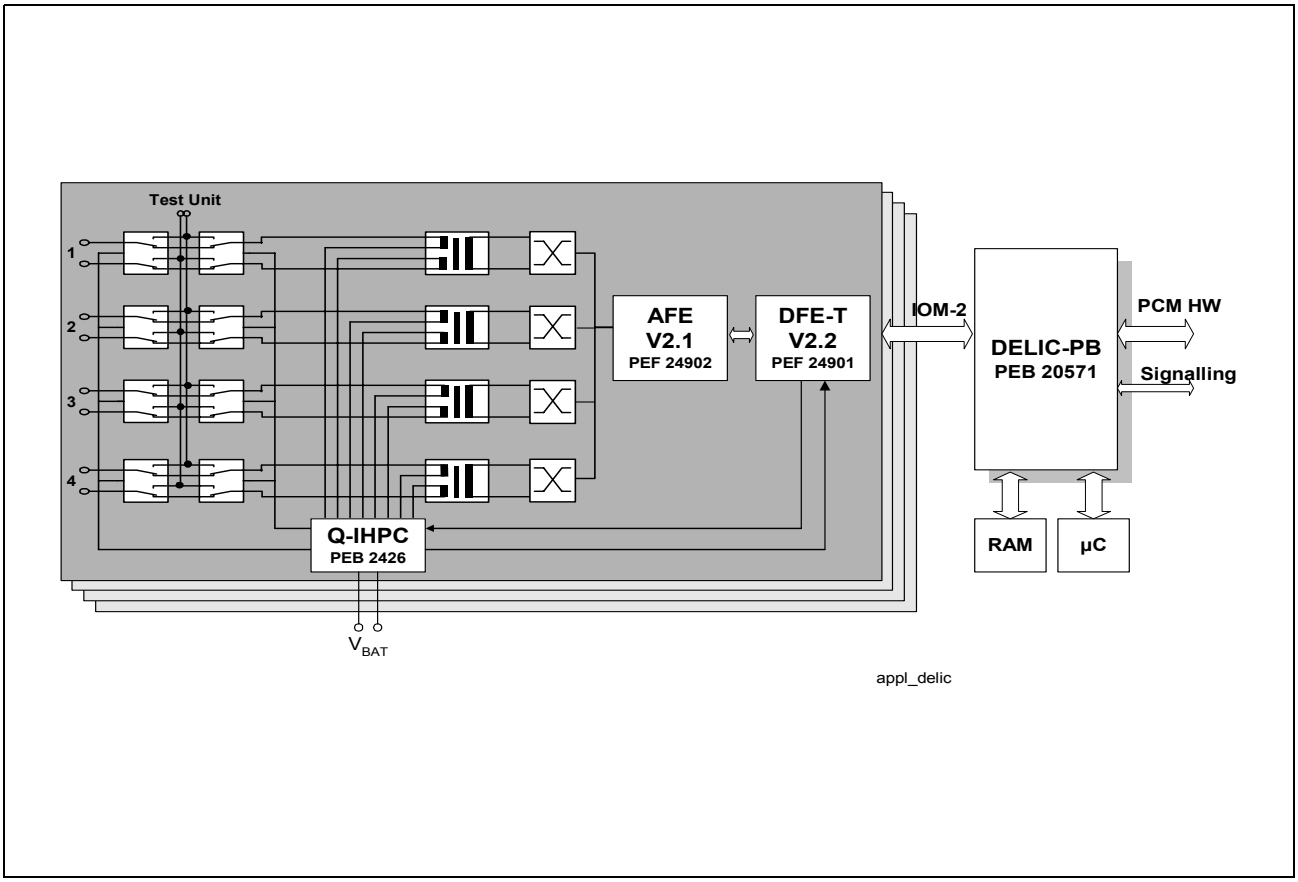


Figure 3 16-Line Card Application with DELIC-PB Solution

Figure 4 shows how a 8 channel line card application is realized by use of two AFE/ DFE-T chip sets:

One AFE PLL generates the synchronized 15.36 MHz clock and provides the master clock at pin CL15 for the other 3 devices. The internal PLL of the first AFE synchronizes the 15.36 MHz master clock onto a PTT reference clock of either 8 kHz or 2048 kHz. **Infineon recommends to feed the FSC clock input of the DFE-T V2.2 and the PLL reference clock input (pin CLOCK) of the AFE from the same clock source.**

The PLL of the second AFE is deactivated. The 15.36 MHz master clock is applied at pin CL15. CL15 is configured as input if XIN is clamped either to VDD or to VSS. Pin XOUT has to be left open and CLOCK shall be tied to GND.

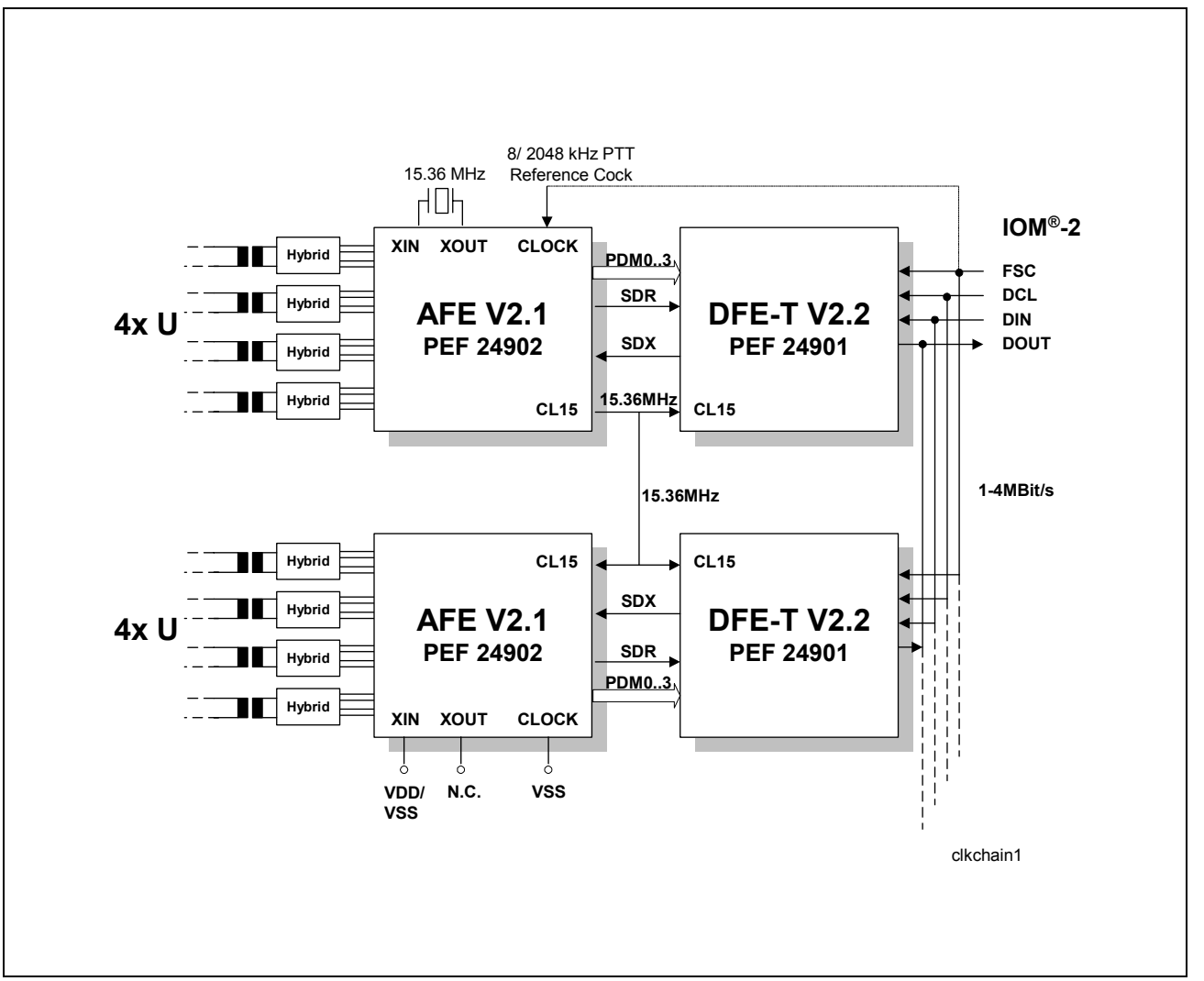


Figure 4 Connecting Two AFE/DFE-T Chip Sets

The DFE-T devices are supplied by the first AFE at pin CL15 with the synchronized 15.36 MHz clock. The IOM®-2 channels the DFE-T devices are assigned to can be programmed by the two slot pins. Starting from channel no. 0/4/8/12 always four subsequent channels are occupied.

Alternatively the clocking scheme as shown in **Figure 5** may be applied if more than 3 devices are to be clocked (e.g. in a 16-channel line card application). Instead to supply the 2nd AFE with the master clock at pin CL15, here the 15.36 MHz master clock is input at pin XIN. Thereby pin CL15 is configured as output and passes the 15.36 MHz clock on to the attached DFE-T. If the clock chain is extended in the same way by another two AFE/DFE-T chip sets a 16-channel line card application can be realized with just one single crystal. Note that the 15.36 MHz clock is inverted once by the AFE if it is input at XIN and output at CL15. This way the duty cycle is recovered again.

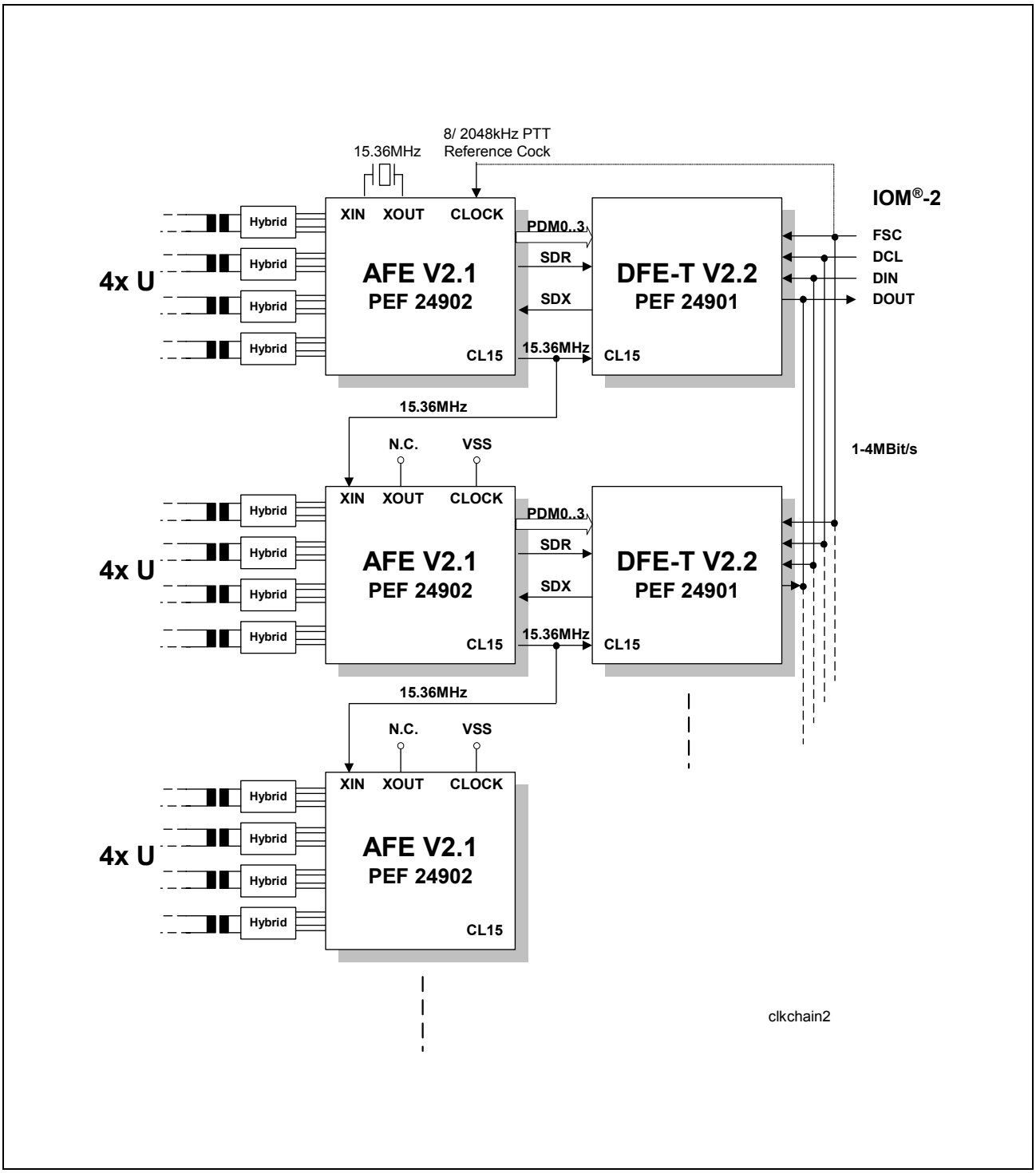


Figure 5 Recommended Clocking Scheme for More Than Two DFE-T/AFE Chip Sets

1.4 Operational Overview

The DFE-T V2.2 operates always in LT mode.

System Interface Configurations

The following parameters of the system interface are configurable:

- Open Drain/ Push-Pull Mode
  Configured as open drain the output pin DOUT is floating and a pull-up resistor is required. In push-pull mode the output pin is high impedance outside the active time slots.
- IOM®-2 Channel Assignment
  IOM®-2 channels are always assigned in blocks of four.

SLOT1	SLOT0	Assigned IOM®-2 Channels
0	0	0 .. 3
0	1	4 .. 7
1	0	8 .. 11
1	1	12 .. 15

- IOM®-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM®-2 Channels
2048	1024	4
3072	1536	6
4096	2048	8
6144	3072	12
8192	4096	16

Send Single Pulses Test Mode

In test mode 'Send Single Pulses' +1 pulses spaced by 1 ms are transmitted on all U lines. The test mode is activated by pin SSP= set to '1'. The SSP test function can be as well stimulated by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

Data Through Mode

In test mode ’Data Through’ the U-transceiver is forced to enter the ’Transparent’ state and to issue U4 independently of the wake-up protocol. The DT test mode is activated by pin DT= set to ’1’. The DT test function can be as well stimulated by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

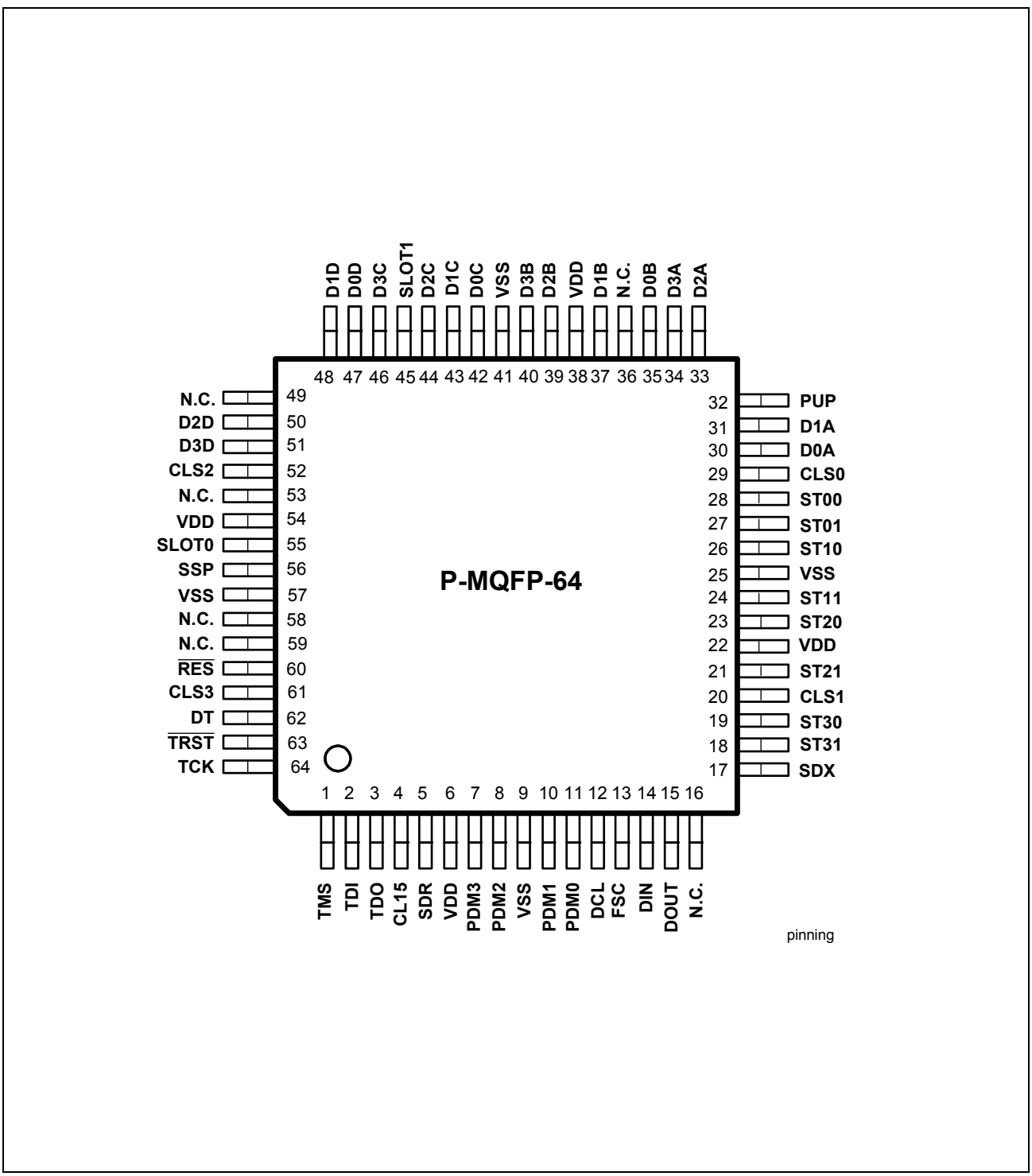


Figure 6 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
IOM®-2 Interface			
13	FSC	I	Frame Synchronization Clock (8 kHz) the start of the first B1-channel in time-slot 0 is marked, FSC is expected to be ’1’ for at least two DCL periods.
12	DCL	I	Data Clock clock rate ranges from 2048 to 8192 kHz (1024 to 4096 kBit/s)
14	DIN	I	Data In input of IOM®-2 data synchronous to DCL clock
15	DOUT	O (OD/PuP)	Data Out output of IOM®-2 data synchronous to DCL clock
Mode Selection Pins			
60	$\overline{\text{RES}}$	I	Reset triggers asynchronous HW reset, Schmitt trigger input ’1’= inactive ’0’= active (see **Table 3**)
55	SLOT0	I	IOM®-2 Channel Slot Selection 0 assigns IOM®-2 channels in blocks of 4 SLOT1, 0: ’00’= IOM®-2 channels 0 to 3 ’01’= IOM®-2 channels 4 to 7 ’10’= IOM®-2 channels 8 to 11 ’11’= IOM®-2 channels 12 to 15

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
45	SLOT1	I (PD)	IOM®-2 Channel Slot Selection 1 assigns IOM®-2 channels in blocks of 4
32	PUP	I (PD)	Push Pull Mode in push pull mode '0' and '1' is actively driven during an occupied time slot outside the active time slots DOUT is high impedance (tristate) '1'= configures DOUT as push/pull output '0'= configures DOUT as open drain output
56	SSP	I	Send Single Pulses (SSP) Test Mode enables/disables SSP test mode '1'= SSP test mode enabled, +1 pulses are issued at the four line ports in 1ms intervals '0'= SSP test mode disabled This pin function corresponds to the SW selection by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line *Note: For activation of SSP test mode, pin $\overline{RES}$ and pin DT must be inactive (see **Table 3**)*
62	DT	I	Data Through (DT) Test Mode enables/disables DT test mode '1'= DT test mode enabled, the U-transceiver is forced on all line ports to enter the 'Transparent' state '0'= DT test mode disabled This pin function corresponds to the SW selection by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line *Note: For activation of DT test mode, pin $\overline{RES}$ and pin SSP must be inactive (see **Table 3**)*