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Data Sheet, DS 3, July 2001

DFE-Q V2.1 Quad ISDN 2B1Q Echocanceller Digital Front End

PEF 24911 Version 2.1

Wired Communications

Infineon technologies

Never stop thinking.

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Data Sheet, DS 3, July 2001

DFE-Q V2.1
Quad ISDN 2B1Q Echocanceller Digital Front End

PEF 24911 Version 2.1

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Revision History:	**2001-07-16**	DS 3
Previous Version:	Data Sheet 11.00	DS 2

Page	Subjects (major changes since last revision)
Page 13	New function: Disable Super Frame Marker introduced on pin 16: DSFM
Page 13 **Page 13**, **Page 39**	Refined description of pin 49: CRCON Especially, CRCON = ’1’ selects MFILT= 0011 0xxx (erroneously, MFILT= 00010xx was documented in DS2)
Page 28	Added note: MON-12 read access is impossible in state ’Deactivated’
Page 43	Restriction: PACA/PACE must not be used during local loopback active
Page 54	C/I-command LTD added (function as in V1.x)
Page 63	AR0 and ARX set UOA = ’1’ (before: AR0 and ARX set UOA to the same value as the received SAI bit)
Page 95 **Page 130**	Refined description ’Framer / Deframer Loopback’: - always transparent - prerequisite is transparent state
Page 97	Bit Error Rate Counter: refined operational description
Page 103	Data Through is only test mode, C/I-command = ARL must not be applied when pin DT = ’1’
Page 113	Refined description of ’Control via MON-2’
Page 119	Removed ’Propagation Delay Measurement’: function not supported
Page 120	Refined description of mode register evaluation timing
Page 121	Removed description OPMODE.MODE1,0: no settings possible
Page 125 **Page 127**	SAI-evaluation / UOA-control: - M4RMASK.bit6: only SAI-reporting via MON-2 is selected - M4WMASK.bit6: in addition to UOA-bit control, also SAI-evaluation by the state machine is selected; refined description (see also **Figure 21** and **Figure 22**)
Page 129	Changed TEST.bit6 = ’1’ (not ’0’)
Page 130	Statemachine is put into transparent state by TRANS=’0’ (not ’1’)
Page 135	Refined reset timing description; added 900µs internal delay to figure
Page 136	Refined description of FSC / Superframe-FSC-timing
Page 137	**Table 21**: Max. connection resistance specified
Page 139	Removed input capacitance of pin XIN (pin XIN is not supported)

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1 Introduction

The Quad ISDN 2B1Q Echocanceller Digital Front End (DFE-Q) is the digital part of an optimized two-chip solution featuring 4x ISDN basic rate access and IDSL access at 144 kbit/s. The PEF 24911 is designed to provide in conjunction with the Quad ISDN Echocanceller Analog Front End (PEF 24902 V2.1) full duplex data transmission at the U-reference point according to ANSI T1.601 (1998), ETSI TS 102 080 (1998) and ITU-T G.961 standards.

The DFE-Q 2nd generation has been completely reengineered to guarantee the availability of the well proved DFE-Q/AFE solution over the year 2000. The PEF 24911 V2.1 is downwards pin compatible and functionally equivalent to the DFE-Q V1.x. Thus, line card manufacturers can make use of the most advanced process technology without the need to change their current design (besides the changeover to 3.3 V power supply).

No software changes are required if the DFE-Q V2.1 is deployed in existing DFE-Q V1.x solutions. Some new features are provided such as free programmable filtering options for the maintenance bits (M1-6) and enhanced monitoring and test functions. The data rate is programmable from 1 Mbit/s to 4 Mbit/s.

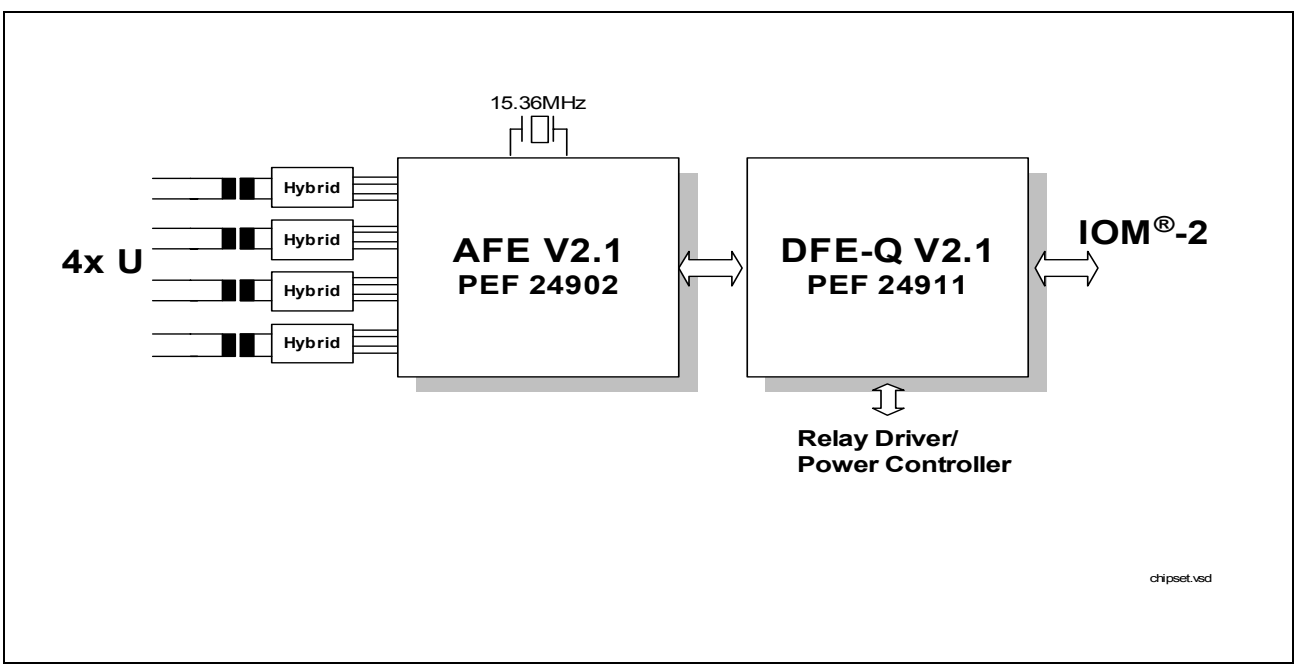


Figure 1 DFE-Q/ AFE 2nd Generation Chip Set

The output and input pins are throughout 5 V TTL compatible although the PEF 24911 is processed in advanced 3.3 V CMOS technology. A power down state with very low power consumption is featured.

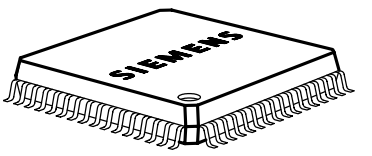
The PEF 24911 comes in a P-MQFP-64 package.

Quad ISDN 2B1Q Echocanceller Digital Front End DFE-Q V2.1

PEF 24911

Version 2.1

1.1 Features



P-MQFP-64

U-Interface

- Digital part of a two-chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access or IDSL access at 144 kbit/s
- Conforms to:
  - ANSI T1.601–1998
  - ETSI TS 102 080 (1998)
  - Recommendation ITU-T G.961
- 2B1Q-block code (2 binary, 1 quaternary) at 80-kHz symbol rate
- LT mode
- Data rate of the system interface programmable
- Activation/ deactivation controller
- 15 s start-up guard timer (T1) can be disabled for use in repeater applications
- Adaptive echo cancellation and equalization
- Automatic gain control and polarity adaptation
- Clock recovery (frame and bit synchronization) in all applications
- Built-in wake-up unit for activation from power-down state.

System Interface

- IOM®-2 interface with programmable data rates (1 Mbit/s to 4 Mbit/s)
- SW controlled I/O ports for relay driver and power feeder control
  - 4 relay driver pins per port
  - 2 status pins per port

Type	Package
PEF 24911	P-MQFP-64

Others

- Software compatible to PEF 24911 V1.3 (Quad IEC DFE-Q)
- Inputs and outputs 5 V TTL compatible
- DOUT (open drain) accepts pull-up to 3.3 V or 5 V
- +3.3 V ±0.3 V Power Supply
- Advanced low power CMOS technology
- Extended temperature range (– 40...to 85 °C)
- Boundary-Scan, JTAG IEEE 1149.1

Add-On Features and Differences with Respect to DFE-Q V1.3/V1.2/V1.1

- Max. IOM®-2 data rate 4 Mbit/s (DCL= 8 MHz)
- +3.3 V instead of +5 V power supply
- Dedicated pins for SSP and DT test modes
- DOUT configurable either as open drain or push-pull (tristate) output
- New MON-12 class features internal register access
- Coefficients retrievable by MON-12 commands instead of MON-8 commands
- Advanced filter options for MON-0 and MON-2 messages
- Bit Error Rate measurement per port
- Additional digital local loops
- C/I codes ’LTD’ and ’HI’ are no more supported
- Optimized LT-state machine
- JTAG Boundary-Scan with dedicated reset line $\overline{\text{TRST}}$ (replaces power-on reset functionality)

Addressed Applications

- ISDN Line Cards for Central Office
- ISDN Line Cards for Access Networks
- ISDN Line Cards in PBX Systems
- IDSL Line Cards

1.2 Logic Symbol

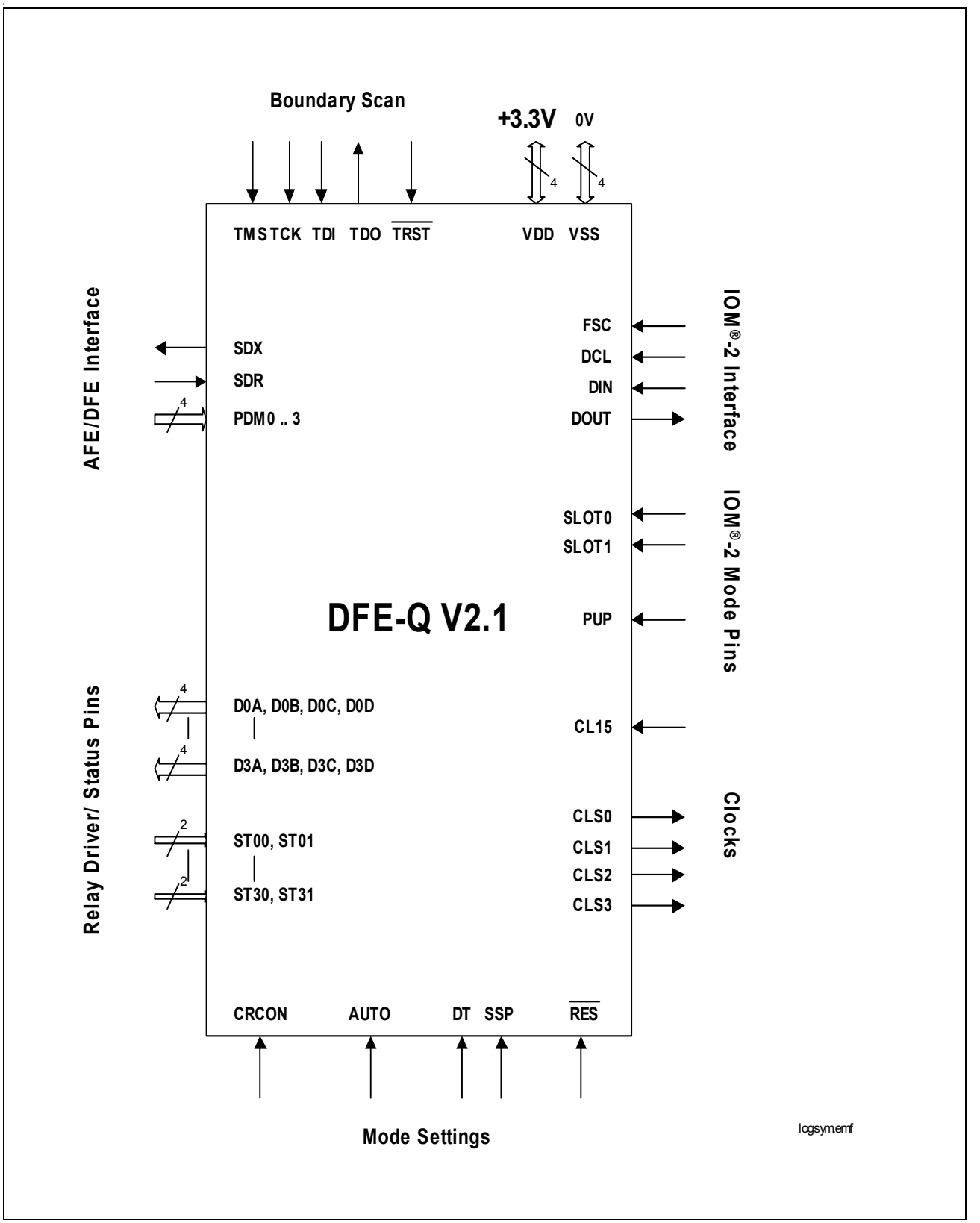


Figure 2 Logic Symbol

1.3 System Integration

This paragraph shows how the DFE-Q V2.1 may be integrated in systems using other Infineon ISDN devices. The PEF 24911 DFE-Q is optimized for use in the following applications:

- Digital Line Cards for Central Office
- Digital Line Cards for Access Networks (LT mode only)
- PBX applications (LT mode only)

Figure 3 and **Figure 4** illustrate line card solutions with various Infineon line card controllers. The DELIC-PB (PEB 20571) supersedes the ELIC® (PEB 20550) and will feature up to 32 HDLC controllers on-chip.The DELIC controls up to 4 devices of DFE-Q V2.1 on a single IOM®-2 interface. In this application an additional clock doubler is necessary to generate the 8.192 MHz DCL clock for the DFE-Q derived from the 4.096 MHz BCL clock of the DELIC.

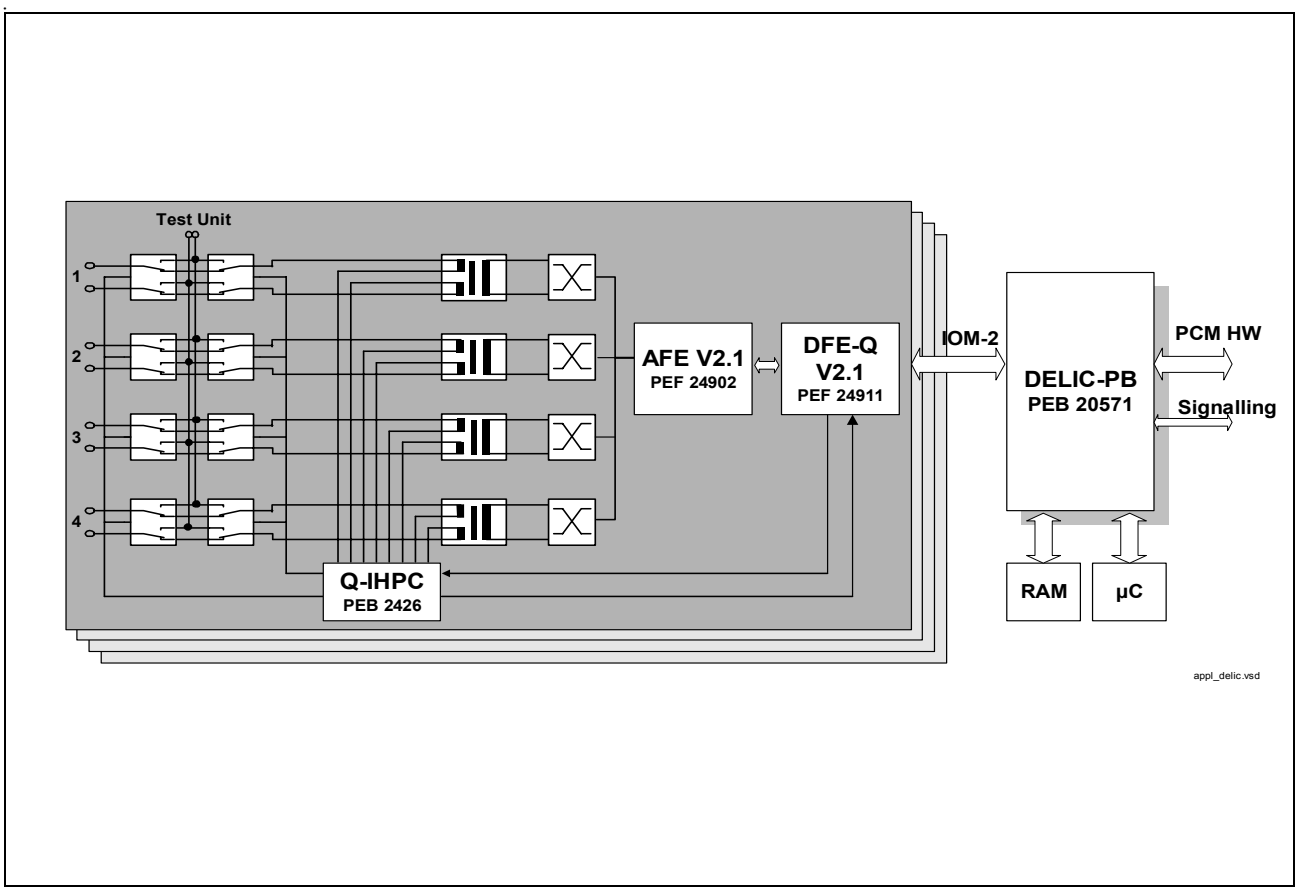


Figure 3 16-Line Card Application with DELIC Solution

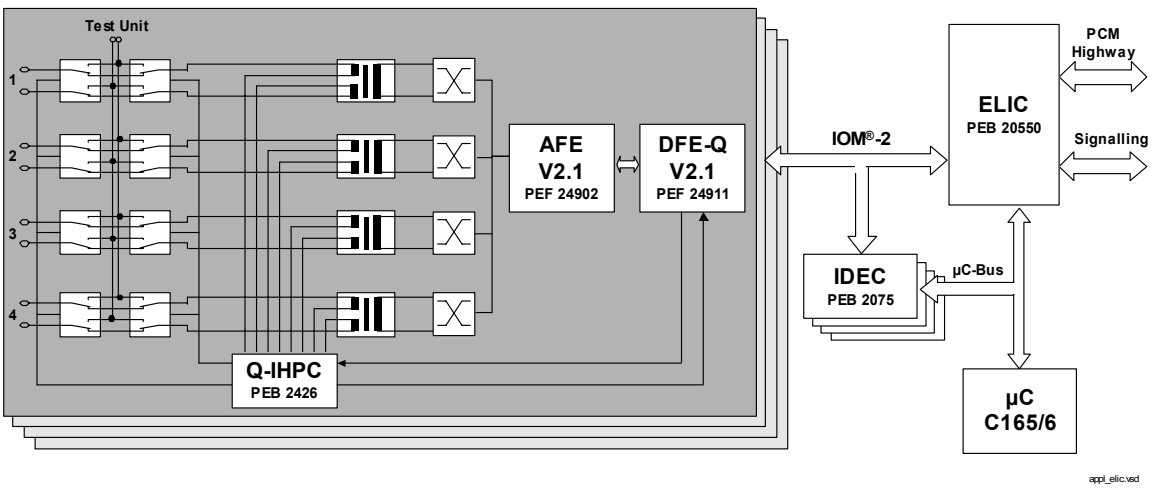


Figure 4 16-Line Card Application with ELIC®/ IDEC® Solution

Figure 5 shows how an 8 channel line card application is realized by use of two AFE/ DFE-Q chip sets:

One AFE-PLL generates the synchronized 15.36 MHz clock and provides the master clock at pin CL15 for the other 3 devices. The internal PLL of the first AFE synchronizes the 15.36 MHz master clock onto a PTT reference clock of either 8 kHz or 2048 kHz. **Infineon recommends to feed the FSC clock input of the DFE-Q V2.1 and the PLL reference clock input (pin CLOCK) of the AFE from the same clock source.**

The PLL of the second AFE is deactivated. The 15.36 MHz master clock is applied at pin CL15. CL15 is configured as input if XIN is clamped either to VDD or to VSS. Pin XOUT has to be left open and CLOCK shall be tied to GND.

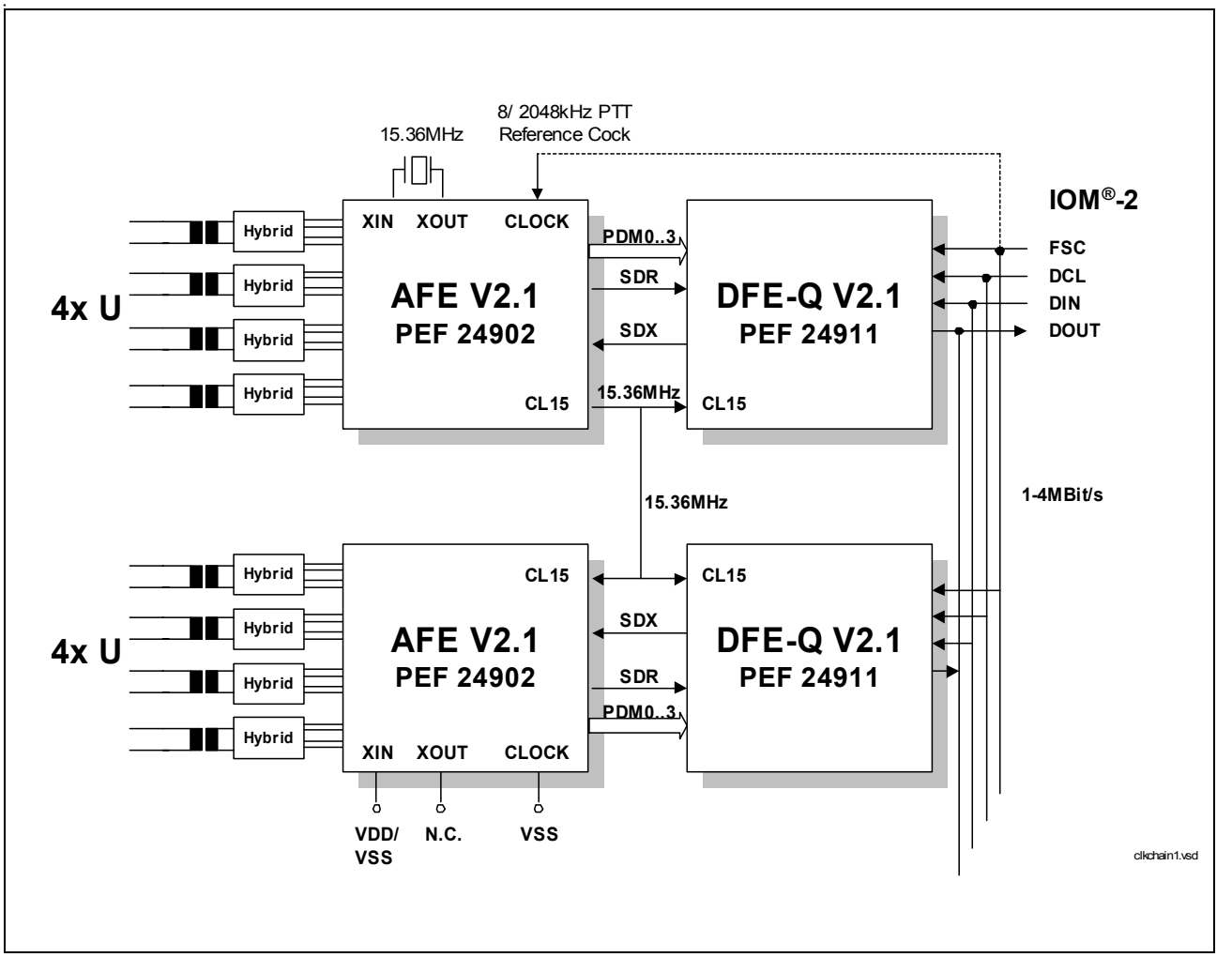


Figure 5 Connecting Two AFE/DFE-Q Chip Sets

The DFE-Q devices are supplied by the first AFE at pin CL15 with the synchronized 15.36 MHz clock. The IOM®-2 channels the DFE-Q devices are assigned to can be programmed by the two slot pins. Starting from channel no. 0/4/8/12 always four subsequent channels are occupied.

Alternatively the clocking scheme as shown in **Figure 6** may be applied if more than 3 devices are to be clocked (e.g. in a 16-channel line card application). Instead to supply the 2nd AFE with the master clock at pin CL15, here the 15.36 MHz master clock is input at pin XIN. Thereby pin CL15 is configured as output and passes the 15.36 MHz clock on to the attached DFE-Q. If the clock chain is extended in the same way by another two AFE/DFE-Q chip sets a 16-channel line card application can be realized with just one single crystal. Note that the 15.36 MHz clock is inverted once by the AFE if it is input at XIN and output at CL15. This way the duty cycle is recovered again.

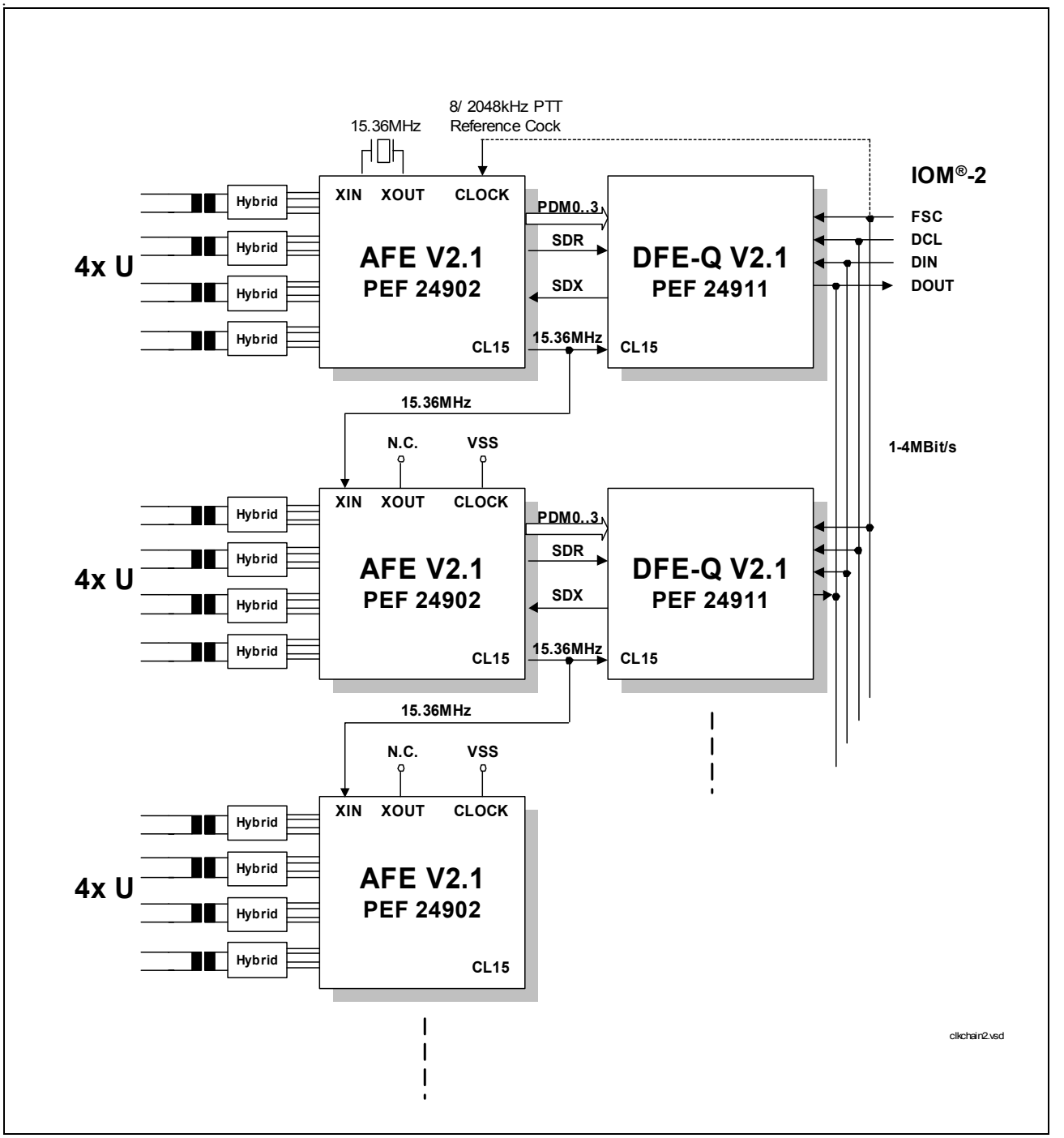


Figure 6 **Recommended Clocking Scheme for More Than Two DFE-Q/AFE Chip Sets**

1.4 Operational Overview

The DFE-Q V2.1 operates always in LT mode. Other operating modes known from former versions of the DFE-Q are not further supported.

System Interface Configurations

The following parameters of the system interface are configurable:

- Open Drain/ Push-Pull Mode
  Configured as open drain the output pin DOUT is floating and a pull-up resistor is required. In push-pull mode the output pin is high impedance outside the active time slots.

- IOM®-2 Channel Assignment
- IOM®-2 channels are always assigned in blocks of four.

SLOT1	SLOT0	Assigned IOM®-2 Channels
0	0	0 .. 3
0	1	4 .. 7
1	0	8 .. 11
1	1	12 .. 15

- IOM®-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM®-2 Channels
2048	1024	4
3072	1536	6
4096	2048	8
6144	3072	12
8192	4096	16

Send Single Pulses Test Mode

In test mode 'Send Single Pulses' +/-3 pulses spaced by 1.5 ms are transmitted on all U lines. The test mode is activated by pin SSP= set to '1'. The SSP test function can be as well stimulated by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

Data Through Mode

In test mode ’Data Through’ the U-transceiver is forced to enter the ’Transparent’ state and to issue SL3T (see **Table 12**) independently of the wake-up protocol. The DT test mode is activated by pin DT= set to ’1’. The DT test function can be as well stimulated by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

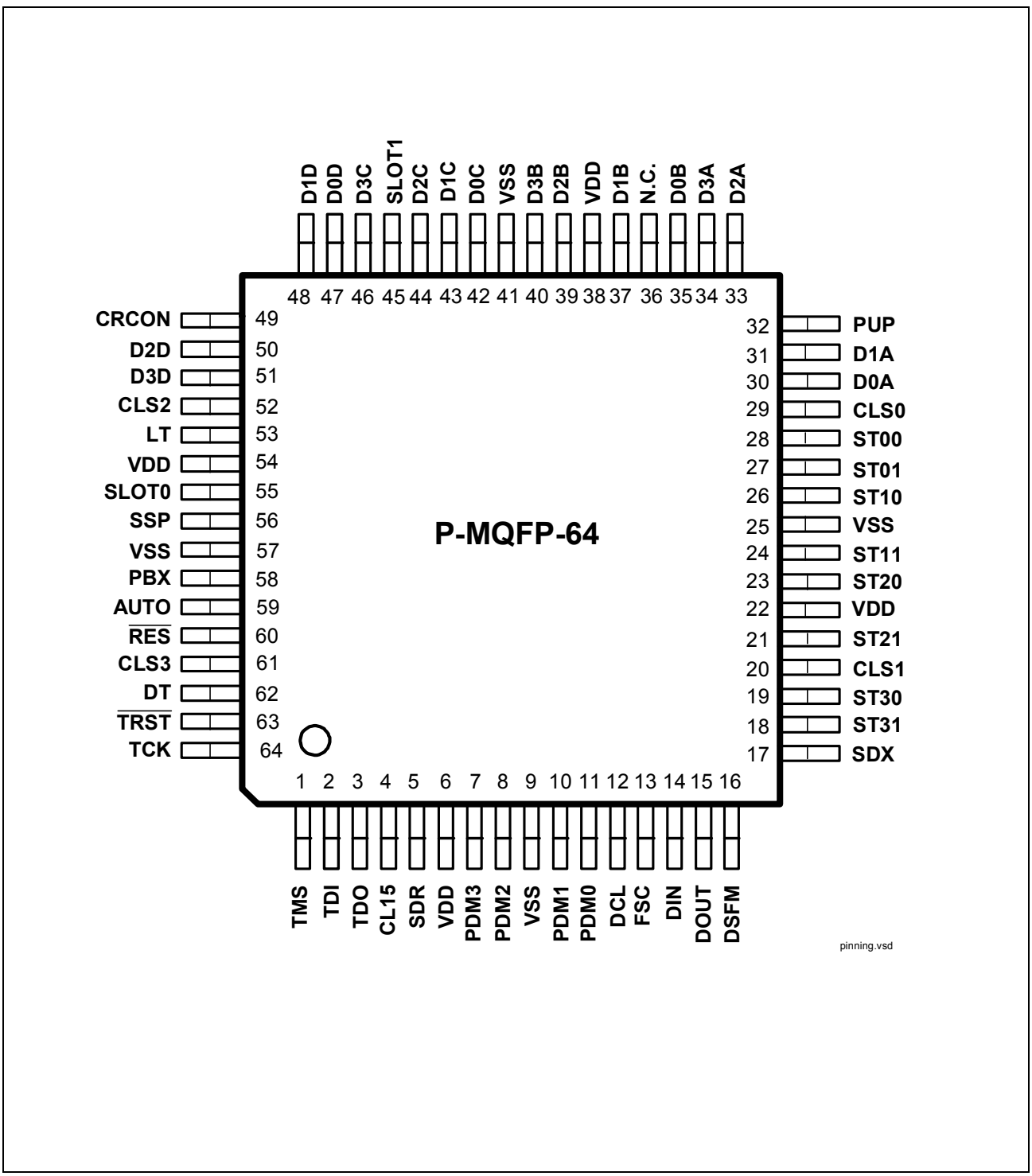


Figure 7 Pin Configuration (63 of 64 used)

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
IOM®-2 Interface			
13	FSC	I	Frame Synchronization Clock (8kHz) the start of the first B1-channel in time-slot 0 is marked, FSC is expected to be ’1’ for at least two DCL periods.
12	DCL	I	Data Clock clock rate ranges from 2048 to 8192 kHz (1024 to 4096 kBit/s)
14	DIN	I	Data In input of IOM®-2 data synchronous to DCL clock
15	DOUT	O (OD/ PuP)	Data Out output of IOM®-2 data synchronous to DCL clock
Mode Selection Pins			
60	$\overline{\text{RES}}$	I	Reset triggers asynchronous HW reset, Schmitt trigger input ’1’= inactive ’0’= active
55	SLOT0	I	IOM®-2 Channel Slot Selection 0 assigns IOM®-2 channels in blocks of 4 SLOT1, 0: ’00’= IOM®-2 channels 0 to 3 ’01’= IOM®-2 channels 4 to 7 ’10’= IOM®-2 channels 8 to 11 ’11’= IOM®-2 channels 12 to 15
45	SLOT1	I (PD)	IOM®-2 Channel Slot Selection 1 assigns IOM®-2 channels in blocks of 4

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
16	DSFM	I (PD)	Disable Super Frame Marker '1' = Inhibits the evaluation of the super frame marker on FSC. I.e the transmitted super-frame is not affected by an FSC pulse shorter than 2 DCL clock periods. '0' = The position of the transmitted superframe is synchronized to short FSC pulses.
32	PUP	I (PD)	Push Pull Mode in push pull mode '0' and '1' is actively driven during an occupied time slot, outside the active time slots DOUT is high impedance (tristate) '1'= configures DOUT as push/pull output '0'= configures DOUT as open drain output
49	CRCON	I (PD)	CRC Check On/Off defines the condition on which MON-2 messages and M4 bit will be passed on, the setting has effect on all ports (see **Table 7**). Pin CRCON is evaluated only after hardware reset. '1'= CRC Check On MON-2 messages are not issued and M4-bit are not forwarded to the statemachine if the CRC-check of the U-superframe containing M4-bit changes is not ok. (MFILT= 0011 0xxx) '0'= CRC Check Off MON-2 messages are issued every time a change in at least one of the overhead bits (M4,5,6) of the U-interface is detected, regardless of the CRC checksum status. M4-bit are forwarded to the statemachine with triple-last-look filtering (TLL). (MFILT= 0000 0xxx)
53	LT	I	reserved, clamp to high

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
58	PBX	I	reserved, clamp to low
59	AUTO	I	EOC Auto Mode selects auto or transparent mode for EOC channel processing, the setting has effect on all ports '1'= EOC auto mode (MFILT= xxxx x100) '0'= EOC transparent mode (MFILT= xxxx x001)
56	SSP	I	Send Single Pulses (SSP) Test Mode '1'= alternating +/-3 pulses are issued at all line ports in 1.5 ms intervals '0'= deactivated, clamp to GND if not used This pin function corresponds to the SW selection by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line
62	DT	I	Data Through (DT) Test Mode enables/disables DT test mode '1'= DT test mode enabled, the U-transceiver is forced on all line ports to enter the 'Transparent' state '0'= DT test mode disabled This pin function corresponds to the SW selection by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line
Interface to the Analog Front End			
4	CL15	I	15.36 MHz Master Clock Input
11	PDM0	I	Pulse Density Modulated Receive Data of Line Port 0 pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
10	PDM1	I	Pulse Density Modulated Receive Data of Line Port 1 pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
8	PDM2	I	Pulse Density Modulated Receive Data of Line Port 2 pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
7	PDM3	I	Pulse Density Modulated Receive Data of Line Port 3 pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
5	SDR	I	Serial Data Receive Line interface signal from the PEF 24902 Quad AFE that transports level detect information for the wake-up recognition of all 4 lines by use of TDM
17	SDX	O	Serial Data Transmit Line interface to the PEF 24902 Quad AFE for the transmit and control data. Transmission is based on clock CL15 (15.36 Mbit/s). For each line port the following bits are exchanged: TD0, TD1: Transmit data RANGE: Range select LOOP: Analog loopback switch PDOW: Power down/power up Synchronization information