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Data Sheet, Rev. 2, Jan. 2005

TE3-LIU™

Line Interface Unit for DS3, STS1 and E3

PEF 3452, Version 1.3

Wireline Communications

Never stop thinking.

Edition 2005-01-24

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Revision History:	**2005-01-24**	Rev. 2
Previous Version:	**Preliminary Data Sheet TE3-LIU V1.3, 2001-12-05, DS1**	

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Preface

The PEF 3452 (TE3-LIU™) is a flexible line interface unit for a wide area of telecommunication and data communication applications. The device is addressed to fulfill all requirements to build a DS3, STS-1 or E3 line interface.

Organization of this Document

This Data Sheet is organized as follows:

- **Overview**
  Gives a general description of the product, lists the key features, and presents some typical applications.
- **Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
- **Functional Description**
  Describes the functional blocks and principle operation modes.
- **Interface Description**
  Describes the device interfaces.
- **Operational Description**
  Shows the operation modes and how their initialization.
- **Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.
- **Package Outlines**
  Shows the mechanical values of the device package.
- **Appendix**
- **Index**

Related Documentation

This document refers to the following international standards
(in alphabetical/numerical order):

ACA TS016 (general requirements for Australia)

CTR-24/TBR-24 (E3 requirements)

ETS 300 166 (E3 transmit return loss)

ITU-T G.703 (E3 pulse mask, B3ZS/HDB3 code, E3 receive return loss)

ITU-T G.751 (jitter requirements E3)

ITU-T G.775 (loss of signal definition)

ITU-T G.823 (jitter requirements E3)

ITU-T G.824 (jitter requirements DS3)

ITU-T O.151 (pseudo random binary sequence (PRBS) definition)

GR-253-CORE (STS-1 jitter requirements)

GR-499-CORE (DS3 pulse mask, DS3 jitter requirements)

ANSI T1.102 (STS-1 pulse mask)

ANSI T1.102 Annex B (DS3 monitoring)

ANSI T1.231 (maintenance functions, defect definitions)

ANSI T1.404 (DS3 pulse mask)

MIL-STD 883D (ESD requirements)

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We welcome your comments on this document. We are continuously trying improving our documentation. Please send your remarks and suggestions by e-mail to

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Please provide in the *subject* of your e-mail:
device name (TE3-LIU™), device number (PEF 3452), device version (Version 1.3),

and in the *body* of your e-mail:
document type (Data Sheet), issue date (2005-01-24) and document revision number (Rev. 2).

1 Overview

The TE3-LIU™ PEF 3452 Line Interface Unit is used to connect a DS3/STS-1 or E3 framer device to an analog transmission line. The line interface fulfills the relevant standards for DS3 (44.736 Mbit/s), STS-1 (51.840 Mbit/s) and E3 (34.368 Mbit/s) systems.

The TE3-LIU™ comes in a P-MQFP-44-2 package (SMD) to save a significant amount of board space. The integrated jitter attenuation further reduces overall system complexity and cost.

This CMOS 3.3 V low power device contains an integrated pulse shaper to drive any line length within the range of up to 1100 ft. without the need for external length selection (Line Build Out).

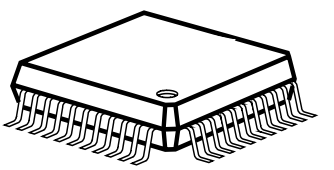
The hardware configuration mode allows low cost systems with flexible device setting without the need for a microprocessor.

An optional microprocessor mode allows the connection to a standard microprocessor bus to control hardware settings.

Line Interface Unit for DS3, STS1 and E3 PEF 3452
TE3-LIU™

Version 1.3

1.1 Features



P-MQFP-44-2

- Generic analog interface for all DS3/STS-1/E3 applications
- Single chip solution for receive and transmit direction
- 3.3 V low power device
- Integrated receive equalization network
- Integrated noise and crosstalk filter
- Clock and data recovery using an integrated PLL with ultra-low intrinsic jitter
- Transmit clock duty cycle correction PLL
- No external components required for clock and data recovery and receive equalizer
- DSX receive line monitor (additional 20 dB gain according to ANSI T1.102)
- Low transmitter output impedances for high transmit return loss
- Disable function of the analog transmit line outputs
- Transmit pulse shaper to fulfill requirements of ANSI T1.404, Telcordia GR-499-CORE, ANSI T1.102 and ITU-T G.703 (E3)
- Maximum line length up to 1100 ft. (using standard coaxial cable, for example AT&T 728A, 734A or 734D)
- External line length selection (LBO) is not required
- Jitter specifications of GR-499-CORE and ITU-T G.823 are met
- Integrated jitter attenuation PLL and buffer in transmit direction
- Dual or single rail digital inputs and outputs from/to the framer interface
- Selectable line codes (HDB3 (E3), B3ZS (DS3/STS-1), AMI)
- Analog and digital loss of signal detection and indication
- Automatic RDOP/RDON blanking option in case of LOS
- Bipolar violation indication
- Local loop and remote loop for diagnostic purposes
- Insertion of alarm indication signal ("all ones")
- Flexible hardware or software controlled device configuration
- Device power down function

Type	Package
PEF 3452	P-MQFP-44-2

Hardware Interface Mode

- DS3/STS-1 or E3
- Line Coding (E3: HDB3 or AMI; DS3/STS-1: B3ZS or AMI)
- Transmitter disable
- Power down
- Remote loop
- Local loop
- Single/dual rail operation
- Receive clock edge selection
- Transmit clock edge selection
- Transmit "all ones"
- Receive line monitoring mode
- Automatic RDOP/RDON blanking option
- Jitter attenuation
- Loss of signal indication
- Bipolar violation indication

Microprocessor Interface Mode

- Microprocessor bus compatible interface
- Hardware control lines directly accessible

General

- CMOS device
- P-MQFP-44-2 package (body size 10 mm × 10 mm, lead pitch 0.8 mm)
- Single power supply: 3.3 V ± 5%
- 5V-tolerant digital input lines
- Temperature range of -40°C to +85°C
- Low power device

Applications

- Interface for SONET/DS3 and E3 network equipment
- WAN gateways
- CSU/DSU
- Multiplexers
- Digital crossconnect systems
- DS3/STS-1/E3 Test Equipment

1.2 Logic Symbol

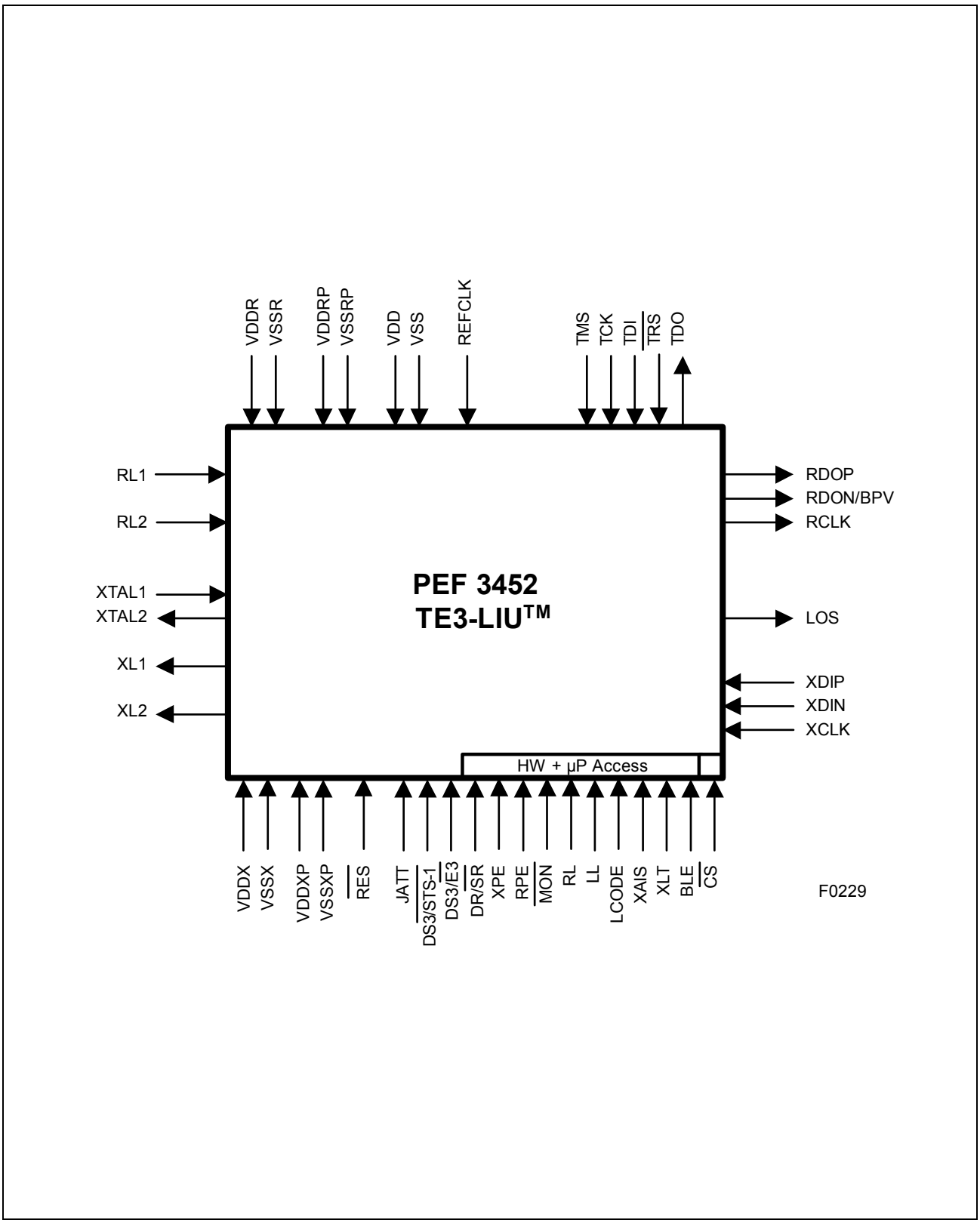


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 to **Figure 4** show typical applications using the TE3-LIU™.

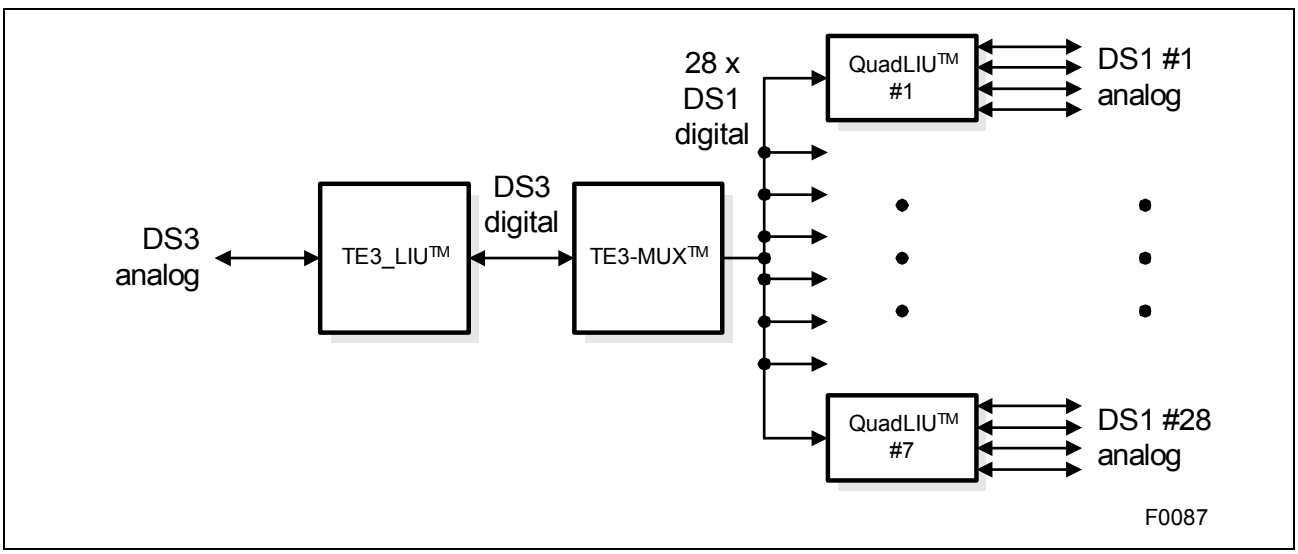


Figure 2 T3/T1 Multiplexer Application

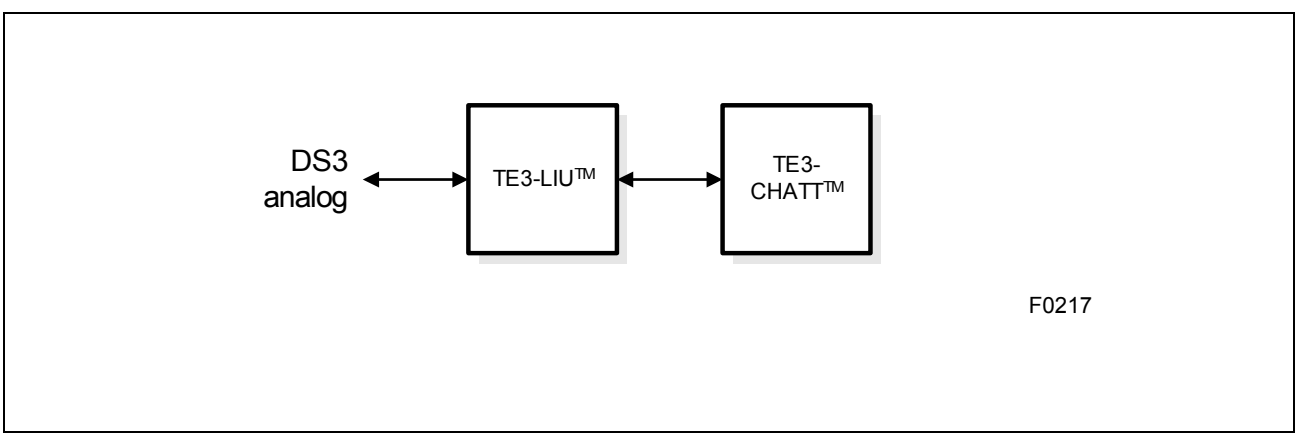


Figure 3 Channelized T3 Link Layer Application

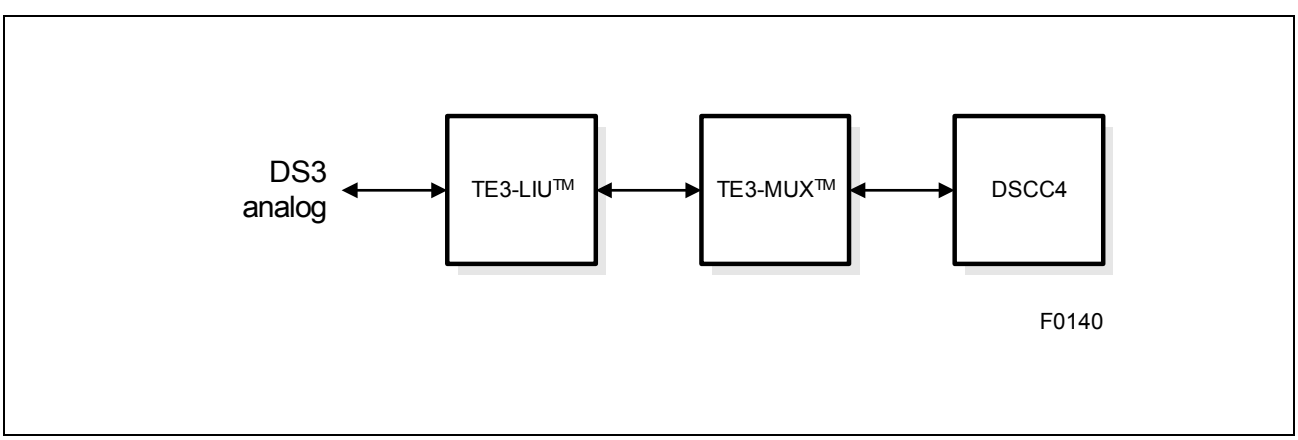


Figure 4 Unchannelized T3 Link Layer Application

*Note: TE3-MUX™ (PEB 3445) is an M13 **MU**ltiple**X**er/demultiplexer with an integrated DS3 framer*

*QuadLIU™ (PEB 22504) is a **4**-channel **L**ine **I**nterface **U**nit for E1/T1/J1*

*DSCC4™ (PEB 20534) is a 4-channel **S**erial **C**ommunication **C**ontroller*

*TE3-CHATT™ (PEB 3456) is a **CHA**nnelized **T**3 **T**ermination with DS3 Framer, M13 Multiplexer, T1/E1 Framers and 256 Channel HDLC/PPP controller*

2 Pin Descriptions

2.1 Pin Diagram

P-MQFP-44-2 (top view)

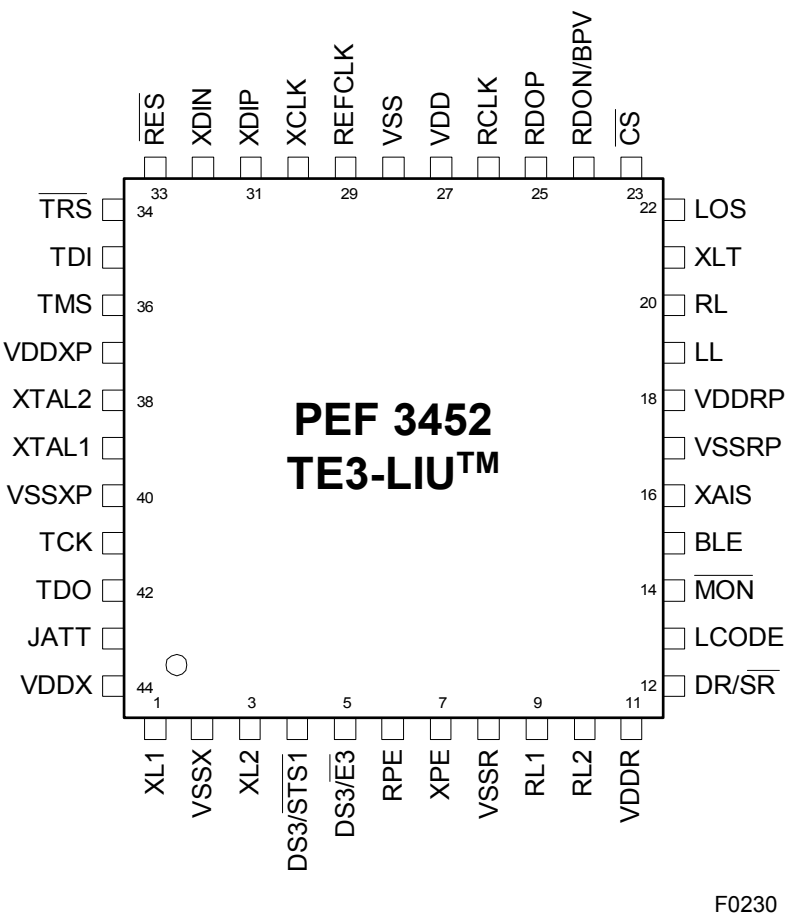


Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Interface Pin Functions

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
Receive Direction			
9	RL1	I (analog)	**Line Receiver 1** Analog input from the external transformer (receive bipolar ring). The signal at RL1 must be coded according to B3ZS or HDB3.
10	RL2	I (analog)	**Line Receiver 2** Analog input from the external transformer (receive bipolar tip). The signal at RL1 must be coded according to B3ZS or HDB3.
25	RDOP	O	**Receive Data Output/Positive** Received data at RL1/2 is sent on RDOP/RDON to the framer interface. Data is clocked with the rising or falling edge of RCLK, depending on RPE. In single rail mode (DR/$\overline{SR}$=0), data is sent in NRZ format.
24	RDON	O	**Receive Data Output/Negative** If dual rail data format is selected, the negative data signal is output on RDON/BPV.
	BPV		**Bipolar Violation** If single rail data format is selected, the bipolar violation indication signal is output on RDON/BPV. BPV is synchronized on RCLK.
26	RCLK	O	**Receive Clock** Receive Clock extracted from the incoming data pulses. The active clock edge is determined by RPE. During LOS, a clock signal is generated internally and driven on RCLK (derived from REFCLK).

Table 1 Interface Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
Transmit Direction			
1	XL1	O (analog)	**Transmit Line 1** (transmit bipolar ring) Analog output to the external transformer. XL1 can be switched into inactive mode.
3	XL2	O (analog)	**Transmit Line 2** (transmit bipolar tip) Analog output to the external transformer. XL2 can be switched into inactive mode.
31	XDIP	I + PU	**Transmit Data In/Positive** Transmit data received from the framer interface to be output on XL1/2. NRZ or dual rail positive data has to be provided at XDIP. Latching of data is done with the rising or falling transitions of XCLK, depending on XPE.
32	XDIN	I + PU	**Transmit Data In/Negative** If dual rail format is selected, negative data signal is read from XDIN. If single rail data format is selected, data on XDIN is ignored. Latching of data is done with the rising or falling transitions of XCLK, depending on XPE.
30	XCLK	I + PU	**Transmit Clock** Input of the working clock for the transmitter. The active clock edge is determined by XPE. DS3: 44.736 MHz STS-1: 51.840 MHz E3: 34.368 MHz To fulfill e.g. ITU-T G.832 a clock accuracy of 20 ppm is required. For correct function a clock signal has always to be supplied to XCLK.

Table 1 Interface Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
Global Clock Reference			
29	REFCLK	I	**Reference Clock** REFCLK is the basic internal clock. It must be stable during reset and operation. This clock is also used to synchronize the receive PLL in case of no signal. The clock frequency depends on the target application: DS3: 44.736 MHz STS-1: 51.840 MHz E3: 34.368 MHz To fulfill e.g., ITU-T G.832 a clock accuracy of 20 ppm is required.
39	XTAL1	I	**Jitter Attenuation Reference** Connection for an external pullable crystal. DS3: 14.912 MHz STS-1: 17.280 MHz E3: 11.456 MHz If jitter attenuation is disabled (default), XTAL1 is internally driven to a fixed level (not floating).
38	XTAL2	O	

Table 2 Control Pin Functions

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
33	$\overline{RES}$	I	**Hardware Reset** A low signal at this pin forces the device into reset state.
23	$\overline{CS}$	I + PU	**Chip Select** 0 = hardware control signals are switched through 1 = hardware control signals are ignored
5	DS3/$\overline{E3}$	I + PU	**DS3/STS-1 or E3 Select** Primary mode selection. This signal has to be stable during reset and may not change afterwards. It must not be connected to a µP bus. 0 = E3 1 = DS3 or STS-1 (see DS3/$\overline{STS-1}$)
4	DS3/$\overline{STS-1}$	I + PU	**DS3 or STS-1 Select** Primary mode selection. This signal has to be stable during reset and may not change afterwards. It must not be connected to a µP bus. 0 = STS-1 1 = DS3
13	LCODE	I + PU	**Line Code Select** for receive and transmit direction E3: 0 = AMI 1 = HDB3 DS3/STS-1: 0 = AMI 1 = B3ZS
16	XAIS	I + PU	**Transmit Alarm Indication** 0 = no AIS 1 = AIS all-ones insertion

Table 2 Control Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
20	RL	I + PU	**Remote Loop Switching** 0 = no loop 1 = Remote Loop[1)]
19	LL	I + PU	**Local Loop Switching** 0 = no loop 1 = Local Loop[1)]
21	XLT	I + PU	**Transmitter inactive** 0 = transmitter enabled 1 = transmitter disabled (outputs 1.5 V common mode voltage)
14	$\overline{\text{MON}}$	I + PU	**Line Monitoring Mode** 0 = additional 20 dB gain at RL1/RL2 1 = normal
15	BLE	I + PU	**Blanking Enable** 0 = detected signal is switched through even in case of LOS 1 = all-zero signal is sent on RDOP/RDON in case of LOS, REFCLK is used to drive RCLK
12	DR/$\overline{\text{SR}}$	I + PU	**Dual Rail/Single Rail Select** The framer interface is operated either in dual rail or single rail mode. In single rail mode, the BPV signal is output on RDON/BPV and input on XDIN is ignored. 0 = single rail 1 = dual rail
6	RPE	I + PU	**RCLK Positive Edge Selection** 0 = RDOP, RDON are clocked with negative (falling) edge of RCLK 1 = RDOP, RDON are clocked with positive (rising) edge of RCLK
7	XPE	I + PU	**XCLK Positive Edge Selection** 0 = XDIP, XDIN are clocked with negative (falling) edge of XCLK 1 = XDIP, XDIN are clocked with positive (rising) edge of XCLK

Table 2 Control Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
43	JATT	I + PD	**Jitter Attenuation Enable** This signal has to be stable during reset and may not change afterwards. It must not be connected to a µP bus. 0 = no jitter attenuation (default if left open) 1 = jitter attenuation in transmit direction
22	LOS	O	**Loss of Signal Indication** 0 = correct signal 1 = loss of signal LOS is synchronized on RCLK. During LOS, a clock signal is generated internally and driven on RCLK.

1) If RL=LL=1, the device is set into power down mode.

Table 3 Power Supply Pins

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
11	V_{DDR}	S (analog)	**Positive Power Supply** for the analog receiver
8	V_{SSR}	S (analog)	**Power Supply Ground** for the analog receiver
44	V_{DDX}	S (analog)	**Positive Power Supply** for the analog transmitter
2	V_{SSX}	S (analog)	**Power Supply Ground** for the analog transmitter
18	V_{DDRP}	S (analog)	**Positive Power Supply** for the analog receiver PLL
17	V_{SSRP}	S (analog)	**Power Supply Ground** for the analog receiver PLL
37	V_{DDXP}	S (analog)	**Positive Power Supply** for the analog transmitter PLL
40	V_{SSXP}	S (analog)	**Power Supply Ground** for the analog transmitter PLL
27	V_{DD}	S	**Positive Power Supply** for digital subcircuits and the digital receiver output
28	V_{SS}	S	**Power Supply Ground** for digital subcircuits and the digital receiver output

Table 4 Test Pins[1)]

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
34	$\overline{TRS}$	I + PU	**TAP Controller Reset** Active low test controller reset; this pin must be connected to $\overline{RST}$ or V_{SS}
35	TDI	I + PU	**Test Data Input**
36	TMS	I + PU	**Test Mode Select**
41	TCK	I + PU	**Test Clock**
42	TDO	O	**Test Data Output**

1) These pins are used for factory test only; boundary scan mode is not provided.

Note: PU = input or input/output comprising an internal pullup device
PD = input or input/output comprising an internal pulldown device

To override the internal pullup (pulldown) by an external pulldown (pullup), a resistor value of 47 kΩ is recommended.

Unused pins containing pullups or pulldowns can be left open.

3 Functional Description

3.1 Functional Overview

The TE3-LIU™ device contains analog and digital functional blocks, which are configured and controlled by direct hardware or microprocessor control.

The main interfaces are

- Receive Line Interface
- Transmit Line Interface
- Framer Interface
- Hardware Interface

The main internal functional blocks are

- Analog line receiver with noise & crosstalk filter, equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper
- Central clock generation module
- Jitter attenuator
- Maintenance functions (e.g., loop switching local or remote)
- Hardware/microprocessor control interface