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Data Sheet, DS 1, Nov. 2001

T-SMINTO
4B3T Second Gen. Modular ISDN NT (Ordinary)

PEF 80902 Version 1.1

Wired Communications

Infineon technologies

Never stop thinking.

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Revision History: **2001-11-12** DS 1

Previous Version: Preliminary Data Sheet 06.01

Page	Subjects (major changes since last revision)
Table 10 **Figure 12** **Chapter 2.3.7.4**	Additional C/I-command LTD
Chapter 4.2	Input Leakage Current AIN, BIN: max. 30µA
Chapter 4.4	Reduced power consumption

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1 Overview

The **PEB 80902** (T-SMINT®O) offers all NT1 features known from the PEB 8090 [9] and can hence replace the latter in all NT1 applications.

Table 1 on **Page 1** summarizes the 2nd generation NT products.

Table 1 NT Products of the 2nd Generation

	PEF 80902	PEF 81902	PEF 82902
	T-SMINT®O	**T-SMINT®IX**	**T-SMINT®I**
Package	P-MQFP-44	P-MQFP-64 P-TQFP-64	P-MQFP-64 P-TQFP-64
Register access	no	U+S+HDLC+ IOM®–2	U+S+IOM®–2
Access via	n.a	parallel (or SCI or IOM®–2)	parallel (or SCI or IOM®–2)
MCLK, watchdog timer, SDS, BCL, D-channel arbitration, IOM®–2 access and manipulation etc. provided	no	yes	yes
HDLC controller	no	yes	no
NT1 mode available	yes (only)	no	no

1.1 References

[1] TS 102 080, Transmission and Multiplexing; ISDN basic rate access; Digital transmission system on metallic local lines, ETSI, November 1998

[2] FTZ 1 TR 220 Technische Richtlinie, Spezifikation der ISDN Schnittstelle Uk0 Schicht 1, Deutsche Telecom AG, August 1991

[3] TS 0284/96 Technische Spezifikation Intelligenter Netzabschluß (iNT) mit den Funktionen eines Terminaladapters TA 2a/b (ohne Internverkehr), Deutsche Telekom AG, März 2001

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[5] T1.605-1991, ISDN-Basic Access Interface for S and T Reference Points (Layer 1 Specification), ANSI, 1991

[6] I.430, ISDN User-Network Interfaces: Layer 1 Recommendations, ITU, November 1988

[7] IEC-T, ISDN Echocancellation Circuit, PEB 20901 (IEC - TD) / PEB 20902 (IEC - TA), preliminary Target Specification 11.88, Siemens AG, 1988

[8] SBCX, S/T Bus Interface Circuit Extended, PEB 2081 V3.4, User's Manual 11.96, Siemens AG, 1996

[9] NTC-T, Network Termination Controller (4B3T), PEB 8090 V1.1, Data Sheet 06.98, Siemens AG, 1998

[10] INTC-Q, Intelligent Network Termination Controller (2B1Q), PEB 8191 V1.1, Data Sheet 10.97, Siemens AG, 1997

[11] Q-SMINTO, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(O**rdinary), PEF 80912
Q-SMINTIX, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent e**X**tended), PEF 81912
Q-SMINTI, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent), PEF 82912
V1.3, Data Sheets 03.01, Infineon AG, 2001

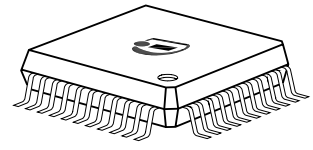
[12] IOM®-2 Interface Reference Guide, Siemens AG, 03.91

[13] SCOUT-S(X), Siemens Codec with S/T-Transceiver, PSB 2138x V1.1, Preliminary Data Sheet 08.98, Infineon Technologies AG, 1999

[14] PITA, PCI Interface for Telephony/Data Applications V0.3, SICAN GmbH, September1997

[15] Dual Channel SLICOFI-2, HV-SLIC; DUSLIC; PEB3265, 4265, 4266; Data Sheet DS2, Infineon Technologies, July 2000.

1.2 Features



P-MQFP-44

Features known from the PEB 8090

- Single chip solution including U- and S-transceiver
- Perfectly suited for the NT1 in the ISDN
- Fully automatic activation and deactivation
- U-interface (4B3T) conform to ETSI [1] and FTZ [2]:
  - Meets all transmission requirements on all ETSI and FTZ loops with margin
- S/T-interface conform to ETSI [4], ANSI [5] and ITU [6]
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
- Optional IOM®-2 interface eases chip testing and evaluation
- Power-on reset and Undervoltage Detection with no external components
- ESD robustness 2kV

Type	Package
PEF 80902	P-MQFP-44

New Features

- Optional use of transformers with non-negligible resistance corresponding to up to 20Ω on the line sidePin Vref and the according external capacitor removed
- Inputs accept 3.3V and 5V
- I/O (open drain) accepts pull-up to 3.3V[1)]
- Pin compatible with Q-SMINT®O (2nd Generation)
- LEDs indicating Loopback 2 and activation status
- Lowest power consumption due to
  - Low power CMOS technology (0.35µ)
  - Newly optimized low power libraries
  - High output swing on U- and S-line interface leads to minimized power consumption
  - Single 3.3 Volt power supply
- 185mW (NTC-T: 233mW) power consumption with random data over ETSI Loop 2.
- 15mW typical power consumption in power down (as NTC-T; NTC-Q: 28mW)

1.3 Not Supported are ...

- No integrated hybrid is provided by the T-SMINT®O. Therefore, an external hybrid is always required, which consists of only two additional resistors as compared to an integrated hybrid, but allows for more flexibility in board design.
- Auxiliary IOM®–2 interface
- SRA (capacitive receiver coupling is not suited for S-feeding)
- NT-Star with star point on the IOM®-2 bus (already not supported in NTC-T).

1) Pull-ups to 5V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

1.4 Pin Configuration

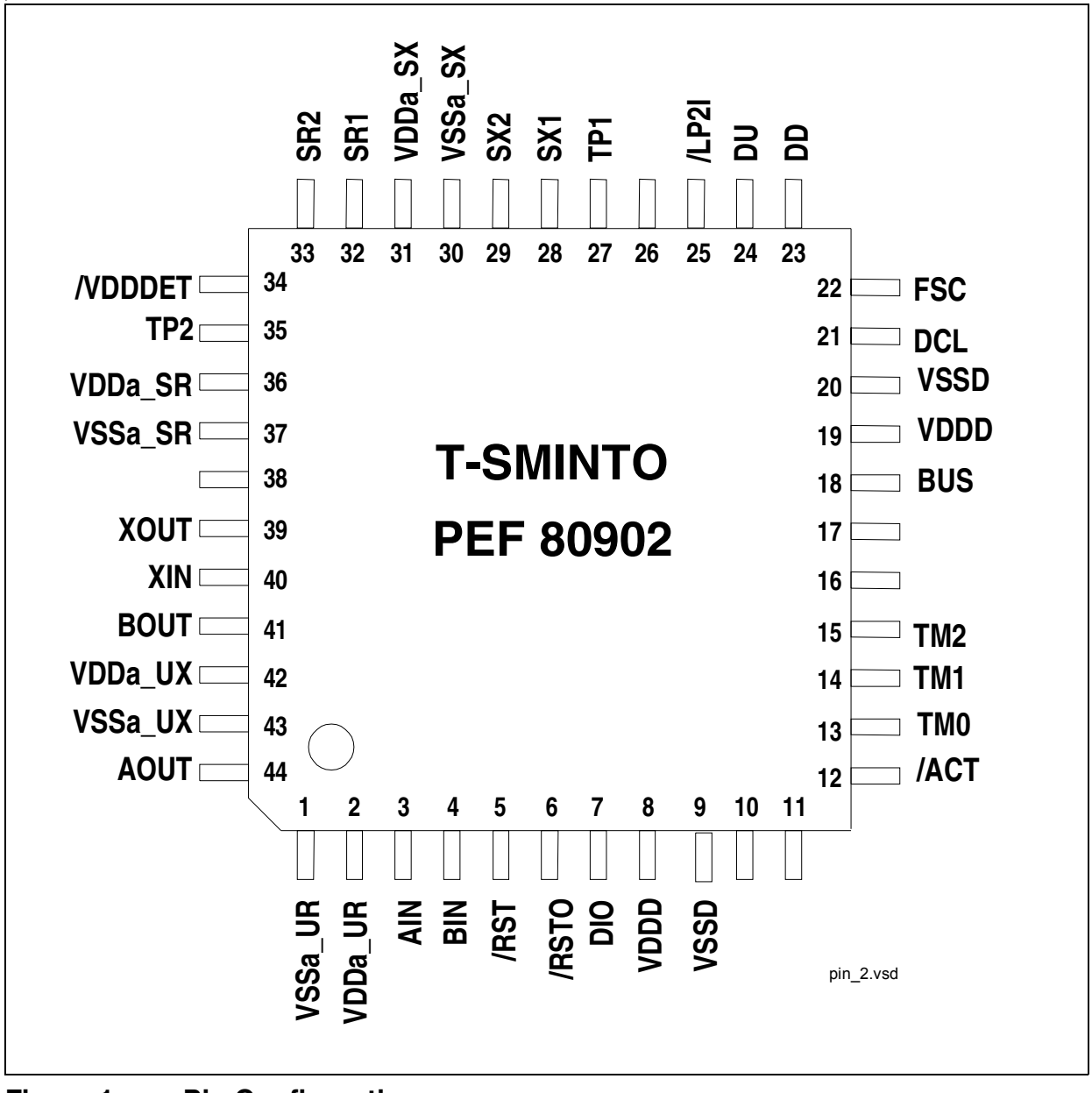


Figure 1 Pin Configuration

1.5 Block Diagram

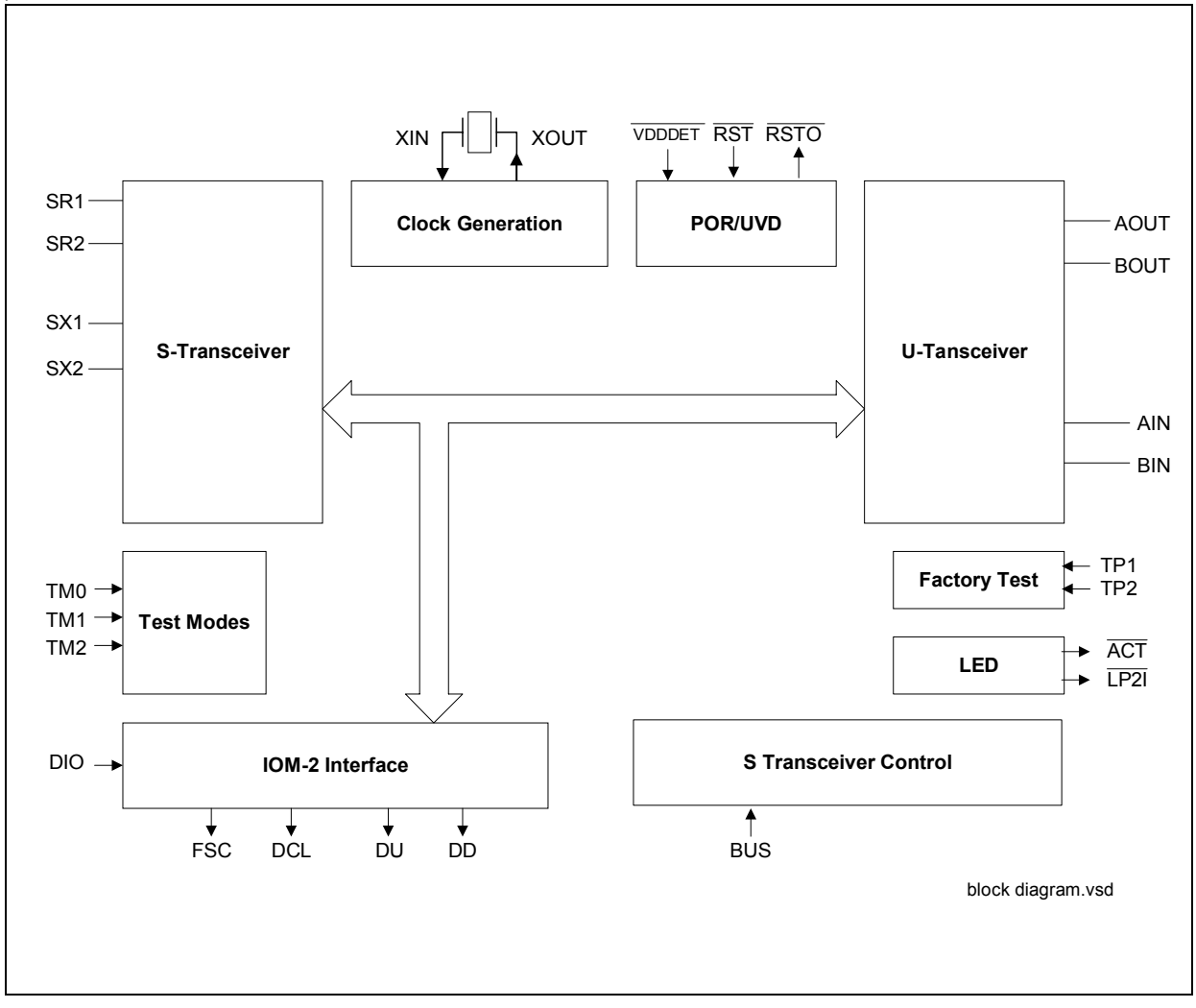


Figure 2 Block Diagram

1.6 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Pin		Symbol	Type	Function
2		VDDa_UR	–	Supply voltage for U-Receiver (3.3 V ± 5 %)
1		VSSa_UR	–	Analog ground (0 V) U-Receiver
42		VDDa_UX	–	Supply voltage for U-Transmitter (3.3 V ± 5 %)
43		VSSa_UX	–	Analog ground (0 V) U-Transmitter
36		VDDa_SR	–	Supply voltage for S-Receiver (3.3 V ± 5 %)
37		VSSa_SR	–	Analog ground (0 V) S-Receiver
31		VDDa_SX	–	Supply voltage for S-Transmitter (3.3 V ± 5 %)
30		VSSa_SX	–	Analog ground (0 V) S-Transmitter
19		VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
20		VSSD	–	Ground (0 V) digital circuits
8		VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
9		VSSD	–	Ground (0 V) digital circuits
22		FSC	O	**Frame Sync:** 8-kHz frame synchronization signal
21		DCL	O	**Data Clock:** IOM®-2 interface clock signal (double clock): 512 kHz
25		LP2I	O	**Loopback 2 indication:** Can directly drive a LED (4mA). 0: Loopback 2 closed 1: Loopback 2 not closed.
23		DD	I/O	**Data Downstream:** Data on the IOM®-2 interface

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
24		DU	I/O	**Data Upstream:** Data on the IOM®-2 interface
7		$\overline{\text{DIO}}$	I	Disable IOM®-2: 1: FSC, DCL, DU and DD high Z 0: FSC, DCL, DU and DD push-pull
18		BUS	I (PU)	**Bus mode on S-interface:** 1: passive S-bus (fixed timing) 0: point-to-point / extended passive S-bus (adaptive timing)
5		$\overline{\text{RST}}$	I	**Reset:** Low active reset input. Schmitt-Trigger input with hysteresis of typical 360mV. Tie to '1' if not used.
6		$\overline{\text{RSTO}}$	OD	**Reset Output:** Low active reset output.
13		TM0	I	**Test Mode 0.** Selects test pattern (see **Page 10**).
14		TM1	I	**Test Mode 1.** Selects test pattern (see **Page 10**).
15		TM2	I	**Test Mode 2.** Selects test pattern (see **Page 10**).
28		SX1	O	**S-Bus Transmitter Output (**positive**)**
29		SX2	O	**S-Bus Transmitter Output (**negative**)**
32		SR1	I	**S-Bus Receiver Input**
33		SR2	I	**S-Bus Receiver Input**
40		XIN	I	**Crystal 1:** Connected to a 15.36 MHz crystal
39		XOUT	O	**Crystal 2:** Connected to a 15.36 MHz crystal

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
44		AOUT	O	**Differential U-interface Output**
41		BOUT	O	**Differential U-interface Output**
3		AIN	I	**Differential U-interface Input**
4		BIN	I	**Differential U-interface Input**
34		$\overline{\text{VDDDET}}$	I	**VDD Detection:** This pin selects if the V_{DD} detection is active ('0') and reset pulses are generated on pin $\overline{\text{RSTO}}$ or whether it is deactivated ('1') and an external reset has to be applied on pin $\overline{\text{RST}}$.
12		$\overline{\text{ACT}}$	O	**Activation LED.** Indicates the activation status of U- and S-transceiver. Can directly drive a LED (4mA).
27		TP1	I	**Test Pin 1.** Used for factory device test. Tie to 'V_{SS}'
35		TP2	I	**Test Pin 2.** Used for factory device test. Tie to 'V_{SS}'
10,11, 16,17, 26,38				Tie to '1'

PU: Internal pull-up resistor (typ. 100µA)

I: Input

O: Output (Push-Pull)

OD: Output (Open Drain)

1.6.1 Specific Pins and Test Modes

LED Pins $\overline{\text{ACT}}$, $\overline{\text{LP2I}}$

A LED can be connected to pin **$\overline{\text{ACT}}$** to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U- and S-transceiver according to **Table 3**.

Table 3 ACT States

Pin $\overline{ACT}$	LED	U_Deactivated	U_Activated	S_Activated
V_{DD}	OFF	1	x	x
2Hz (1 : 1)*	fast flashing	0	0	x
1Hz (3 : 1)*	slow flashing	0	1	0
GND	ON	0	1	1

Note: * denotes the duty cycle 'high' : 'low'.

with:

U_Deactivated: 'Deactivated State' as defined in **Chapter 2.3.7.6**.

U_Activated: 'SBC Synchronizing', 'Wait for Info U4H', and 'Transparent' as defined in **Chapter 2.3.7.6**.

S-Activated: 'Activated State' as defined in **Chapter 2.4.5.1**.

Note: Optionally, pin $\overline{ACT}$ can drive a second LED with inverse polarity (connect this additional LED to 3.3V only).

Another LED can be connected to pin **$\overline{LP2I}$** to indicate an active Loopback 2 according to **Table 4.**

Table 4 LP2I States

Pin $\overline{LP2I}$	LED	Loopback 2 command in the C_L -channel
V_{DD}	off	received no loopback 2 command or loopback deactivation after a loopback 2 command.
GND	on	Loopback 2 command has been received. Complete analog loop is being closed on the S-interface.

Test Modes

Different test patterns on the U- and S-interface can be generated via pins TM0-2 according to **Table 5**.

Table 5 Test Modes

TM0	TM1	TM2	U-transceiver	S-transceiver
0	0	0	Reserved for future use. Normal operation in this version.	
0	0	1		
0	1	0	Normal operation	96 kHz[1)] Continuous Pulses
0	1	1		2 kHz[2)] Single Pulses

Table 5 Test Modes (cont'd)

TM0	TM1	TM2	U-transceiver	S-transceiver
1	0	0	Data Through[3]	Normal operation
1	0	1	Send Single Pulses[4]	
1	1	0	Quiet Mode[5]	
1	1	1	normal operation	

1) The S-transceiver transmits pulses with alternating polarity at a rate of 192 kHz resulting in a 96 kHz envelope.

2) The S-transceiver transmits pulses with alternating polarity at a rate of 4 kHz resulting in a 2 kHz envelope.

3) Forces the U-transceiver into the state 'Transparent' where it transmits signal U5.

4) Forces the U-transceiver to go into state 'Test' and to send single pulses. The pulses are issued at 1.0 ms intervals and have a duration of 8.33 µs.

5) The U-transceiver is hardware reset.

1.7 System Integration

The T-SMINT®O provides NT1 functionality without a microcontroller being necessary. Special selections can be done via pin strapping (DIO, BUS, TM0-2). The device has no µP interface.

The IOM®-2 Interface serves only for monitoring and debugging purposes. It can be regarded as a window to the internal IOM®-2.

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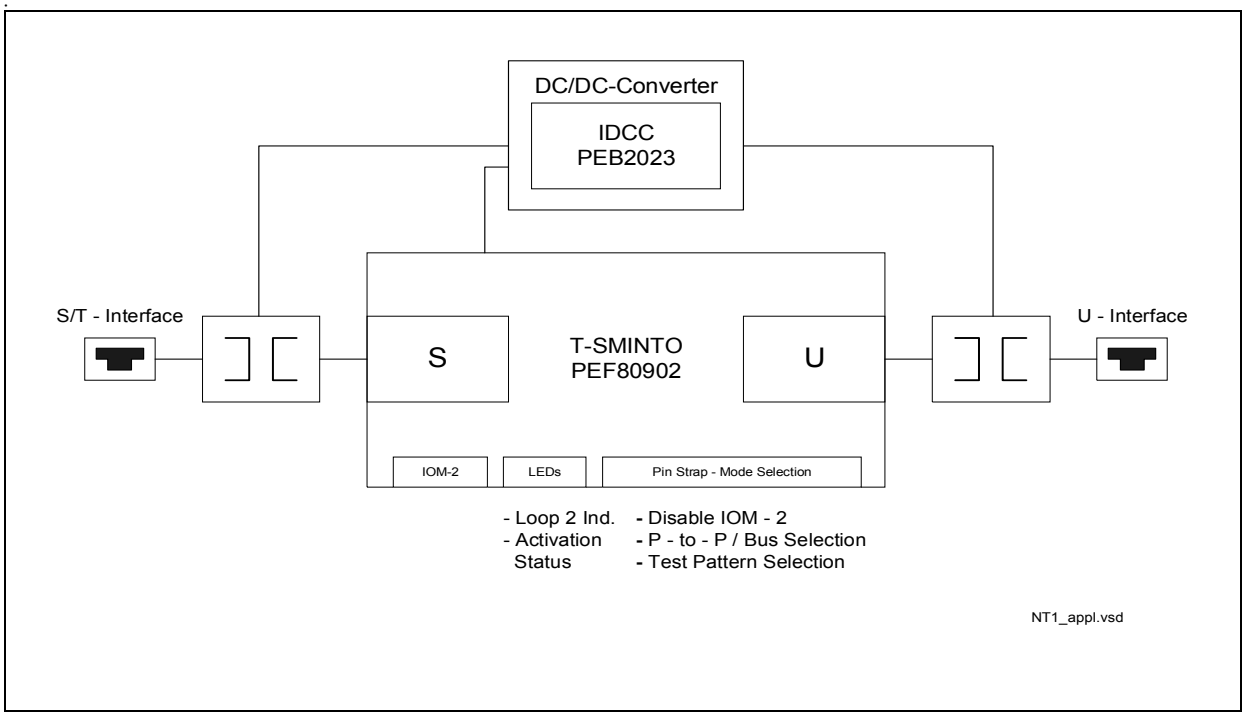

Figure 3 Application Example T-SMINT®O: Standard NT1

2 Functional Description

2.1 Reset Generation

External Reset Input

At the $\overline{\text{RST}}$ input an external reset can be applied forcing the T-SMINT®O in the reset state. This external reset signal is additionally fed to the $\overline{\text{RSTO}}$ output.

Reset Ouput

If $\overline{\text{VDDDET}}$ is active, then the deactivation of a reset output on $\overline{\text{RSTO}}$ is delayed by t_{DEACT} (see **Table 28**).

Reset Generation

The T-SMINT®O has an on-chip reset generator based on a Power-On Reset (POR) and Under Voltage Detection (UVD) circuit (see **Table 28**). The POR/UVD requires no external components.

The POR/UVD circuit can be disabled via pin $\overline{\text{VDDDET}}$.

The requirements on V_{DD} ramp-up during power-on reset are described in **Chapter 4.6.3**.

Clocks and Data Lines During Reset

During reset the data clock (DCL) and the frame synchronization (FSC) keep running.

During reset DD and DU are high; with the exception of:

- The output C/I code from the U-Transceiver on DD is 'DR' = 0000
- The output C/I code from the S-Transceiver on DU is 'TIM' = 0000.

2.2 IOM®-2 Interface

The IOM®-2 interface always operates in NT mode according to the IOM®-2 Reference Guide [12].

2.2.1 IOM®-2 Functional Description

The IOM®-2 interface consists of four lines: FSC, DCL, DD, DU. The rising edge of FSC indicates the start of an IOM®-2 frame. The DCL clock signal synchronizes the data transfer on both data lines DU and DD. The DCL is twice the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle.

Note: It is not possible to write any data via IOM®-2 into the T-SMINT®O.

The IOM®-2 interface can be enabled/disabled with pin DIO.

The FSC signal is an 8 kHz frame sync signal. The number of PCM timeslots on the transmit line is determined by the frequency of the DCL clock , with the 512 kHz clock 1 channel consisting of 4 timeslots is available.

IOM®-2 Frame Structure of the T-SMINT®O

The frame structure on the IOM®-2 data ports (DU,DD) of the T-SMINT®O with a DCL clock of 512 kHz is shown in **Figure 4.**

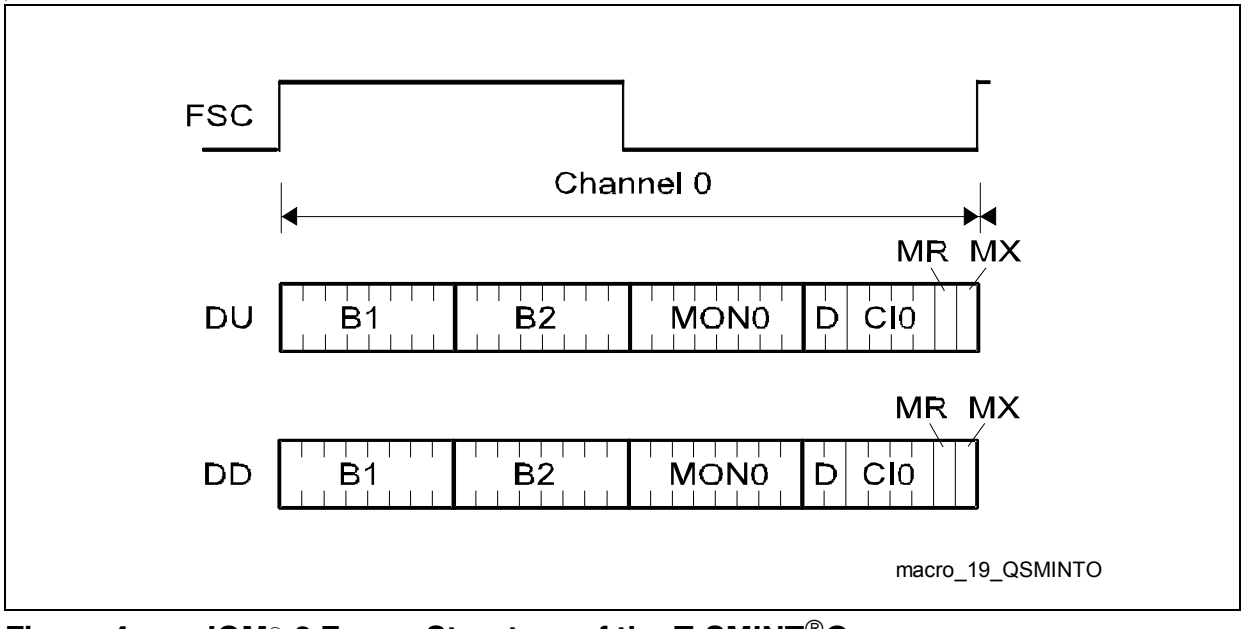

Figure 4 IOM®-2 Frame Structure of the T-SMINT®O

The frame is composed of one channel:

- Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (not available in T-SMINT®O) and a command/indication channel (CI0) for control of e.g. the U-transceiver.

2.3 U-Transceiver

The statemachine of the U-Transceiver is compatible to the NT state machine in the PEB 8090 documentation [9], but includes some minor changes for simplification and compliance to Ref. [1].

Basic configurations are selected via pin strapping

2.3.1 4B3T Frame Structure

The 4B3T U-interface performs full duplex data transmission and reception at the U-reference point according to ETSI TS 102 080 and FTZ 1TR 220. It applies the 4B3T block code together with adaptive echo cancelling and equalization. Transmission performance shall be such, that it meets all ETSI and FTZ test loops with margin.

The U-interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

The following information is transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock
  - 1 kHz Frame
  - Activation
  - 1 kbit/s Transparent Channel (M symbol), (not implemented)
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops (M symbol)
- From NT to LT side:
  - Indication of monitored code violations (M symbol)

Performance Requirements according to FTZ 1 TR 220 (August 1991):

On the U-interface, the following transmission ranges are achieved without additional signal regeneration on the loop (bit error rate $\leq 10^{-7}$):

- with noise: ≥ 4.2 km on wires of 0.4 mm diameter and ≥ 8 km on 0.6 mm wires
- without noise: ≥ 5 km on wires of 0.4 mm diameter and ≥ 10 km on 0.6 mm wires

Note: Typical attenuation of FTZ wires of 0.4 mm diameter is about 7dB/km in contrast to ETSI wires of 0.4 mm with about 8dB/km.

The transmission ranges can be doubled by inserting a repeater for signal regeneration.

Performance requirements according to ETSI TS 102 080 are met, too.

1 ms frames are transmitted via the U-interface, each consisting of:

- 108 symbols: 144 bit scrambled and coded B1 + B2 + D data

- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM®-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different syncwords are used for each direction:

- Downstream from LT to NT + + + – – – + – – + –
- Upstream from NT to LT – + – – + – – – + + +

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

Table 6 Frame Structure A for Downstream Transmission LT to NT

1 D_1	2 D_1	3 D_1	4 D_1	5 D_1	6 D_1	7 D_1	8 D_1	9 D_1	10 D_1	11 D_1	12 D_1
13 $D_{1/2}$	14 $D_{1/2}$	15 $D_{1/2}$	16 D_2	17 D_2	18 D_2	19 D_2	20 D_2	21 D_2	22 D_2	23 D_2	24 D_2
25 D_2	26 D_2	27 D_2	28 D_3	29 D_3	30 D_3	31 D_3	32 D_3	33 D_3	34 D_3	35 D_3	36 D_3
37 D_3	38 D_3	39 D_3	40 $D_{3/4}$	41 $D_{3/4}$	42 $D_{3/4}$	43 D_4	44 D_4	45 D_4	46 D_4	47 D_4	48 D_4
49 D_4	50 D_4	51 D_4	52 D_4	53 D_4	54 D_4	55 D_5	56 D_5	57 D_5	58 D_5	59 D_5	60 D_5
61 D_5	62 D_5	63 D_5	64 D_5	65 D_5	66 D_5	67 $D_{5/6}$	68 $D_{5/6}$	69 $D_{5/6}$	70 D_6	71 D_6	72 D_6
73 D_6	74 D_6	75 D_6	76 D_6	77 D_6	78 D_6	79 D_6	80 D_6	81 D_6	82 D_7	83 D_7	84 D_7
85 **M**	86 D_7	87 D_7	88 D_7	89 D_7	90 D_7	91 D_7	92 D_7	93 D_7	94 D_7	95 $D_{7/8}$	96 $D_{7/8}$
97 $D_{7/8}$	98 D_8	99 D_8	100 D_8	101 D_8	102 D_8	103 D_8	104 D_8	105 D_8	106 D_8	107 D_8	108 D_8
109 D_8	110 **+**	111 **+**	112 **+**	113 **–**	114 **–**	115 **–**	116 **+**	117 **–**	118 **–**	119 **+**	120 **–**

D_1 ... D_8	Ternary 2B + D data of IOM®-2 frames 1 ... 8
M	Maintenance symbol
+, –	Syncword